

Features

- ESD/Surge protection for two lines with bi-directional
- Provide transient protection for each line to **IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air), $\pm 30\text{kV}$ (contact) IEC 61000-4-5 (Lightning) 6A (8/20 μs) Cable Discharge Event (CDE)**
- Provide ISO 7637-3
Pulse 3a: -200V
Pulse 3b: +200V
- Suitable for, 24V and below, operating voltage applications
- Fast turn-on and low clamping voltage
- Array of ESD rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**
- **AEC-Q101 qualified**

Applications

- CAN bus protection
- Automotive application
- Industrial control
- Power management system
- Set-top box
- Notebooks, desktops, and servers
- Portable instrumentation
- Peripherals

Description

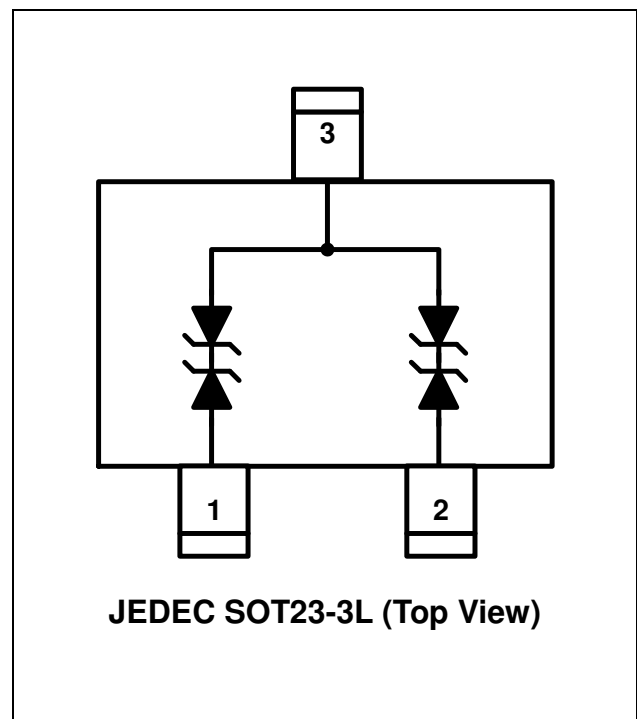
AZ9424-02S is a design which includes ESD /surge rated clamping cell arrays to protect the power lines or control lines in an electronic system. The AZ9424-02S has been specifically designed to protect sensitive components which

are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ9424-02S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ9424-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





SPECIFICATIONS

| ABSOLUTE MAXIMUM RATINGS | | | |
|--|--------------------|---------------|------|
| PARAMETER | SYMBOL | RATING | UNIT |
| Peak Pulse Current (tp=8/20μs) | I _{PP} | 6 | A |
| Operating Supply Voltage (I/O pin-GND) | V _{DC} | ±26 | V |
| ESD per IEC 61000-4-2 (Air) | V _{ESD-1} | ±30 | kV |
| ESD per IEC 61000-4-2 (Contact) | V _{ESD-2} | ±30 | |
| Lead Soldering Temperature | T _{SOL} | 260 (10 sec.) | °C |
| Operating Temperature | T _{OP} | -55 to +125 | °C |
| Storage Temperature | T _{STO} | -55 to +150 | °C |

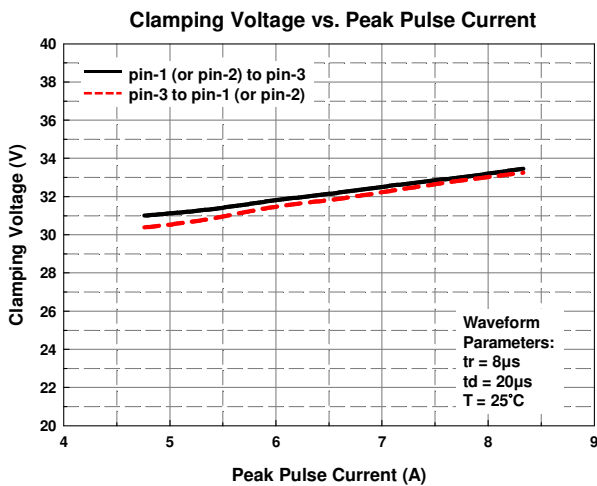
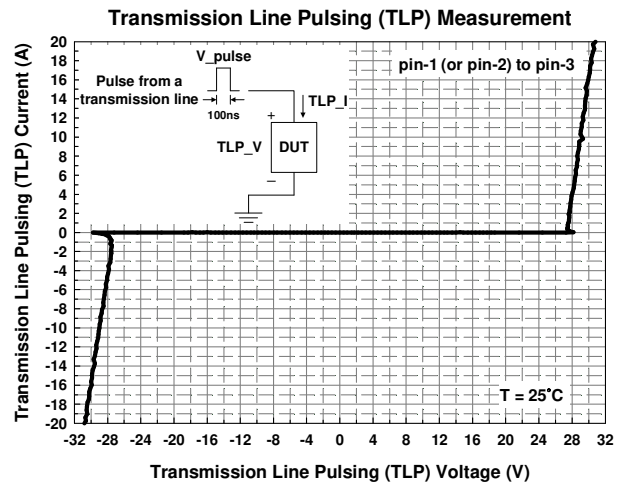
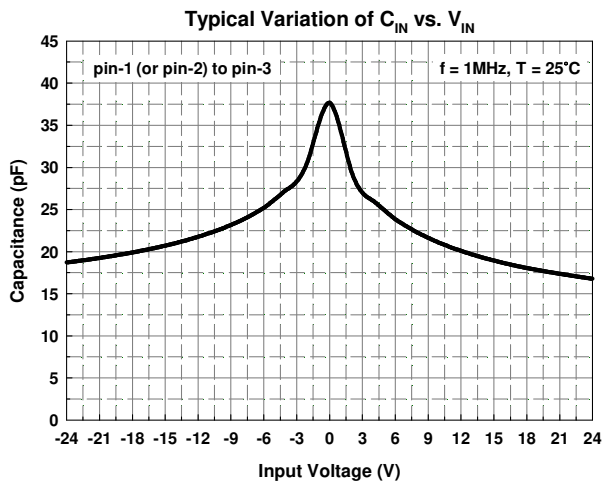
| ELECTRICAL CHARACTERISTICS | | | | | | |
|--------------------------------|-----------------------|---|------|-----|------|------|
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
| Reverse Stand-Off Voltage | V _{RWM} | Pin-1, -2 to pin-3, T=25°C | -24 | | 24 | V |
| Reverse Leakage Current | I _{Leak} | V _{RWM} = ±24V, pin-1, -2 to pin-3, T=25°C | | | 100 | nA |
| Reverse Breakdown Voltage | V _{BV} | I _{BV} = 1mA, pin-1, -2 to pin-3, T=25°C | 26.2 | | 33.5 | V |
| Surge Clamping Voltage | V _{CL-surge} | I _{PP} = 5A, tp = 8/20μs, pin-1, -2 to pin-3, T = 25°C | | 31 | | V |
| ESD Clamping Voltage (Note 1) | V _{CL-ESD} | IEC 61000-4-2 +8kV (I _{TLP} = 16A), contact mode, pin-1, -2 to pin-3, T=25°C | | 31 | | V |
| ESD Dynamic Turn-on Resistance | R _{dynamic} | IEC 61000-4-2 0~+8kV, contact mode, pin-1, -2 to pin-3, T=25°C | | 0.2 | | Ω |
| Channel Input Capacitance | C _{IN} | V _R = 0V, f = 1MHz, pin-1, -2 to pin-3, T=25°C | | 38 | 45 | pF |

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z₀= 50Ω, t_p= 100ns, t_r= 1ns.



Typical Characteristics



Application Information

The AZ9424-02S is designed to protect two lines against system ESD/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9424-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin 2, respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9424-02S should be kept as short as possible.

In order to obtain enough suppression of

ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9424-02S.
- Place the AZ9424-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

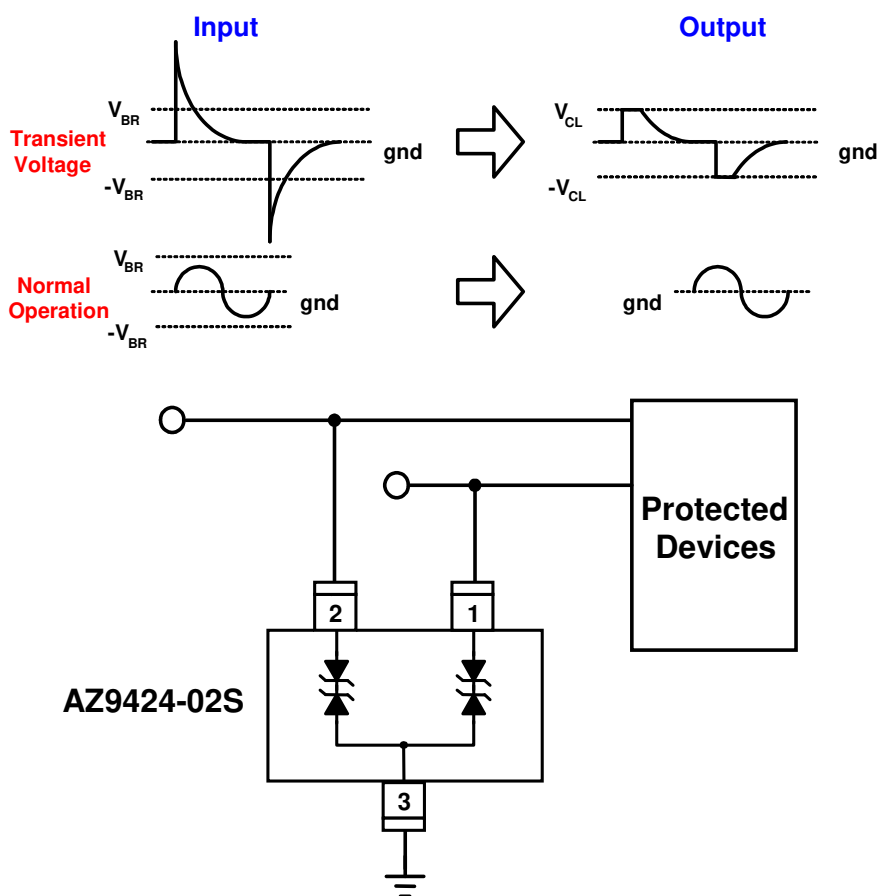
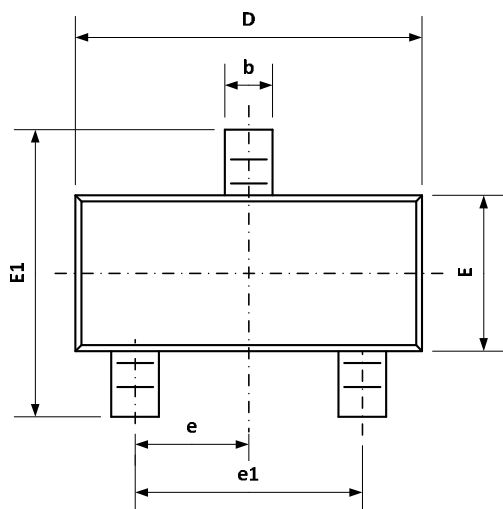


Fig. 1 The ESD protection scheme by using AZ9424-02S.

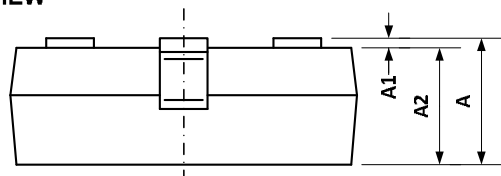
Mechanical Details

SOT23-3L PACKAGE DIAGRAMS

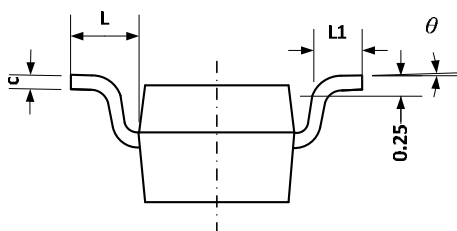
TOP VIEW



SIDE VIEW



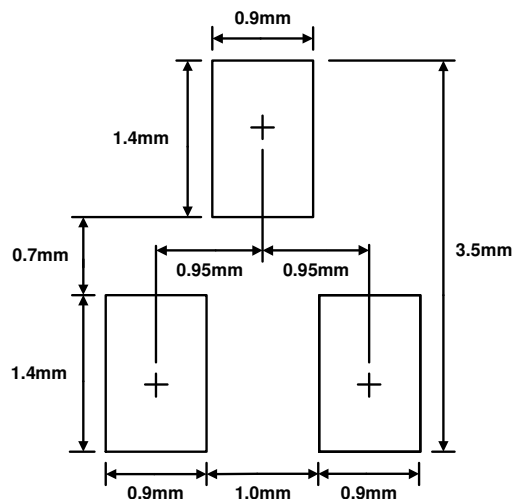
END VIEW



PACKAGE DIMENSIONS

| SYMBOL | MILLIMETERS | |
|----------|-------------|------|
| | MIN. | MAX. |
| A | 0.90 | 1.15 |
| A1 | 0.00 | 0.10 |
| A2 | 0.90 | 1.05 |
| b | 0.30 | 0.50 |
| c | 0.08 | 0.15 |
| D | 2.80 | 3.00 |
| E | 1.20 | 1.40 |
| E1 | 2.25 | 2.55 |
| e | 0.95 TYP | |
| e1 | 1.80 | 2.00 |
| L | 0.55 REF | |
| L1 | 0.30 | 0.50 |
| θ | 0 | 8 |

LAND LAYOUT



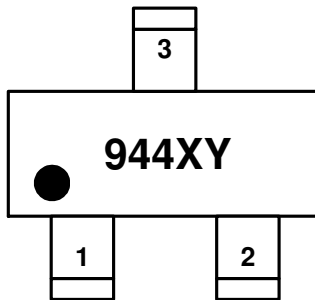
Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Note : Green means Pb-free, RoHS, and Halogen free compliant.



MARKING CODE



944 = Device Code
X = Date Code
Y = Control Code

| Part Number | Marking Code |
|--------------------------------|--------------|
| AZ9424-02S.R7G (Green Part) | 944XY |

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

| PN# | Material | Type | Reel size | MOQ | MOQ/internal box | MOQ/carton |
|----------------|----------|------|-----------|------------|--------------------|-----------------------|
| AZ9424-02S.R7G | Green | T/R | 7 inch | 3,000/reel | 4 reels=12,000/box | 6 boxes=72,000/carton |

Revision History

| Revision | Modification Description |
|---------------------|--------------------------|
| Revision 2018/11/07 | Preliminary Release. |
| Revision 2019/04/26 | Formal Release. |
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