PHD97NQ03LT

N-channel TrenchMOS logic level FET

Rev. 01 — 24 March 2009 | Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Fast switching
- Lead-free packing
- Logic level threshold
- Low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Computer motherboard high frequency DC-to-DC convertors
- Switched-mode power supplies
- Voltage regulators

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	25	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	107	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5$ V; $I_D = 25$ A; $V_{DS} = 12$ V; see Figure 9; see Figure 10	-	1.9	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 7; see Figure 8	-	5.3	6.3	mΩ

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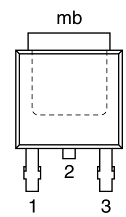
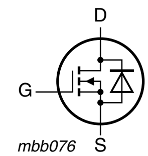
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT428 (SC-63; DPAK)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

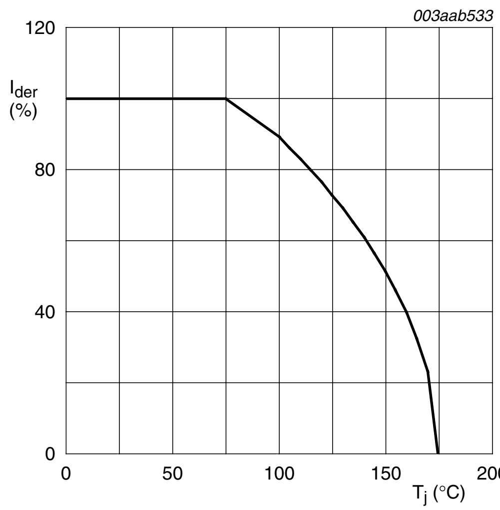
Type number	Package		
	Name	Description	Version
PHD97NQ03LT	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

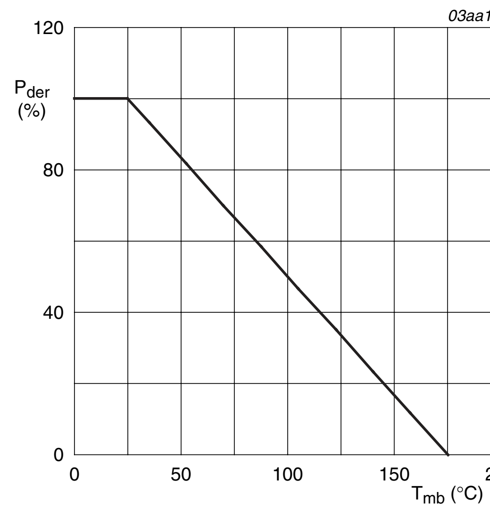
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C	-	25	V
V_{DGR}	drain-gate voltage	T_j ≥ 25 °C; T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	69	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	-	75	A
I_{DM}	peak drain current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	300	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	107	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	75	A
I_{SM}	peak source current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C	-	240	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 35 A; V_{sup} ≤ 25 V; unclamped; t_p = 0.1 ms; R_{GS} = 50 Ω	-	60	mJ



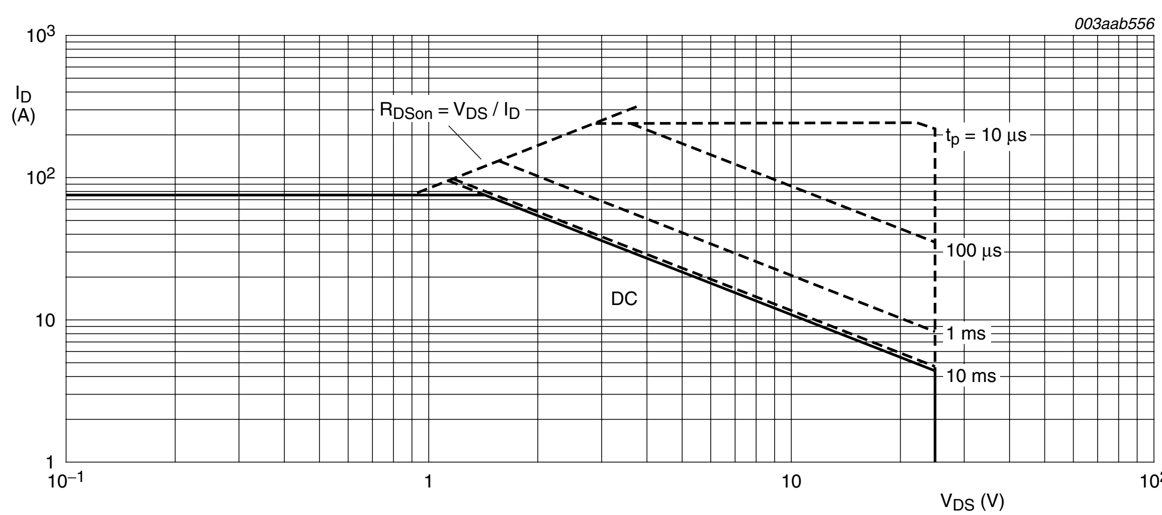
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25\,°C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4		-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	75	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air

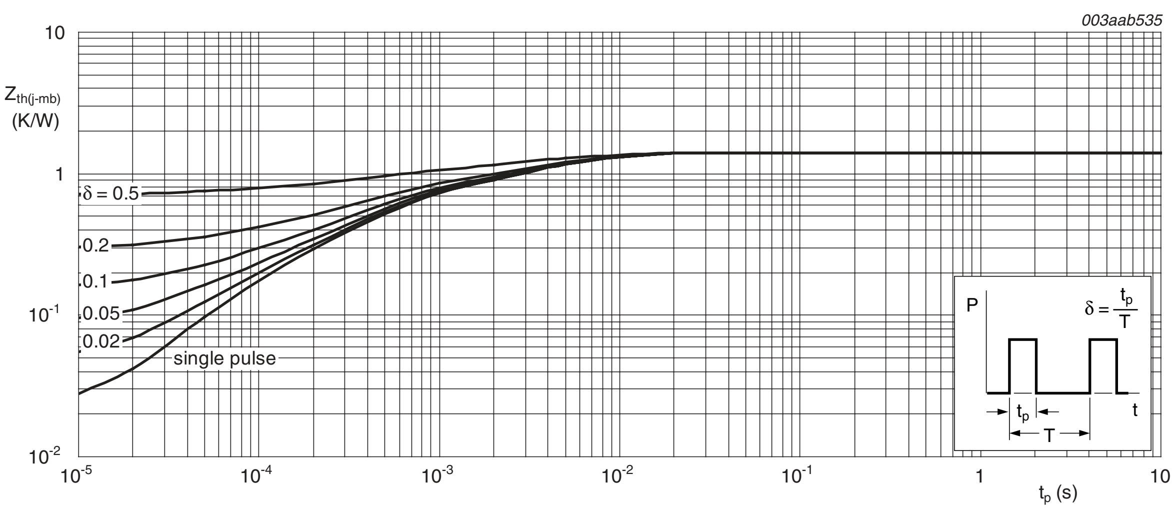


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

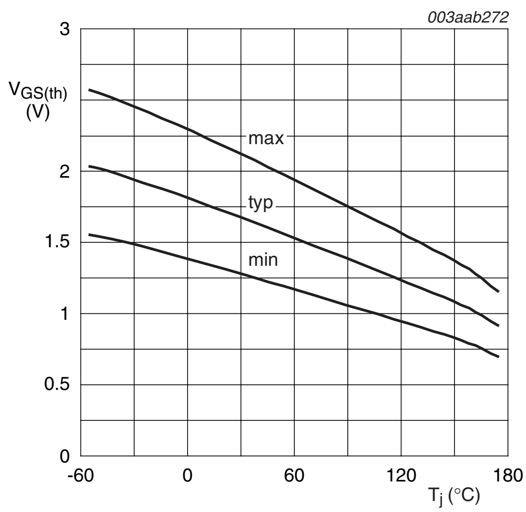
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	25	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 5; see Figure 6	1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 5	0.7	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 5	-	-	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 7; see Figure 8	-	10.1	12	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 7; see Figure 8	-	8	10.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 7; see Figure 8	-	5.3	6.3	mΩ
I_{DSS}	drain leakage current	V_{DS} = 25 V; V_{GS} = 0 V; T_j = 175 °C	-	-	100	µA
R_G	gate resistance	f = 1 MHz	-	1.5	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 9; see Figure 10	-	11.7	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V	-	10.2	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 9; see Figure 10	-	6.2	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	3.4	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.8	-	nC
Q_{GD}	gate-drain charge		-	1.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; see Figure 9; see Figure 10	-	3.1	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 11	-	1570	-	pF
		V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	1800	-	pF
C_{oss}	output capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 11	-	380	-	pF
C_{rss}	reverse transfer capacitance		-	160	-	pF

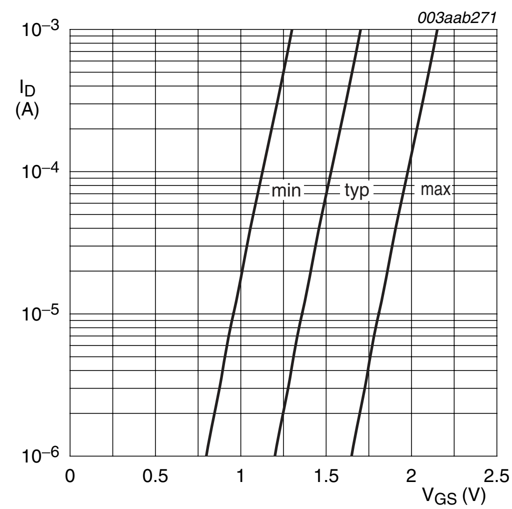
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω	-	18	-	ns
t_r	rise time		-	33	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	12	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	38	-	ns
Q_r	recovered charge		-	14	-	nC



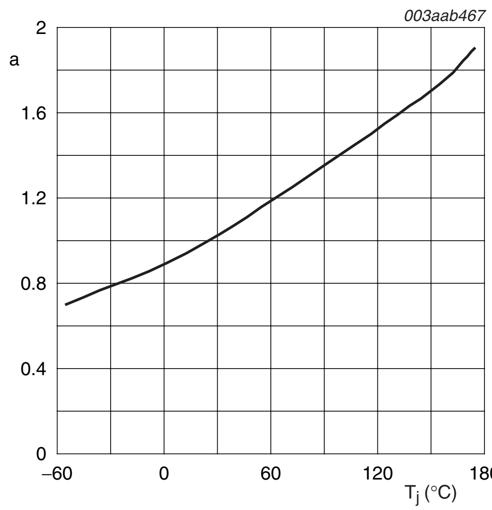
$I_D = 1 mA; V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature



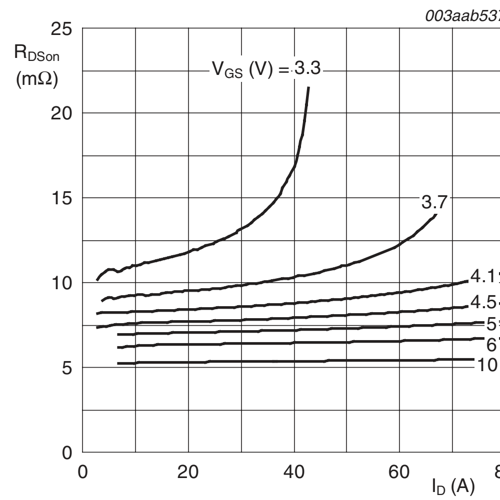
$T_j = 25\,°C; V_{DS} = 5 V$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



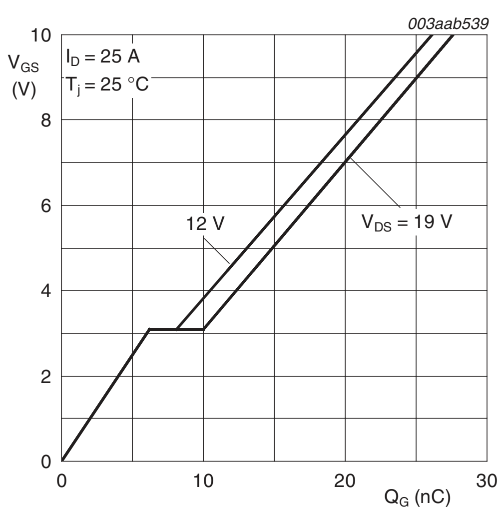
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25°C$$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$$I_D = 25A; V_{DS} = 12V and 19V$$

Fig 9. Gate-source voltage as a function of gate charge; typical values

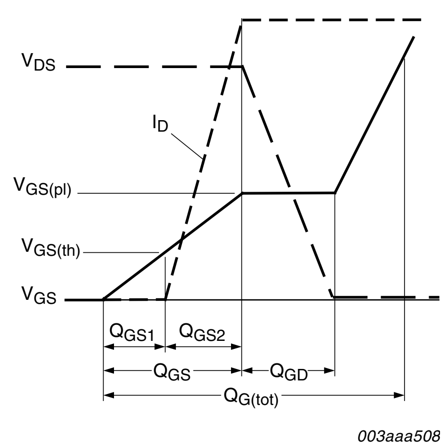
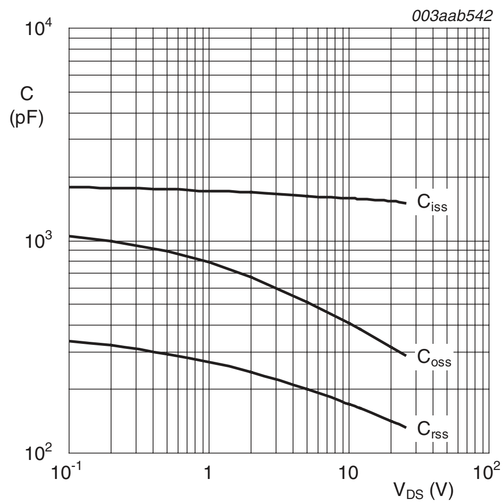
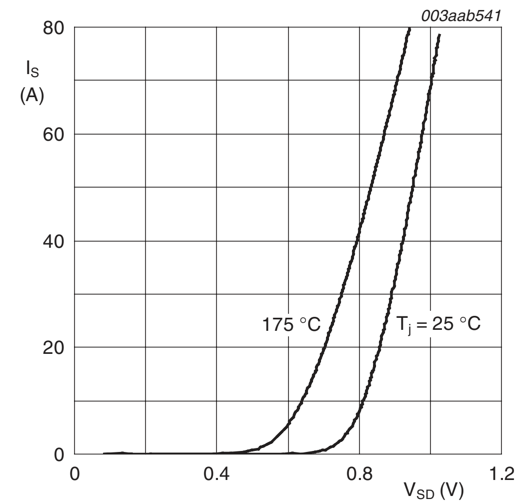


Fig 10. Gate charge waveform definitions



$V_{GS} = 0 V; f = 1 MHz$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

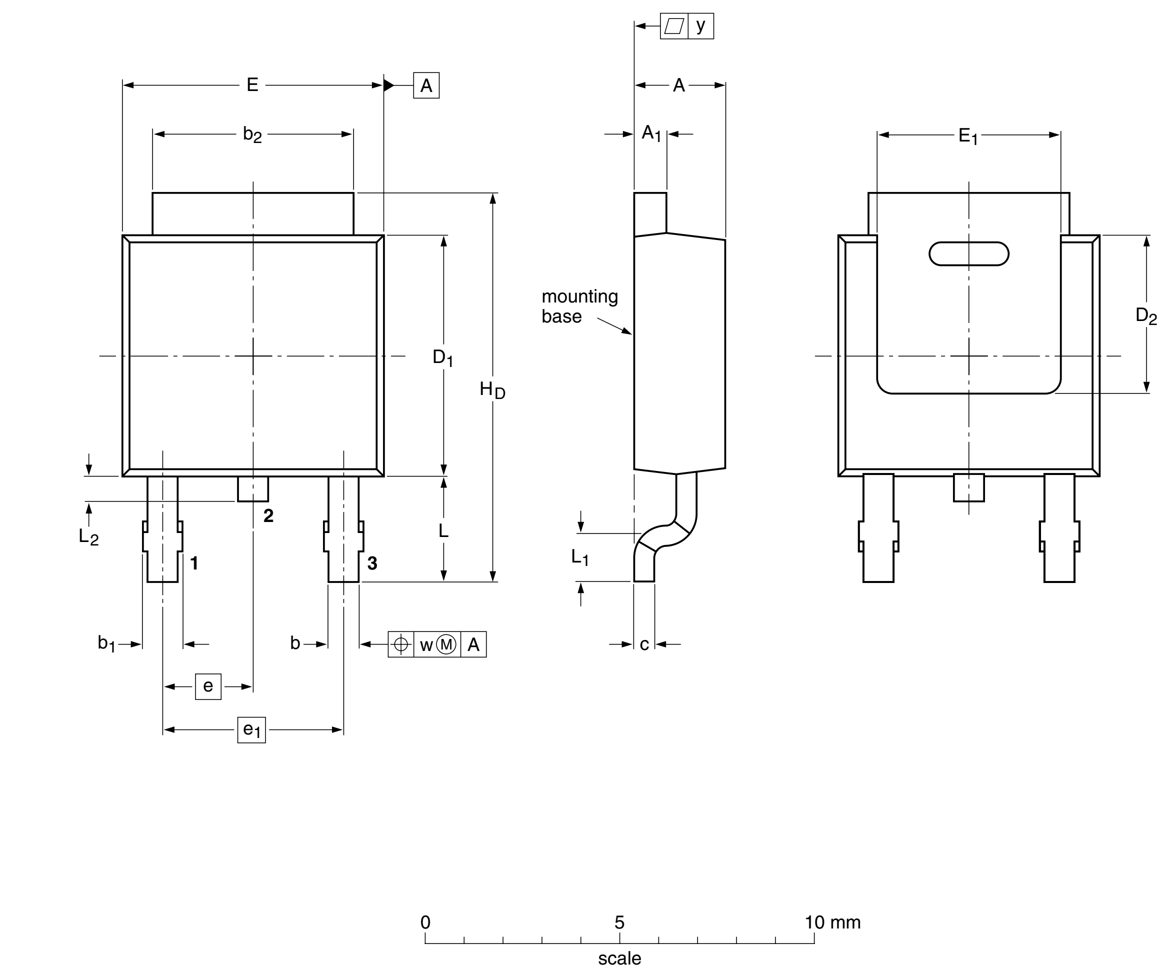


$T_j = 25 °C$ and $175 °C; V_{GS} = 0V$

Fig 12. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 13. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD97NQ03LT_1	20090324	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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Date of release: 24 March 2009