MOSFET – Dual, N-Channel, Small Signal, ESD Protection, SC-88 20 V

Features

- Small Footprint (2 x 2 mm)
- Low Gate Charge N-Channel Device
- ESD Protected Gate
- Same Package as SC-70 (6 Leads)
- AEC-Q101 Qualified and PPAP Capable NVJD4401N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Load Power Switching
- Li-Ion Battery Supplied Devices
- Cell Phones, Media Players, Digital Cameras, PDAs
- DC-DC Conversion

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Param	Symbol	Value	Unit			
Drain-to-Source Voltage	V _{DSS}	20	V			
Gate-to-Source Voltage			V _{GS}	±12	٧	
Continuous Drain Current	Steady State	T _A = 25°C	I _D	0.63	Α	
(Based on R _{θJA})	State	T _A = 85°C		0.46		
Power Dissipation	Steady State	T _A = 25°C	P _D	0.27	W	
(Based on R _{θJA})	State	T _A = 85°C		0.14		
Continuous Drain Current	Steady State	T _A = 25°C	I _D	0.91	Α	
(Based on R _{θJL})	State	T _A = 85°C		0.65		
Power Dissipation	Steady State	T _A = 25°C		0.55	W	
(Based on R _{θJL})	State	T _A = 85°C	P_{D}	0.29		
Pulsed Drain Current		t ≤10 μs	I _{DM}	±1.2	Α	
Operating Junction and	T _J , T _{STG}	–55 to 150	°C			
Continuous Source Curr	I _S	0.63	Α			
Lead Temperature for So (1/8" from case for 10 s)	oldering P	urposes	T_L	260	°C	

THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Тур	Max	Units
Junction-to-Ambient - Steady State	$R_{\theta JA}$	400	458	°C/W
Junction-to-Lead (Drain) - Steady State	$R_{ heta JL}$	194	252	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1

1. Surface mounted on FR4 board using 1 oz Cu area = 0.9523 in sq.

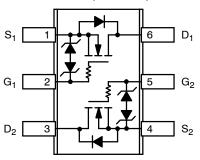


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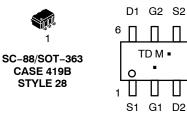
	V _{(BR)DSS}	R _{DS(on)} Typ	I _D Max
ı	20 V	0.29 Ω @ 4.5 V	0.63 A
		0.36 Ω @ 2.5 V	0.03 A

SC-88 (SOT-363)



Top View

MARKING DIAGRAM & PIN ASSIGNMENT



TD = Device Code

M = Date Code

Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Con	dition	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•		•		•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V, } I_D$	= 250 μΑ	20	27		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				22		mV/ °C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V	_{DS} = 16 V			1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{C}$	_{SS} = ±12 V			10	μА
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{DS}$	_O = 250 μA	0.6	0.92	1.5	V
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-2.1		mV/ °C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I	_D = 0.63 A		0.29	0.375	Ω
		V _{GS} = 2.5 V, I	_D = 0.40 A		0.36	0.445	
Forward Transconductance	9FS	V _{DS} = 4.0 V, I _D = 0.63 A			2.0		S
CHARGES AND CAPACITANCES					-		-
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 20 \text{ V}$			33	46	pF
Output Capacitance	Coss				13	22	
Reverse Transfer Capacitance	C _{RSS}				2.8	5.0	1
Total Gate Charge	Q _{G(TOT)}				1.3	3.0	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V	_{'ns} = 10 V,		0.1		
Gate-to-Source Charge	Q _{GS}	I _D = 0.6	3 A		0.2		7
Gate-to-Drain Charge	Q_{GD}		Ī		0.4		1
SWITCHING CHARACTERISTICS (No	ote 3)				-		
Turn-On Delay Time	td _(ON)				0.083		μS
Rise Time	tr	V _{GS} = 4.5 V, V	nn = 10 V,		0.227		1
Turn-Off Delay Time	td _(OFF)	$I_D = 0.5 A, F$	$R_{\rm G} = 20 \ \Omega$		0.786		1
Fall Time	tf				0.506		
DRAIN-SOURCE DIODE CHARACTE	RISTICS		•		-	-	
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 V$	T _J = 25°C		0.76	1.1	V
		I _S =0.23 A	T _J = 125°C		0.63		1
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt$ $I_{S} = 0.6$			0.410		μs

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

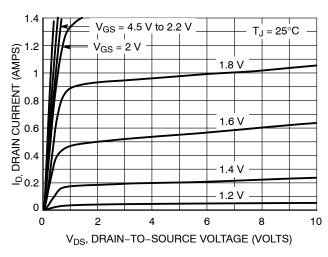


Figure 1. On-Region Characteristics

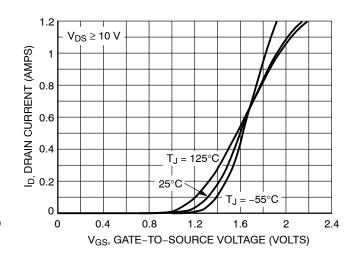


Figure 2. Transfer Characteristics

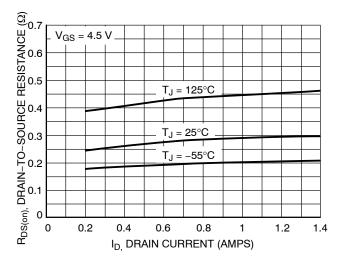


Figure 3. On-Resistance vs. Drain Current and Temperature

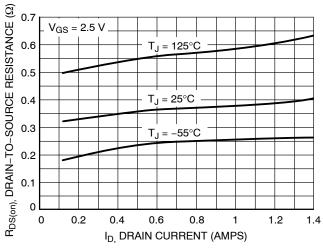


Figure 4. On-Resistance vs. Drain Current and Temperature

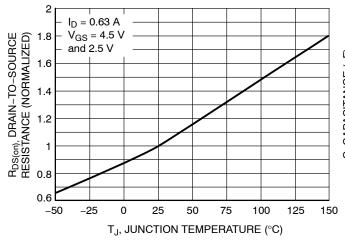


Figure 5. On–Resistance Variation with Temperature

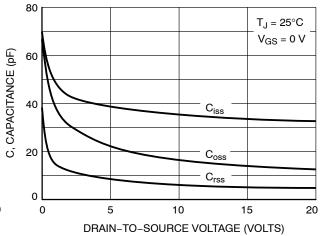


Figure 6. Capacitance Variation

$\textbf{TYPICAL PERFORMANCE CURVES} \ (T_J = 25^{\circ}\text{C unless otherwise noted})$

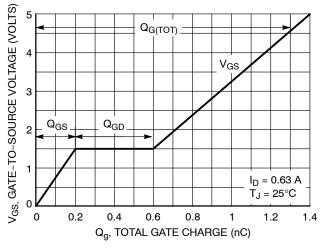


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

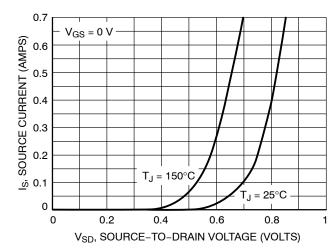


Figure 8. Diode Forward Voltage vs. Current

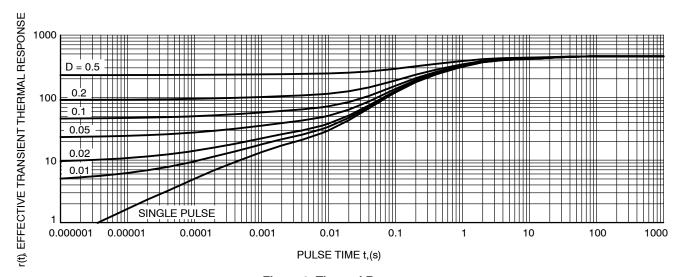


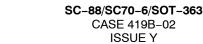
Figure 9. Thermal Response

ORDERING INFORMATION

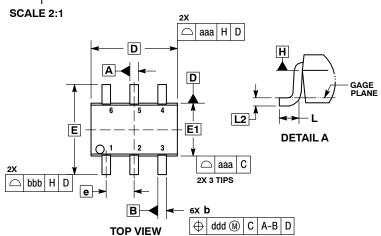
Device	Package	Shipping [†]
NTJD4401NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel
NVJD4401NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel

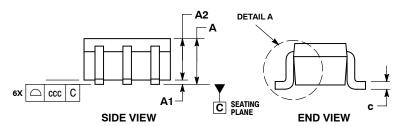
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





DATE 11 DEC 2012





NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M. 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU-SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.

- SIONS, OH GAILE BURHS SHALL NOT EXCEED 0.20 PEH END.
 DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF
 THE PLASTIC BODY AND DATUM H.
 DATUMS A AND B ARE DETERMINED AT DATUM H.
 DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE
 LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MIL	MILLIMETERS			INCHES	;
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α			1.10			0.043
A1	0.00		0.10	0.000		0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
С	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
е		0.65 BS	С	0	.026 BS	С
L	0.26	0.36	0.46	0.010	0.014	0.018
L2		0.15 BSC			0.006 BS	SC
aaa	0.15				0.006	
bbb	0.30				0.012	
ccc		0.10			0.004	
ddd		0.10			0.004	

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

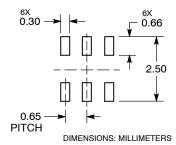
= Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

- *Date Code orientation and/or position may vary depending upon manufacturing location.
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SC-88/SC70-6/SOT-363 CASE 419B-02 ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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