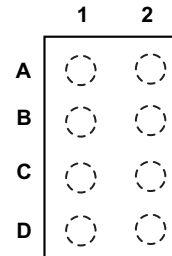


## A Inter Chip-USB Voltage Level Translator

Check for Samples: [TXS0202](#)

### FEATURES

- **No Direction Control Signal Required**
- **V<sub>CCA</sub>, V<sub>CCB</sub> Supply Voltage: 1.65 V to 3.6 V**
- **Meets All Requirements of the IC-USB Standard**
- **Small Packages: WCSP**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **I<sub>off</sub> Supports Partial-Power-Down Mode Operation**
- **ESD Performance**
  - **A port (Host-Side)**
    - **2000-V Human-Body Model**
    - **100-V Machine Model**
    - **500-V Charged-Device Model**
  - **B port (Peripheral-Side)**
    - **>4kV HBM**



**Table 1. YZP TERMINAL ASSIGNMENTS (Top Through View)**

	1	2
<b>A</b>	D+(B)	D–(B)
<b>B</b>	GND	V <sub>CCB</sub>
<b>C</b>	V <sub>CCA</sub>	OE
<b>D</b>	D+(A)	D–(A)

### DESCRIPTION

The TXS0202 is a 2-bit voltage level translator optimized for use in Interchip USB (IC-USB) applications. V<sub>CCA</sub> and V<sub>CCB</sub> can each operate over the full range of 1.65 V to 3.6 V. The device has been designed to maintain cross-over skew to be less than 1 ns. The device has integrated pull-ups and pull-down resistors to aid in the protocol communication between a host and a peripheral. The translator is a buffered auto-direction sensing type translator. When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YZP	Tape and reel	TXS0202YZPR	___7PS_ <sup>(3)</sup>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site.

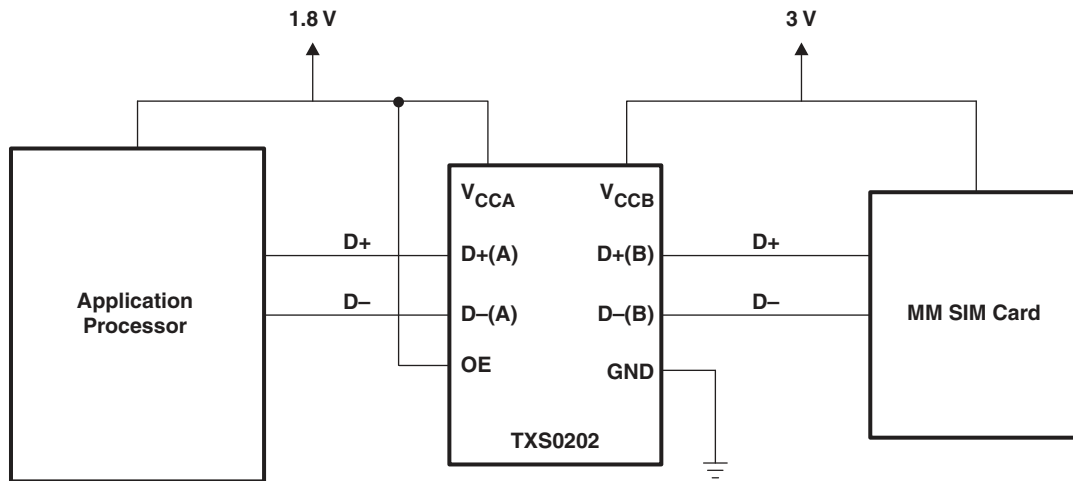


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**TYPICAL APPLICATION BLOCK DIAGRAM**



**PIN FUNCTIONS**

PIN		DESCRIPTION
WSCP (YFP) BALL NO.	NAME	
A1	D+(B)	USB data signal connected to peripheral
A2	D-(B)	USB data signal connected to peripheral
B1	GND	Ground
B2	V <sub>CCB</sub>	B-side supply voltage (1.65 V to 3.6 V)
C1	V <sub>CCA</sub>	A-side supply voltage (1.65 V to 3.6 V)
C2	OE	Output enable input control
D1	D+(A)	USB data signal connected to host
D2	D-(A)	USB data signal connected to host

**FUNCTIONAL TABLE**

CONTROL INPUT	OUTPUT CIRCUIT	OPERATION
OE	B PORT	
L	Hi-Z	Isolation
H	Enabled	Bi-directional communications between host and peripheral

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage rang	-0.5	4.6	V
$V_I$	Input voltage range	A port, B port, control inputs		V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state	A port, B port		V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_{CC}$ $I_{GND}$	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		±100	mA
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TXS0202	UNITS
		YZP	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{CCA}$ , $V_{CCB}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	A port I/Os	$V_{CCA} - 0.2$	$V_{CCA}$
		B port I/Os	$V_{CCB} - 0.2$	$V_{CCB}$
		OE	$V_{CCA} \times 0.65$	3.6
$V_{IL}$	Low-level input voltage	A port I/Os	0	0.15
		B port I/Os	0	0.15
		OE	0	$V_{CCA} \times 0.35$
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

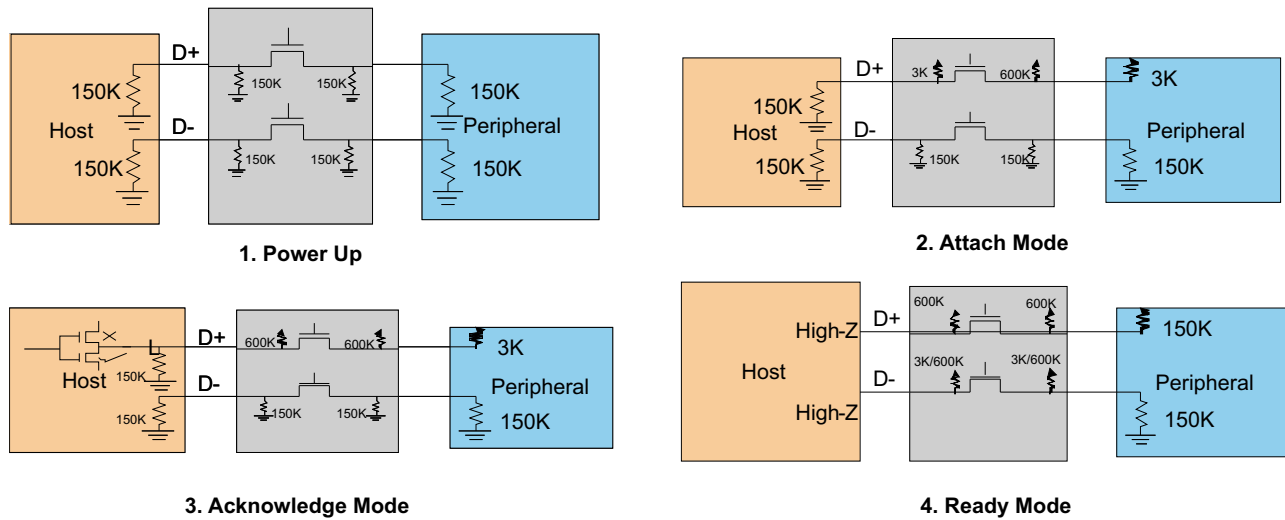


Figure 1. Block Diagram Showing Different Modes in the TXS0202

**ELECTRICAL CHARACTERISTICS**

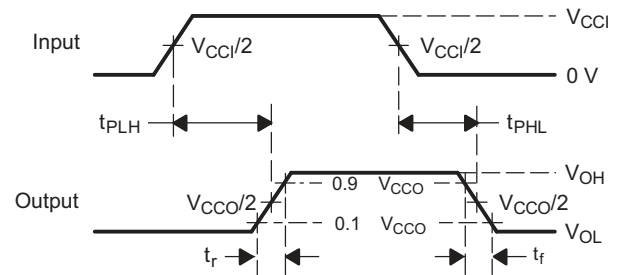
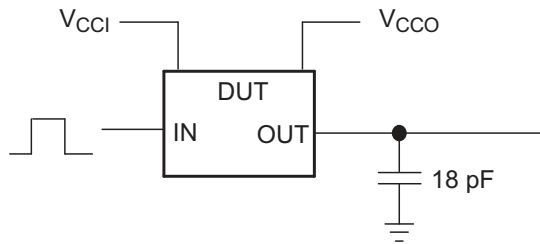
PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCBx</sub>	T <sub>A</sub> = 25°C	T <sub>A</sub> = -40°C to 85°C		UNIT
				TYP	MIN	MAX	
V <sub>OH(D-)</sub> (D- A or B port)	I <sub>OH</sub> = -20 μA, V <sub>Ix</sub> ≥ V <sub>CCx</sub> - 0.2 V	1.65 V	1.65 V		V <sub>CCO</sub> × 0.67		V
		2.3 V	2.3 V		V <sub>CCO</sub> × 0.67		
		3.3 V	3.3 V		V <sub>CCO</sub> × 0.67		
V <sub>OL(D-)</sub> (D- A or B port)	I <sub>OL</sub> = 220 μA, V <sub>Ix</sub> ≤ 0.15 V	1.65 V	1.65 V		0.45		V
		2.3 V	2.3 V		0.55		
		3.3 V	3.3 V		0.7		
V <sub>OH(D+)</sub> (D+ A or B port)	I <sub>OH</sub> = -20 μA, V <sub>Ix</sub> ≥ V <sub>CCx</sub> - 0.2 V	1.65 V	1.65 V		V <sub>CCO</sub> × 0.67		V
		2.3 V	2.3 V		V <sub>CCO</sub> × 0.67		
		3.3 V	3.3 V		V <sub>CCO</sub> × 0.67		
V <sub>OL(D+)</sub> (D- A or B port)	I <sub>OL</sub> = 220 μA, V <sub>Ix</sub> ≤ 0.15 V	1.65 V	1.65 V		0.45		V
		2.3 V	2.3 V		0.55		
		3.3 V	3.3 V		0.7		
I <sub>I</sub>	OE	1.65 V to 3.6 V	1.65 V to 3.6 V	±2	±2		μA
	D-/D+ A or B port, OE = OPEN			±2	±2		
	I <sub>BOFF</sub> , D+, D- B port	1.65 V to 3.6 V	0 V		±2		
	I <sub>AOFF</sub> , D+, D- A port	0 V	1.65 V to 3.6 V		±2		
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>O</sub> = Open, OE = High	1.65 V to 3.6 V	1.65 V to 3.6 V	2.2	12		μA
		3.6 V	0 V	2.3	12		
		0 V	3.6 V	0.026	-1		
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>O</sub> = Open, OE = High	1.65 V to 3.6 V	1.65 V to 3.6 V	2.7	24		μA
		3.6 V	0 V	0.031	-12		
		0 V	3.6 V	2.7	24		
C <sub>i</sub>	OE	3.6 V	3.6 V	2.5	3.5		pF
C <sub>io</sub>	A port	3.6 V	3.6 V	7	7.5		pF
	B port			9.5	10		

### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	UNIT
			TYP	TYP	
$t_{pd}$	A	B	5	5	ns
	B	A	5	5	
$t_{rA}$	A port rise times		2	2	ns
$t_{fA}$	A port fall times		2	2	ns
$t_{rB}$	B port rise times		2	2	ns
$t_{fB}$	B port fall times		2	2	ns
$t_{sk(o)}$	Channel-to-channel		0.5	0.5	ns
Max data rate			15	15	Mbps

### PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

DATA RATE, SKEW, PROPAGATION DELAY,  
OUTPUT RISE AND FALL TIME MEASUREMENT

- A.  $C_L$  includes probe and jig capacitance.
- B. The outputs are measured one at a time, with one transition per measurement.
- C.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0202YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7P	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

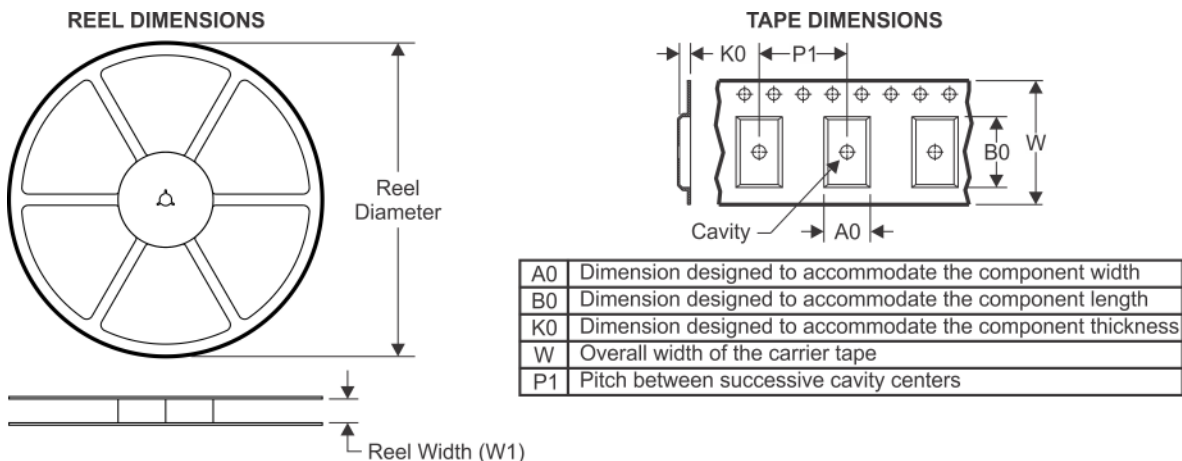
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

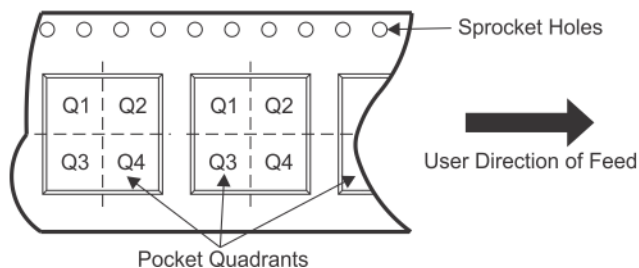
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0202YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0202YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

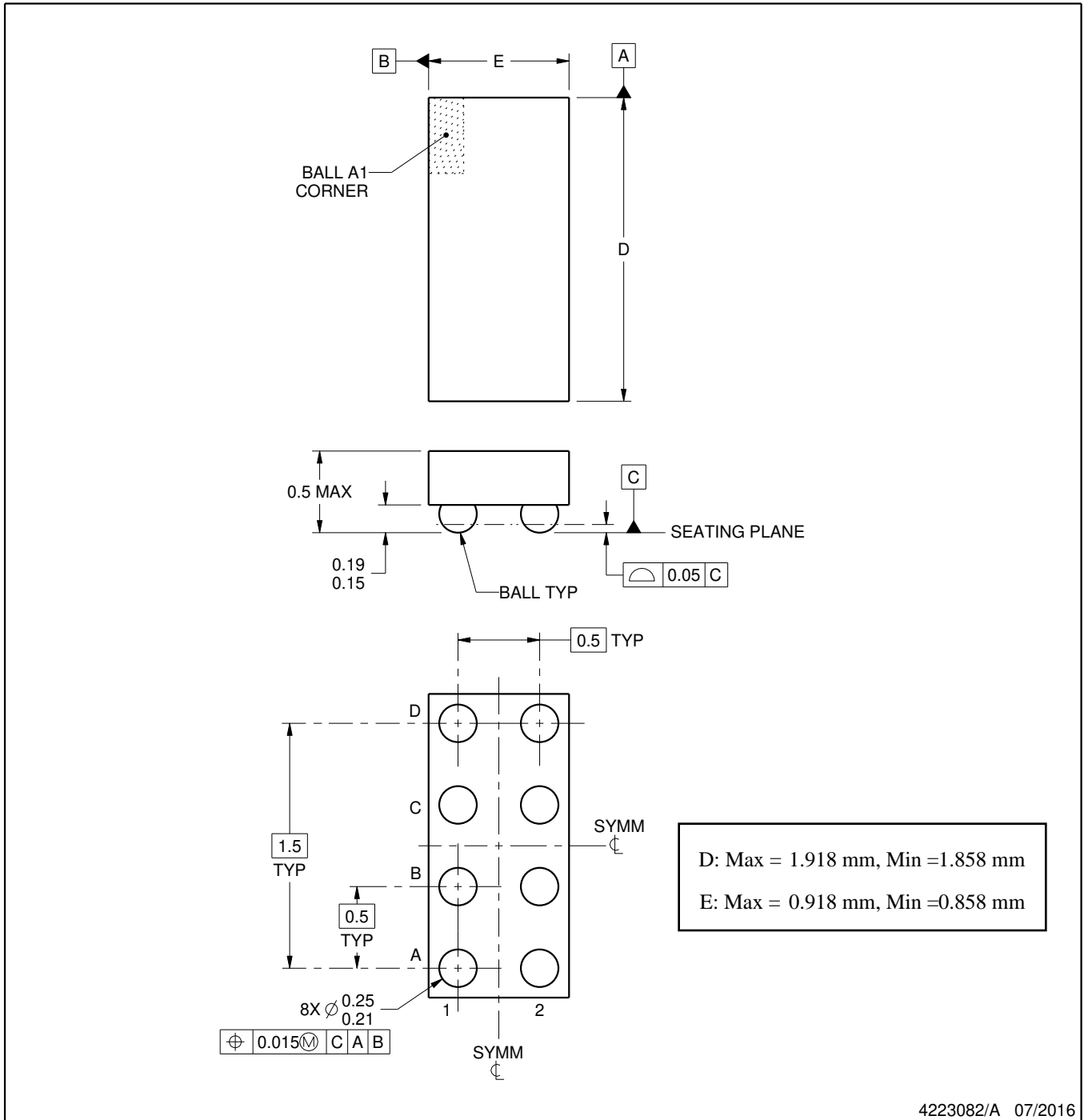
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

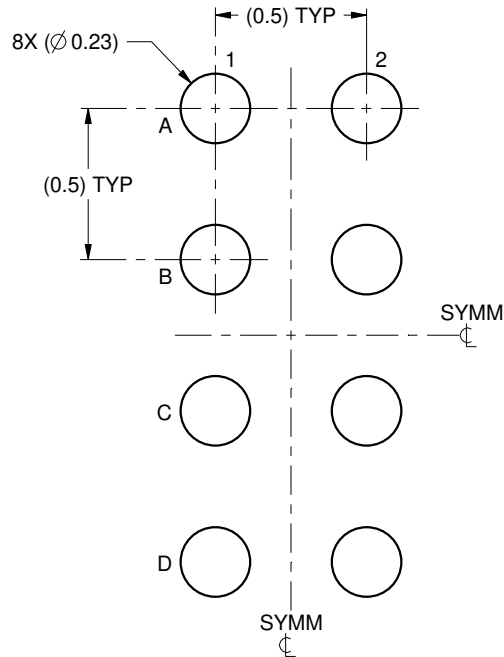
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

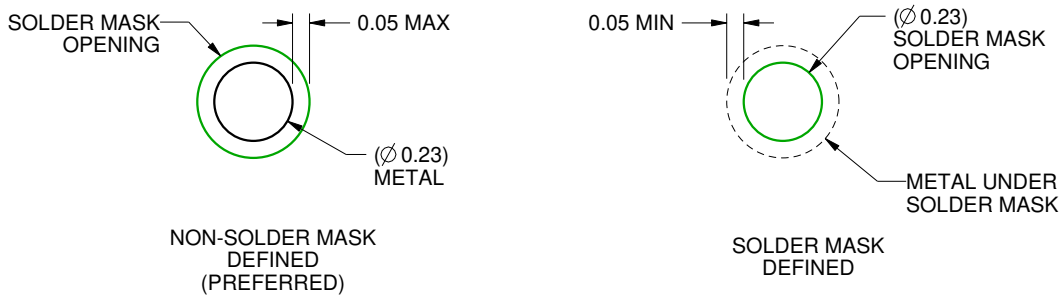
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

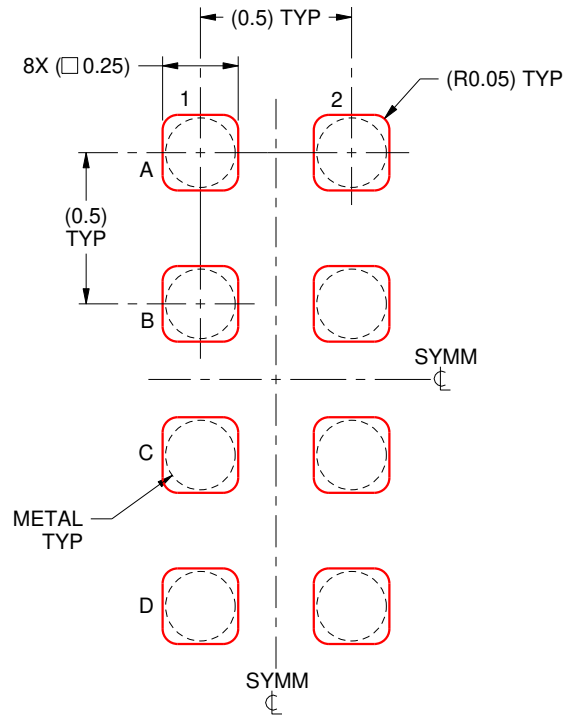
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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