TLV6713 Micropower, 36-V Comparator With 400-mV Reference

1 Features

- High Supply Voltage Range: 1.8 V to 36 V
- Adjustable Threshold: Down to 400 mV
- High Threshold Accuracy:
  - 0.25% (Typ)
  - 0.75% Max Over Temperature
- Low Quiescent Current: 7 µA (Typ)
- Open-Drain Output
- Internal Hysteresis: 5.5 mV (Typ)
- Temperature Range: –40°C to +125°C
- Package: Thin SOT-23-6

2 Applications

- Notebook PCs and Tablets
- Smartphones
- Digital Cameras
- Video Game Controllers
- Relays and Circuit Breakers
- Portable Medical Devices
- Door and Window Sensors
- Portable- and Battery-Powered Products

3 Description

The TLV6713 high voltage comparator operates over a 1.8-V to 36-V range. The device has a precision comparator with an internal 400-mV reference and an open-drain output rated to 25 V for undervoltage detection. Set the monitored voltage with the use of external resistors.

OUT is driven low when the voltage at the SENSE pin drops below the negative threshold, and goes high when the voltage returns above the positive threshold. The comparator in the TLV6713 includes built-in hysteresis for noise rejection, thereby ensuring stable output operation without false triggering.

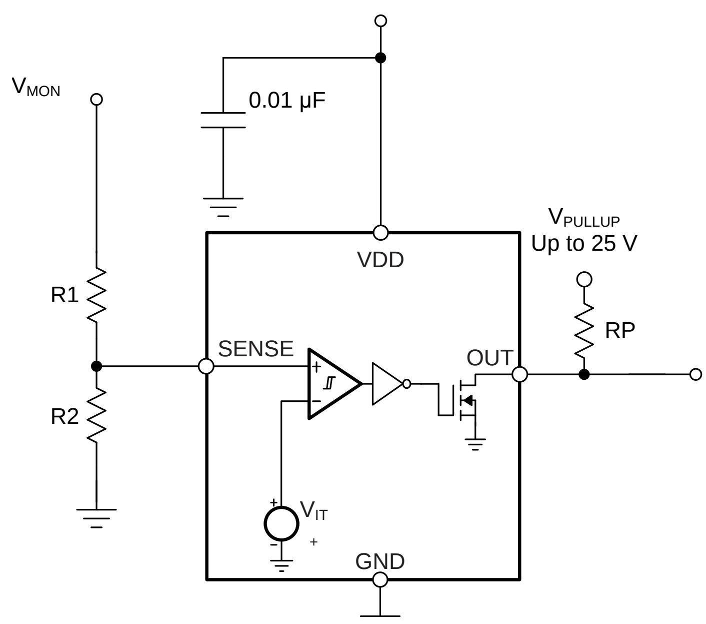
The TLV6713 is available in a Thin SOT-23-6 package and is specified over the junction temperature range of –40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV6713	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application



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4 Revision History

Changes from Revision A (April 2018) to Revision B — **Page**

- Changed Typical Application graphic pull-up resistor text from 36V to 25V 1

Changes from Original (January 2018) to Revision A — **Page**

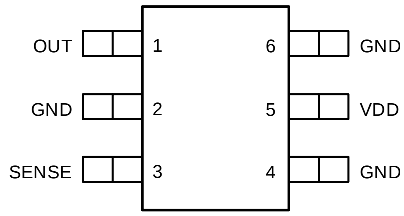
- Changed Advance Information to Production Data 1

5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
TLV6700	Window	1.8 V to 18 V	1%
TLV6703	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6710	Window	1.8 V to 36 V	0.75%
TLV6713	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2, 4, 6	—	Ground. Connect all three pins to ground.
OUT	1	O	Comparator open-drain output. This pin is driven low when the voltage at this comparator is less than V_{IT-}. The output goes high when the sense voltage rises above V_{IT+}.
SENSE	3	I	Comparator input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage V_{IT-}, OUT is driven low.
VDD	5	I	Supply-voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings[(1)]

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage [(2)]	V_{DD}	–0.3	40	V
	V_{OUT}	–0.3	28	
	V_{SENSE}	–0.3	7	
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–40	125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{SENSE}	Input pin voltage	0		1.7	V
V_{OUT}	Output pin voltage	0		25	V
V_{PULLUP}	Pullup voltage	0		25	V
I_{OUT}	Output pin current	0		10	mA
T_J	Junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC [(1)]		TLV6713 DDC (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V ≤ V_{DD} < 36 V, and pullup resistor RP = 100 kΩ (unless otherwise noted). Typical values are at T_J = 25°C and V_{DD} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} ≤ 0.2 V			0.8	V
V_{IT-}	SENSE pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
V_{IT+}	SENSE pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	400	405.5	413	mV
V_{HYS}	SENSE pin hysteresis voltage (HYS = V_{IT+} – V_{IT-})		2	5.5	12	mV
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, I_{OUT} = 3 mA		130	250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA		150	250	
I_{IN}	Input current (at SENSE pin)	V_{DD} = 1.8 V and 36 V, V_{SENSE} = 6.5 V	–25	+1	+25	nA
		V_{DD} = 1.8 V and 36 V, V_{SENSE} = 0.1 V	–15	+1	+15	
$I_{D(leak)}$	Open-drain leakage current	V_{DD} = 1.8 V and 36 V, V_{OUT} = 25 V		10	300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V – 36 V		8	11	µA
UVLO	Undervoltage lockout(2)	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. If less than $V_{(POR)}$, the output is undetermined.
(2) When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined if less than $V_{(POR)}$.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		9.9		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		28.1		µs
$t_{d(start)}$(2)	Startup delay	V_{DD} = 5 V		155		µs
t_r	Output rise time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.1 to 0.9) × V_{DD}		2.7		µs
t_f	Output fall time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.9 to 0.1) × V_{DD}		0.12		µs

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs (typical) before the output state reflects the input condition.

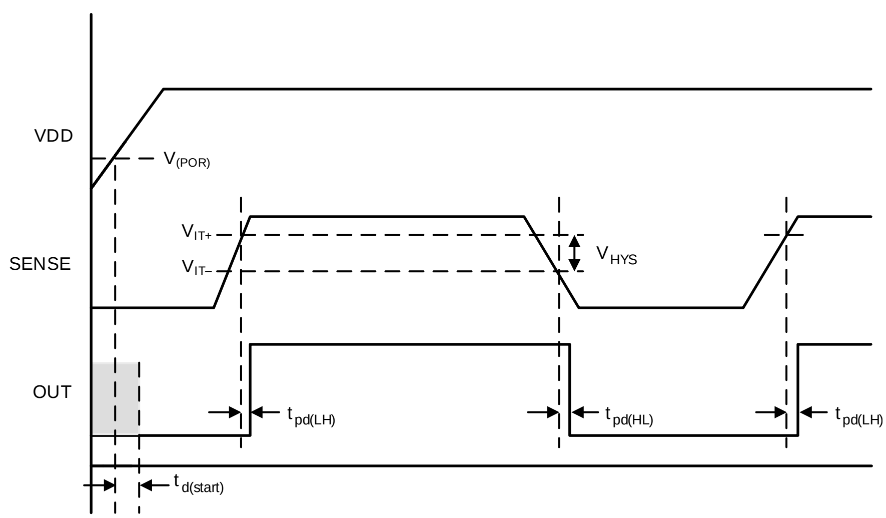


Figure 1. Timing Diagram

7.7 Typical Characteristics

at T_J = 25°C and V_{DD} = 12 V (unless otherwise noted)

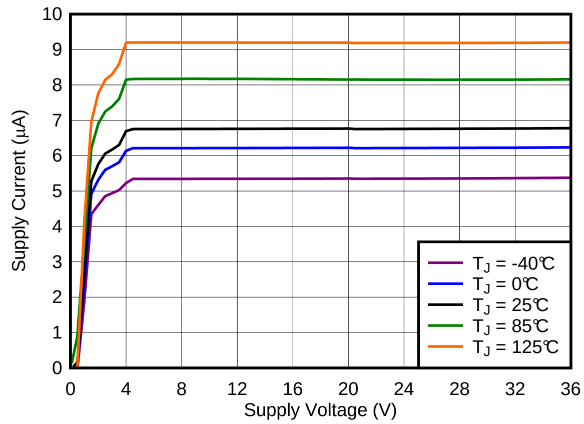
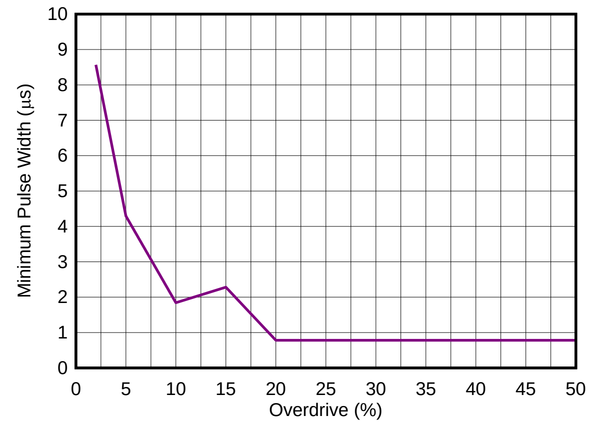


Figure 2. Supply Current vs Supply Voltage



V_{DD} = 24 V, minimum pulse duration required to trigger output high-to-low transition, SENSE = negative spike below V_{IT-}

Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage

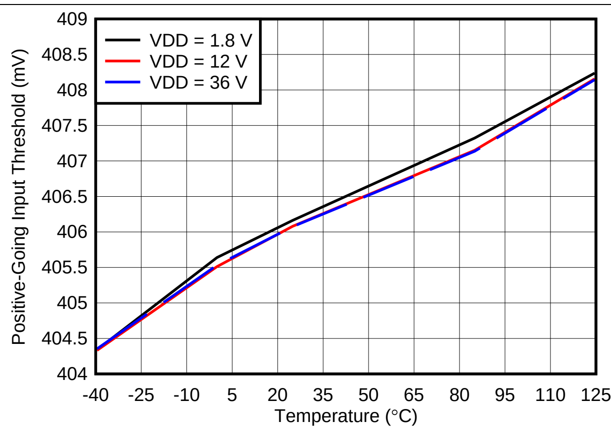


Figure 4. SENSE Positive Input Threshold Voltage (V_{IT+}) vs Temperature

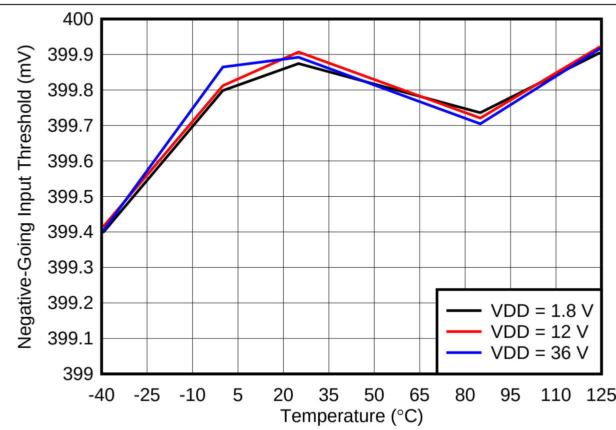
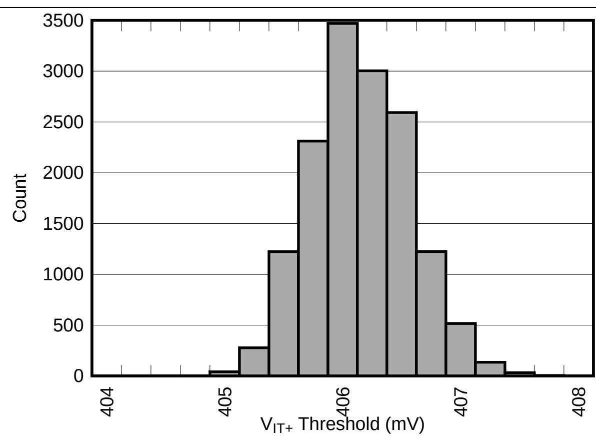
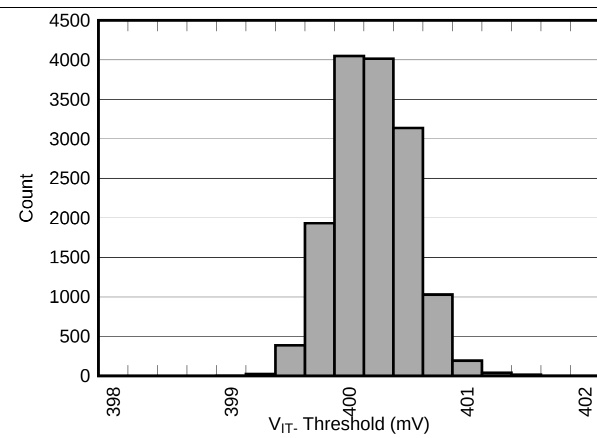


Figure 5. SENSE Negative Input Threshold Voltage ($V_{IT–}$) vs Temperature



V_{DD} = 1.8 V

Figure 6. SENSE Positive Input Threshold Voltage (V_{IT+}) Distribution

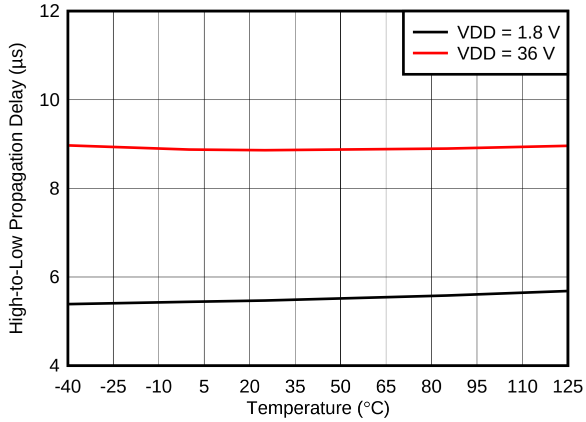


V_{DD} = 1.8 V

Figure 7. SENSE Negative Input Threshold Voltage ($V_{IT–}$) Distribution

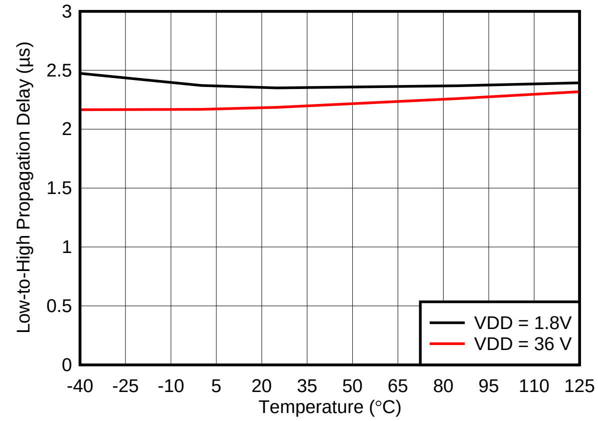
Typical Characteristics (continued)

at T_J = 25°C and V_{DD} = 12 V (unless otherwise noted)



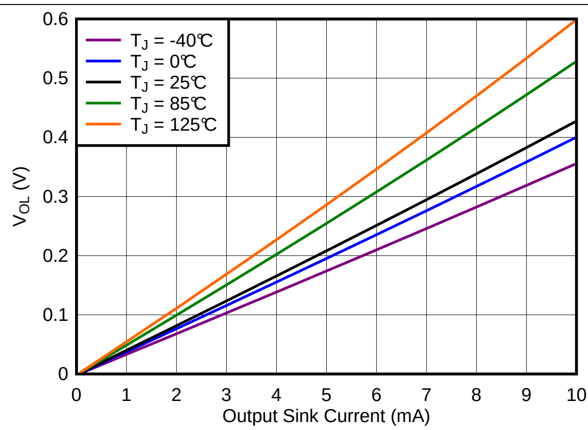
Input step ±200 mV

Figure 8. Propagation Delay vs Temperature (High-to-Low Transition at SENSE)



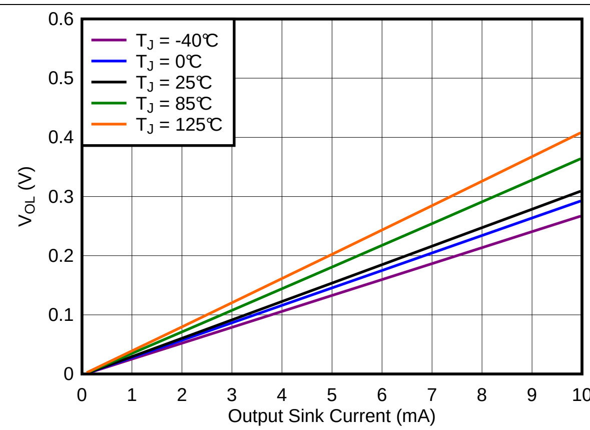
Input step ±200 mV

Figure 9. Propagation Delay vs Temperature (Low-to-High Transition at SENSE)



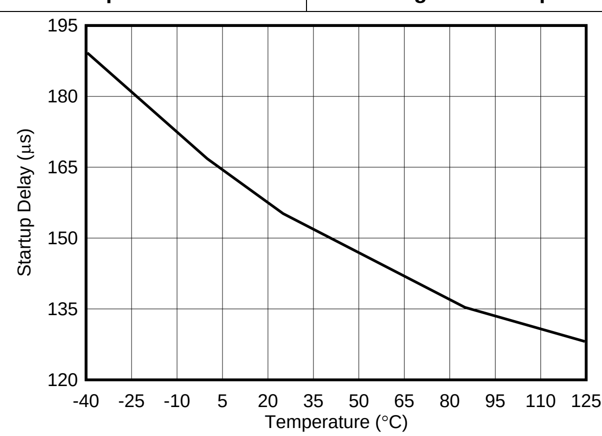
V_{DD} = 1.8 V

Figure 10. Output Voltage Low vs Output Sink Current



V_{DD} = 12 V

Figure 11. Output Voltage Low vs Output Sink Current



V_{DD} = 5 V

Figure 12. Start-up Delay vs Temperature

8 Detailed Description

8.1 Overview

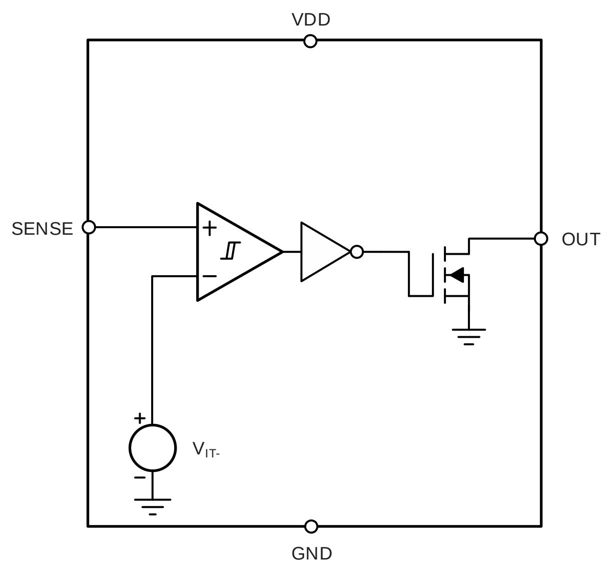
The TLV6713 combines a comparator and a precision reference for undervoltage detection. The TLV6713 features a wide supply voltage range (1.8 V to 36 V) and a high-accuracy threshold voltage of 400 mV (0.75% over temperature) with built-in hysteresis. The output is rated to 25 V and can sink up to 10 mA.

Set the input pin (SENSE) to monitor any voltage above 0.4 V by using an external resistor divider network. SENSE has very low input leakage current, allowing the use of a large resistor divider without sacrificing system accuracy. The relationship between the input and the output is shown in Table 2. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 2. Truth Table

CONDITION	OUTPUT	OUTPUT STATE
SENSE > V_{IT+}	OUT high	Output high impedance
SENSE < V_{IT-}	OUT low	Output sinking

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6713 combines a comparator with a precision reference voltage. The comparator has one external input and one internal input connected to the internal reference. The falling threshold on SENSE is designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy. The comparator also has built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator input swings from ground to 1.7 V (7 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications to reduce sensitivity to transient voltage changes on the monitored signal.

For the comparator, the output (OUT) is driven to logic low when the input SENSE voltage drops below V_{IT-}. When the voltage exceeds V_{IT+}, OUT goes to a high-impedance state; see Figure 1.

8.3.2 Output Pin (OUT)

In a typical TLV6713 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6713 provides an open-drain output (OUT) rated to 25 V, independant of supply voltage, and can sink up to 40 mA.. A pullup resistor is required to hold the line high when the output goes to a high-impedance state. Connect this pullup resistor to a voltage rail that meets the logic requirements of the downstream device. To ensure the proper voltage level, give some consideration when choosing the pullup resistor value. The pullup resistor value is determined by V_{OL}, output capacitive loading, and the open-drain leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table.

Table 2 and *Input Pin (SENSE)* describe how the output is asserted or high impedance. See Figure 1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUT signal corresponds to the voltage on SENSE, as listed in Table 2.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD}$ < UVLO)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), OUT is in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6713 is used as a precision voltage supervisor in several different configurations. The monitored voltage (V_{MON}), VDD voltage, and output pullup voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

9.1.1 Input and Output Configurations

Figure 13 and Figure 14 show examples of the various input and output configurations.

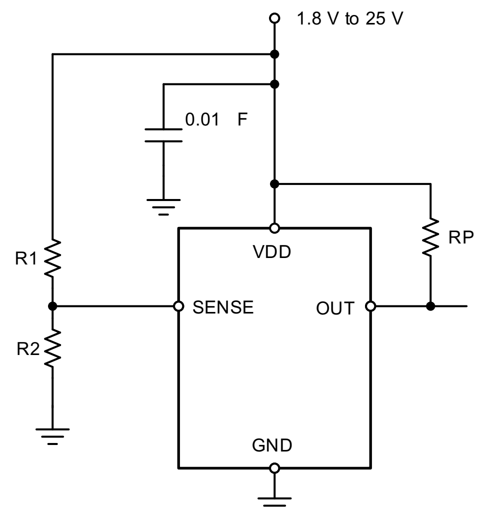
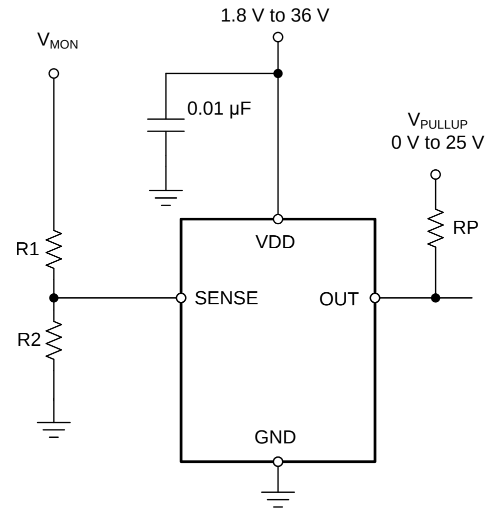


Figure 13. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The input can monitor a voltage higher than V_{DD} (maximum) with the use of an external resistor divider network.

Figure 14. Monitoring a Voltage Other than V_{DD}

9.1.2 Immunity to Input Pin Voltage Transients

The TLV6713 is immune to short voltage transient spikes on the input pin. Sensitivity to transients depends on both transient duration and amplitude; see Figure 3, *Minimum Pulse Duration vs Threshold Overdrive Voltage*.

9.2 Typical Application

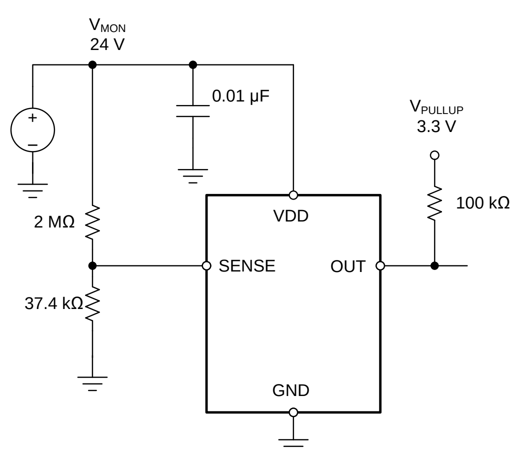


Figure 15. 24-V, 10% Comparator

Typical Application (continued)

9.2.1 Design Requirements

This typical voltage detector application is designed to meet the parameters listed in Table 3:

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, falling ($V_{MON(UV)}$) threshold 10% nominal (21.6 V)	$V_{MON(UV)}$ = 21.8 V ±2.7%
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 µA	24 µA

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-}$$

where

- R1 and R2 are the resistor values for the resistor divider onthe SENSE pin
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected (1)

Choose an R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. Use resistors with high values to minimize current consumption (as a result of low input bias current) without adding significant error to the resistive divider. For details on sizing input resistors, refer to *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

9.2.2.2 Pullup Resistor Selection

To ensure the proper logic-high voltage level (V_{HI}), select a pullup resistor value where the pullup voltage divided by the pullup resistor value does not exceed the sink-current capability of the device. Confirm this voltage level by verifying that the pullup voltage minus the open-drain leakage current ($I_{D(leak)}$) multiplied by the resistor is greater than the desired V_{HI}. These values are specified in the *Electrical Characteristics*.

Use Equation 2 to calculate the value of the pullup resistor.

$$\frac{V_{HI} - V_{pullup}}{I_{D(leak)}} \leq RP \leq \frac{V_{pullup}}{I_{OUT}} \quad (2)$$

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1-µF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.3 Application Curve

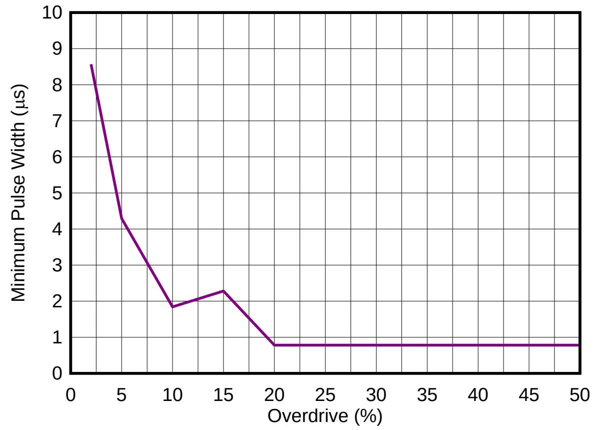


Figure 16. 24-V Window Monitor Output Response

10 Power Supply Recommendations

The TLV6713 has a 40-V absolute maximum rating on the VDD pin, with a recommended maximum operating condition of 36 V. If the voltage supply that provides power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, then place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. In these cases, a 100-Ω resistor and 0.01-µF capacitor are required, as shown in Figure 17.

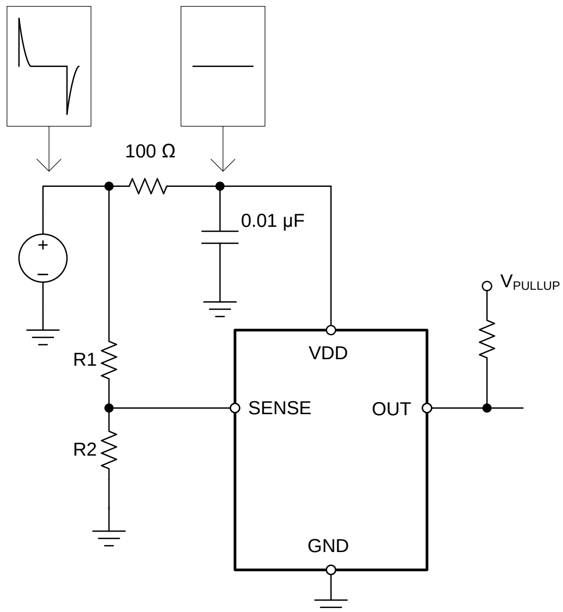


Figure 17. Using a RC Filter to Remove High-Frequency Disturbances on V_{DD}

11 Layout

11.1 Layout Guidelines

- Place R2 and R2 close to the device to minimize noise coupling into the SENSE node.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, might form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If long traces are unavoidable, see Figure 17 for an example of filtering VDD.

11.2 Layout Example

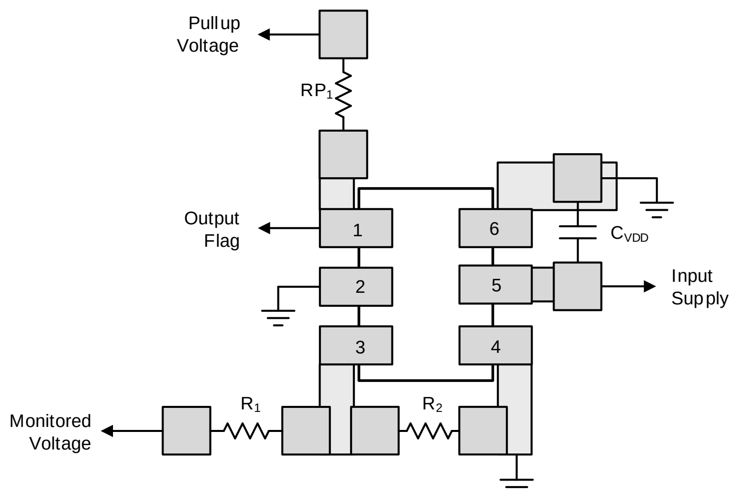


Figure 18. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

The *DIP Adapter Evaluation Module* allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6713DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1	Samples
TLV6713DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

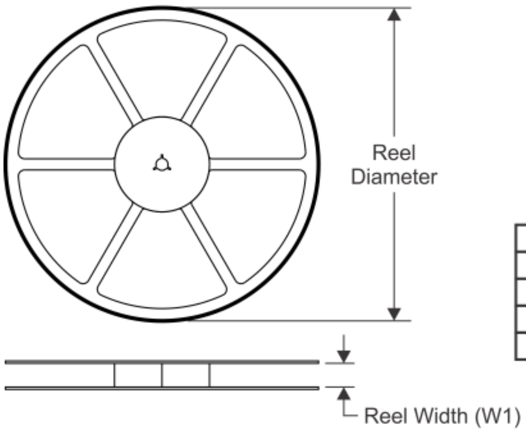
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

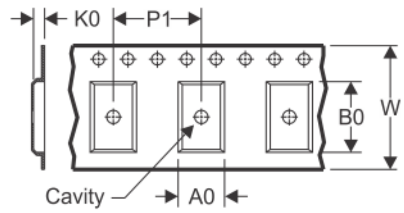
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

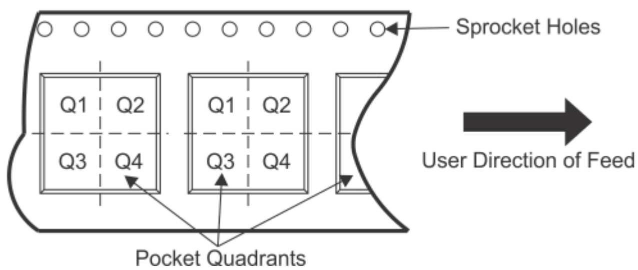


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

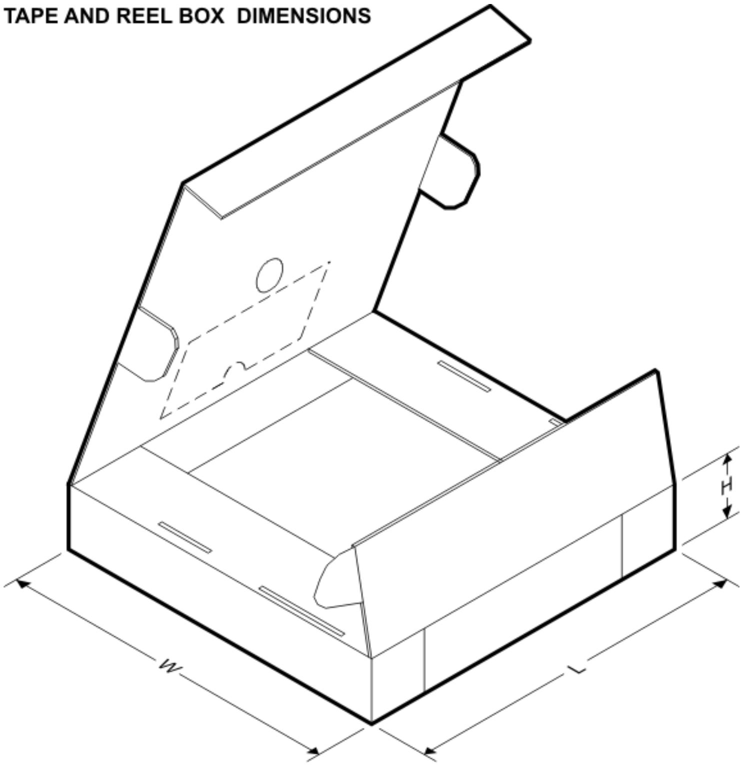
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6713DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6713DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



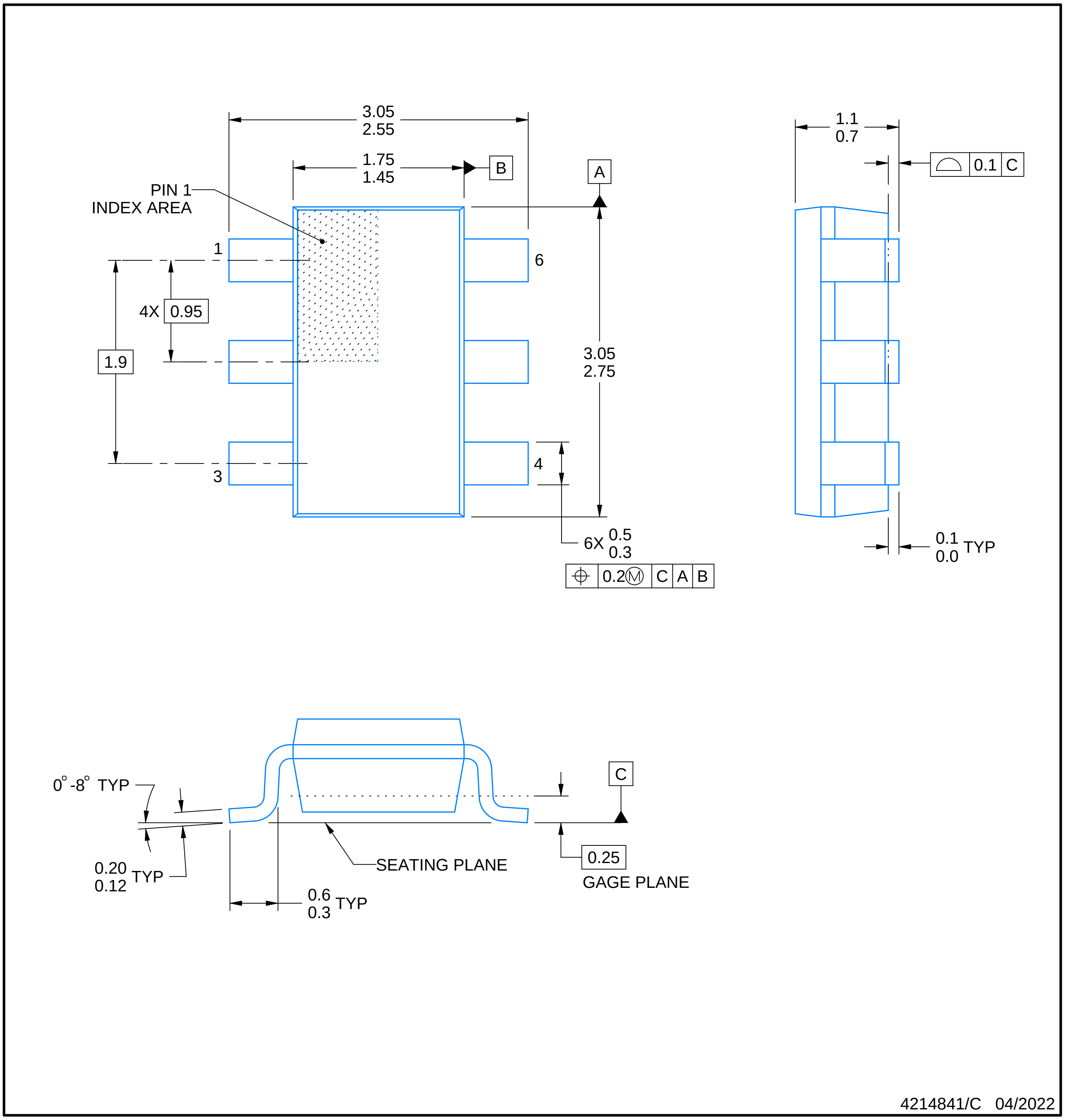
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6713DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6713DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

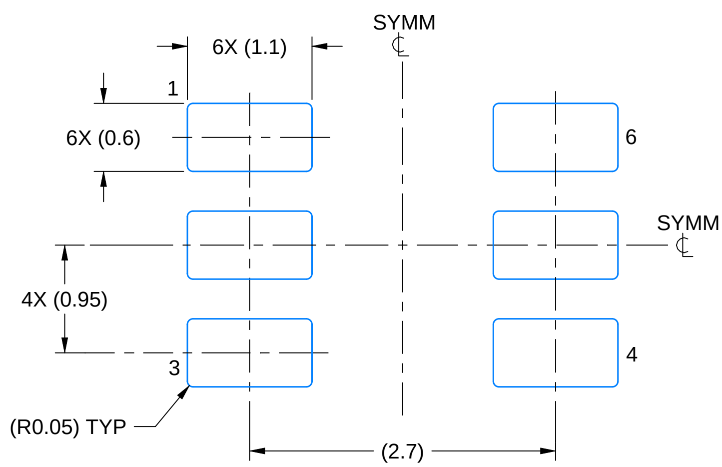
SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

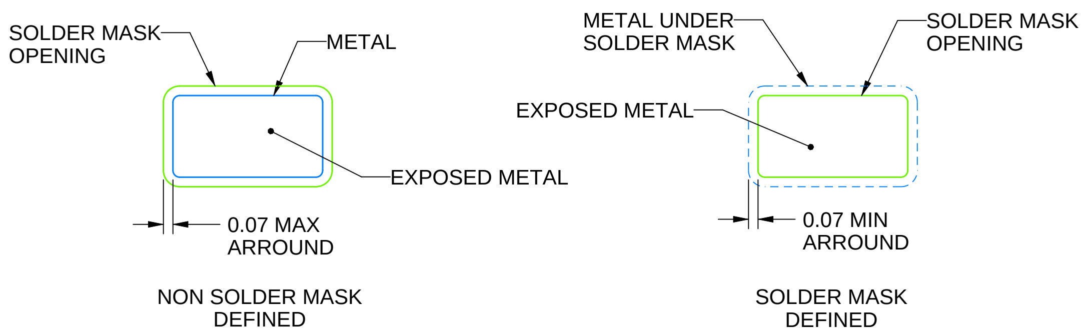


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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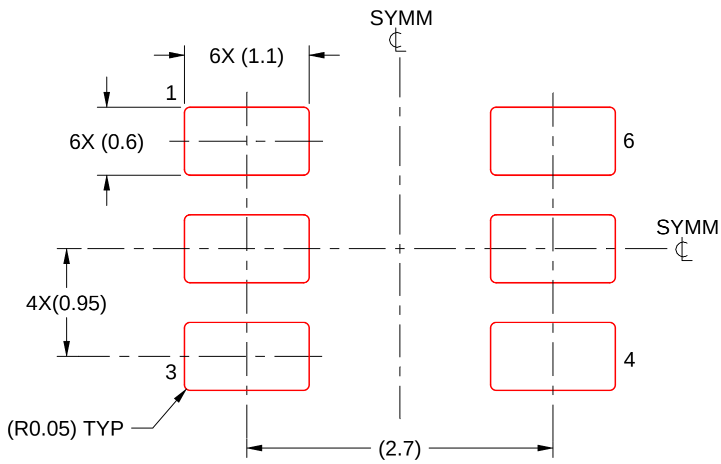
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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