ISL6455EVAL1Z: 600mA Synchronous Buck Regulator with Integrated MOSFETs

Application Note | **May 23, 2007** | **AN1327.0**

The ISL6455 is a highly integrated triple output regulator which provides a single chip solution for FPGAs and wireless chipset power management. The device integrates a high efficiency synchronous buck regulator (adjustable) with two ultra low noise LDO regulators (adjustable). Either the ISL6455 or ISL6455A can be selected based on whether 3.3V ±10% or 5V ±10% is required as an input voltage.

The synchronous current mode control PWM regulator with integrated N-Channel and P-Channel power MOSFET provides adjustable voltages based on external resistor setting. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The ISL6455 also has two LDO adjustable regulators using internal PMOS transistors as pass devices. LDO2 features ultra low noise typically below $30\mu V_{RMS}$ to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6455 also integrates a $\overline{\text{RESET}}$ function, which eliminates the need for additional RESET IC required in WLAN and other applications. The IC asserts a $\overline{\text{RESET}}$ signal whenever the V_{IN} supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after V_{IN} has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include overcurrent protection and thermal shutdown for all the three outputs.

High integration and the thin Quad Flat No-lead (QFN) package makes ISL6455 an ideal choice for powering FPGAs and small form factor wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

Ordering Information

PART NUMBER* (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6455IRZ	64 55IRZ	-40 to +85	24 Ld QFN 4x4	L24.4x4B
ISL6455AIRZ	64 55AIRZ	-40 to +85	24 Ld QFN 4x4	L24.4x4B

*Add “-TK” or T5K suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Fully integrated synchronous buck regulator + dual LDO
- PWM output voltage adjustable.
  - 0.8V to 2.5V with ISL6455 (V_{IN} = 3.3V)
  - 0.8V to 3.3V with ISL6455A (V_{IN} = 5.0V)
- High output current. 600mA
- Dual LDO adjustable options
  - LDO1, 1.2V to V_{IN} - 0.3V ($3.3V_{MAX}$) 300mA
  - LDO2, 1.2V to V_{IN} - 0.3V ($3.3V_{MAX}$) 300mA
- Ultra-compact DC/DC converter design
- Stable with small ceramic output capacitors and no load
- High conversion efficiency
- Low shutdown supply current
- Low dropout voltage for LDOs
  - LDO1 . . . . . 150mV (typical) at 300mA
  - LDO2 . . . . . 150mV (typical) at 300mA
- Low output voltage noise
  - $<30\mu V_{RMS}$ (typical) for LDO2 (VCO supply)
- PG_LDO and PG_PWM (PWM and LDO) outputs
- Extensive circuit protection and monitoring features
  - PWM overvoltage protection
  - Overcurrent protection
  - Shutdown
  - Thermal shutdown
- Integrated $\overline{\text{RESET}}$ output for microprocessor reset
- Proven reference design for total WLAN system solution
- QFN package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale package footprint Improves PCB efficiency and is thinner in Profile
- Pb-free plus anneal available (RoHS compliant)

Applications

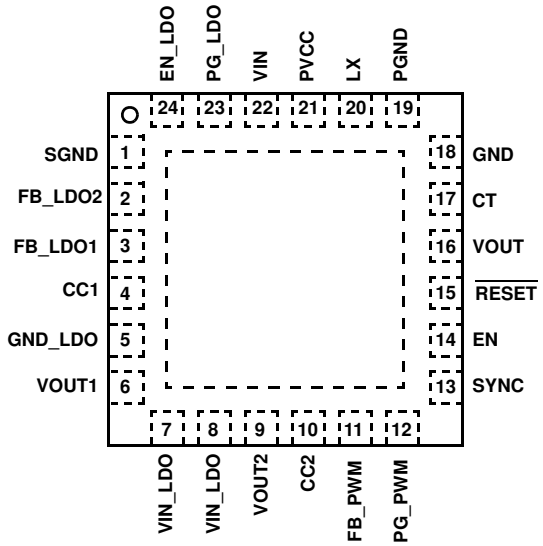
- WLAN cards
  - PCMCIA, Cardbus32, MiniPCI cards
  - Compact flash cards
- Hand-held instruments

Related Literature

- TB363 - Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)
- TB389 - PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

Pinout

ISL6455, ISL6455A
(24 LD QFN)
TOP VIEW



What's Inside

The Evaluation Board Kit contains the following materials:

- The ISL6455 EVAL REVD board
- The ISL6455 datasheet
- This EVAL KIT document

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 15V power supply with at least 5A source current capability, battery, notebook AC adapter
- Two Electronic Loads capable of sinking current up to 5A
- Digital Multimeters (DMMs)
- 100MHz quad-trace Oscilloscope
- Signal generator

Quick Setup Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to V_{IN} the plus terminal to J1(V_{IN}) and the negative return to J2(GND).
3. Turn on the power supply. For the ISL6455, the input voltage should be 3.3V. For the ISL6455A, the input voltage should be 5V.
4. Verify the outputs voltages for ISL6455 are 2.5V for V_{OUT}, 1.8V for V_{OUT1}, and 1.2V for V_{OUT2}.
5. Verify the ouputs voltages for ISL6455A are 3.3V for V_{OUT}, 2.5V for V_{OUT1}, and 1.2V for V_{OUT2}.

Evaluating the Other Output Voltage

The ISL6455 EVAL kit outputs are preset to V_{OUT} = 2.5V; V_{OUT1} = 1.8V, and V_{OUT2} = 1.2V. The ISL6455A EVAL kit outputs are preset to V_{OUT} = 3.3V; V_{OUT1} = 2.5V and V_{OUT2} = 1.2V. Output voltages can be adjusted from 0.8V to 2.5V with ISL6455 (V_{IN} = 3.3V), and from 0.8V to 3.3V with ISL6455A (V_{IN} = 5V) using the following equations:

$$V_{OUT} = \frac{0.45}{R_2}(R_1 + R_2) \quad \text{(EQ. 1)}$$

$$V_{OUT1} = \frac{1.184}{R_6}(R_5 + R_6) \quad \text{(EQ. 2)}$$

$$V_{OUT2} = \frac{1.184}{R_4}(R_3 + R_4) \quad \text{(EQ. 3)}$$

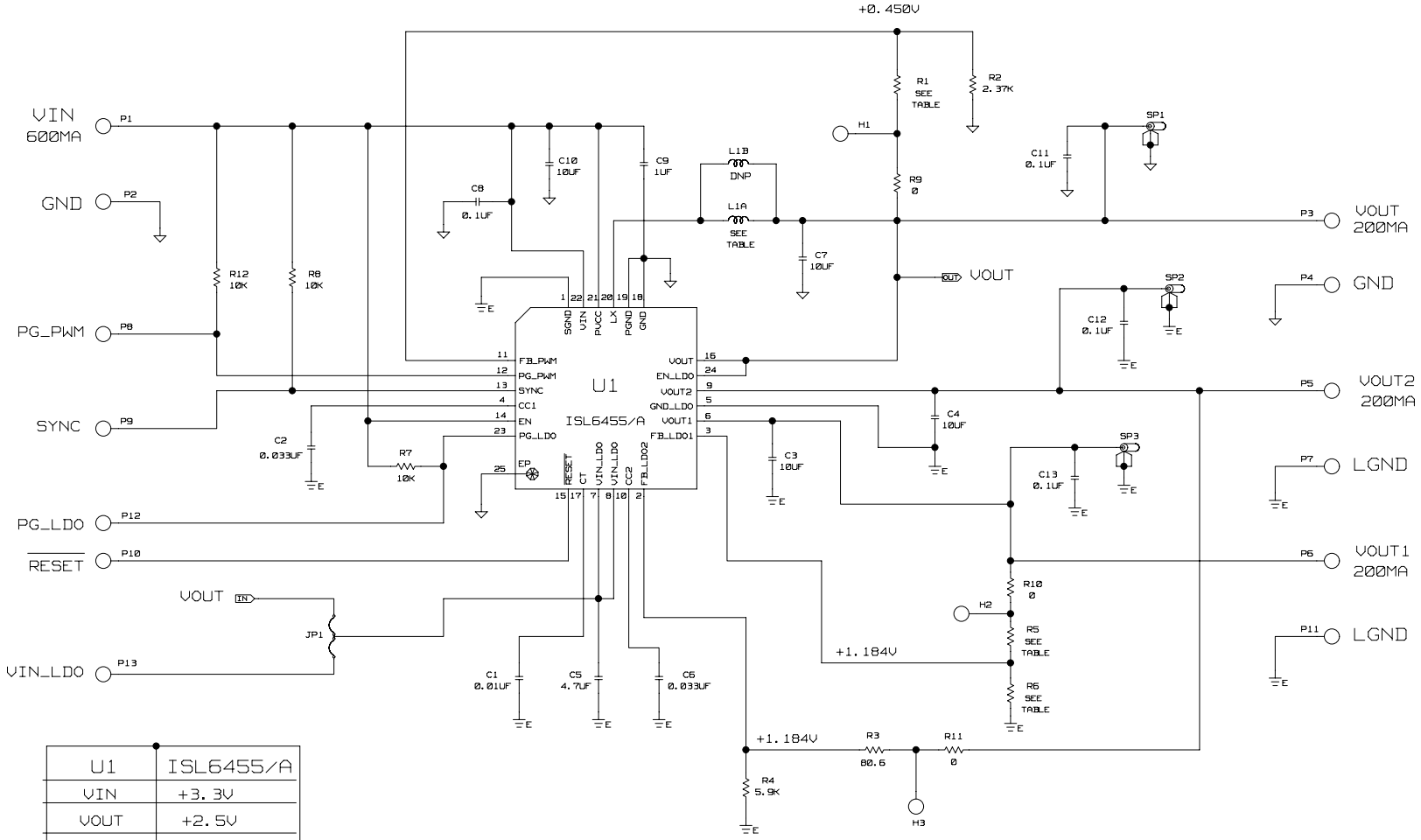
Frequency

The ISL6455EVAL1Z and ISL6455AEVAL1Z can operate at a switching frequency of 750kHZ, however, the switching frequency can adjust from 500kHz to1MHz by using the sync pin (P9).

TABLE 1. SWITCH 1 SETTINGS

J1	VIN_LDO	
1	Center post to right	Connect VIN_LDO to VOUT
2	Center post to left	Connect VIN_LDO to P13

Schematic



U1	ISL6455/A
VIN	+3.3V
VOUT	+2.5V
VOUT1	+1.8V
VOUT2	+1.2V
L1A	8.2UH
R1	11K
R5	2.94K
R6	5.62K

TABLE 2. COMPONENT LIST ISL6455EVAL1Z, ISL6455AEVAL1Z

REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	PART NUMBER	MANUFACTURER	DESCRIPTION
C1	1	0.01µF	10%	25V	0603	06032R103K8B20	PHILLIPS	CAP, SMD, 0603, 0.01µF, 25V, 10%, X7R, ROHS
C8, C11-C13	4	0.1µF	10%	16V	0603	GRM39X7R104K016AD	MURATA	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS
C9	1	1µF	20%	16V	0603	GRM188R61C105KA12D	MURATA	CAP, SMD, 0603, 1µF, 16V, 20%, Y5V, ROHS
C2, C6	2	33000pF	10%	16V	0603	C0603X7R160-333KNE	VENKEL	CAP, SMD, 0603, 33000pF, 16V, 10%, X7R, ROHS
C3, C4, C7	3	10µF	10%	6.3V	0805	C0805X5R6R3-106KNE	VENKEL	CAP, SMD, 0805, 10µF, 6.3V, 10%, X5R, ROHS
C5	1	4.7V	10%	10V	0805	0805ZD475KAT2	AVX	CAP, SMD, 0805, 4.7µF, 10V, 10%, X5R, ROHS
C10	1	10µf	10%	10V	1206	C1206X7R100-106KNE	VENKEL	CAP, SMD, 1206, 10µF, 10V, 10%, X7R, ROHS
L1A	1	8.2µH	20%		6mmx6mm	MSS6122-822ML	COILCRAFT	COIL-PWR INDUCTOR, SMD, 6.1mm, 8.2µH, 20%, 1.25A, SHIELDED, ROHS
U1	1			3.3V to 5.5V	4x4	ISL6455IRZ ISL6455A EVAL1ZA use ISL6455AIRZ	INTERSIL	IC-3.3V TRIPLE OUTPUT REGULATOR, 24P, QFN, 4x4, ROHS
R9-R11	3	0Ω		100V	0603	ERJ-3GEY0R00V	PANASONIC	RES, SMD, 0603, 0Ω, 1/16W, TF, ROHS
R7, R8, R12	3	10k	1%	100V	0603	ERJ-3EKF1002V	PANASONIC	RES, SMD, 0603, 10k, 1/16W, 1%, TF, ROHS
R1	1	11k	1%	100V	0603	CR0603-10W-1102FT	YAGEO	RESISTOR, SMD, 0603, 11K, 1/10W, 1%, TF, ROHS
R2	1	2.37k	1%	100V	0603	ERJ-3EKF2371V	PANASONIC	RES, SMD, 0603, 2.37k, 1/10W, 1%, TF, ROHS
R5	1	2.94k	1%	100V	0603	ERJ-3EKF2941V	PANASONIC	RES, SMD, 0603, 2.94k, 1/10W, 1%, TF, ROHS
R6	1	5.62k	1%	100V	0603	ERJ-3EKF5621V	PANASONIC	RES, SMD, 0603, 5.62k, 1/16W, 1%, TF, ROHS
R4	1	5.9k	1%	100V	0603	ERJ-3EKF5901V	PANASONIC	RES, SMD, 0603, 5.90k, 1/10W, 1%, TF, ROHS
R3	1	80.6Ω	1%	100V	0603	ERJ-3EKF80R6	PANASONIC	RES, SMD, 0603, 80.6Ω, 1/10W, 1%, TF, ROHS

ISL6455AEVAL1Z Board Layout

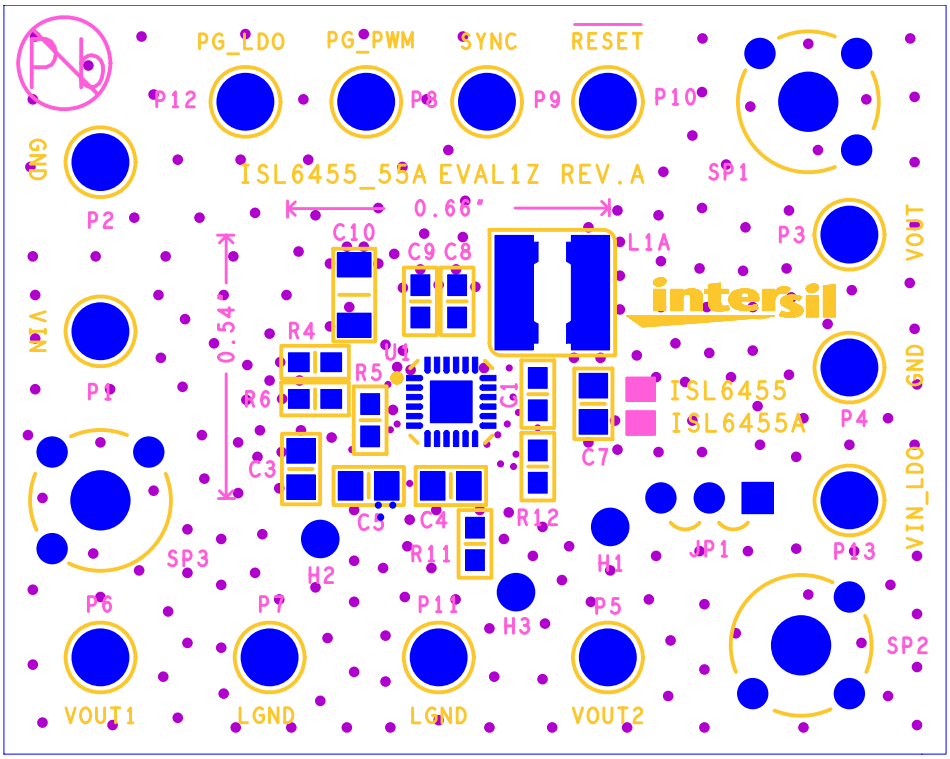


FIGURE 1. TOP COMPONENTS

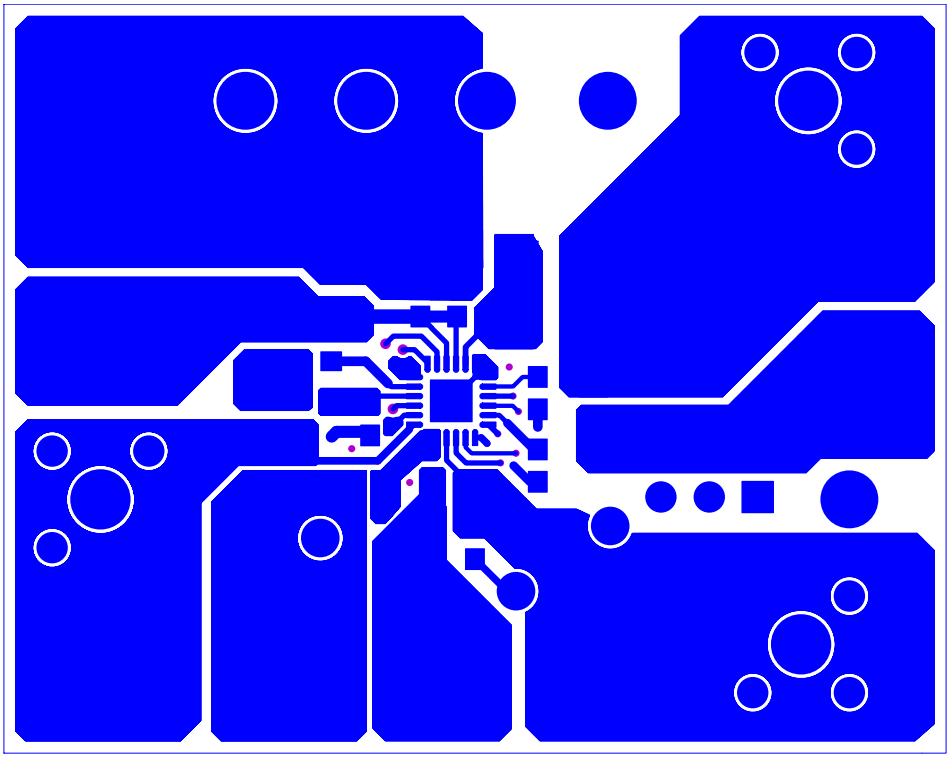


FIGURE 2. TOP LAYER ETCH

ISL6455AEVAL1Z Board Layout (Continued)

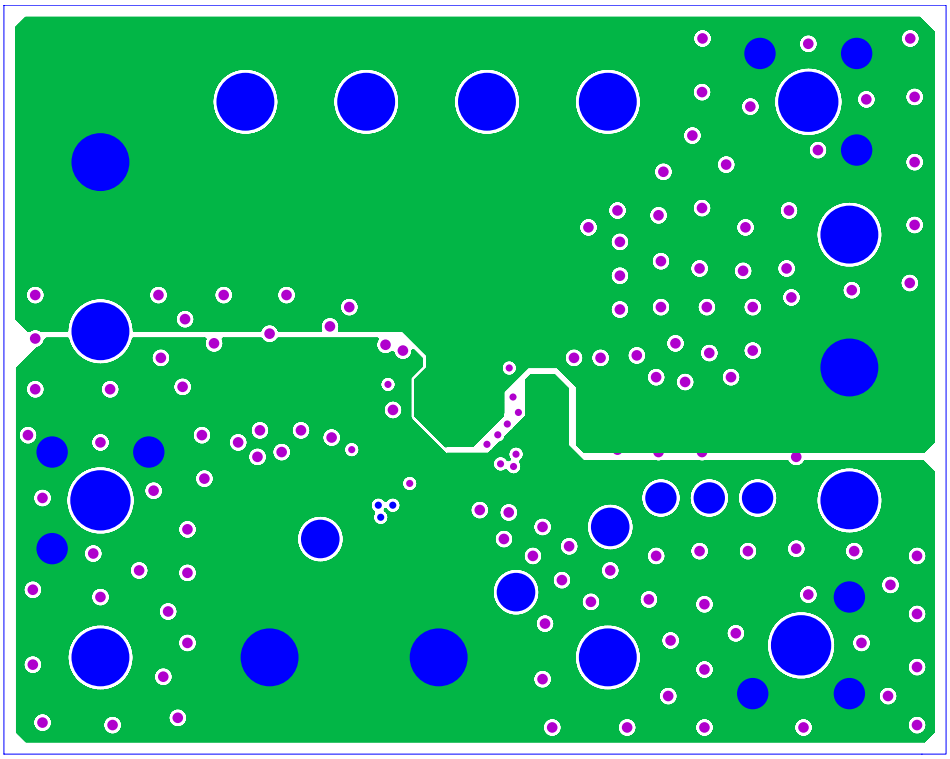


FIGURE 3. 2ND LAYER ETCH

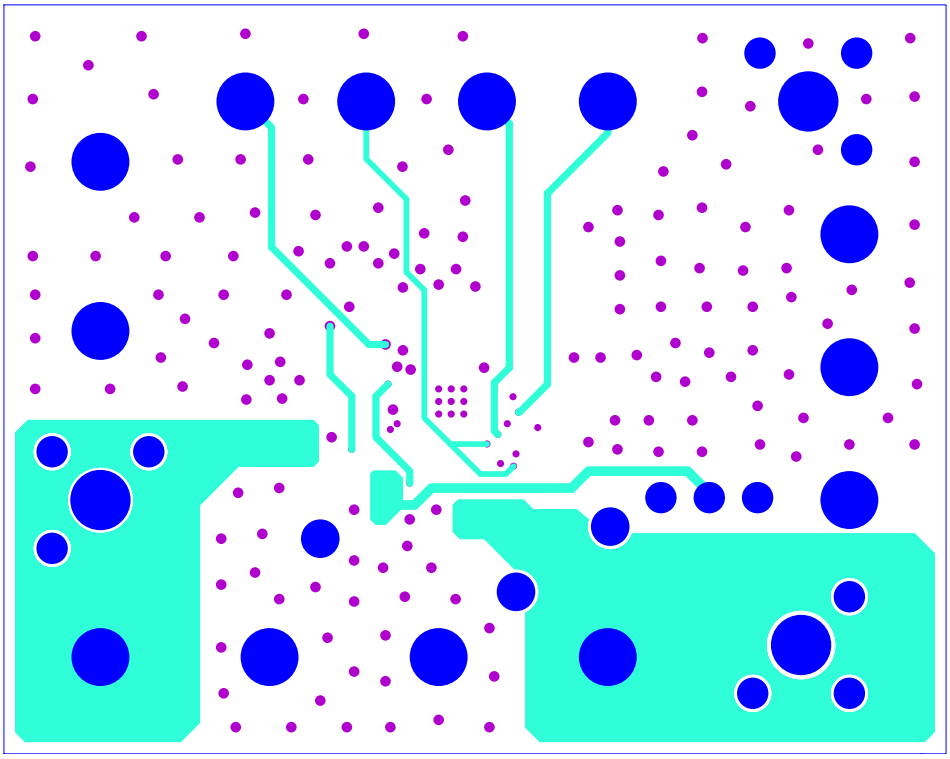


FIGURE 4. 3RD LAYER ETCH

ISL6455AEVAL1Z Board Layout (Continued)

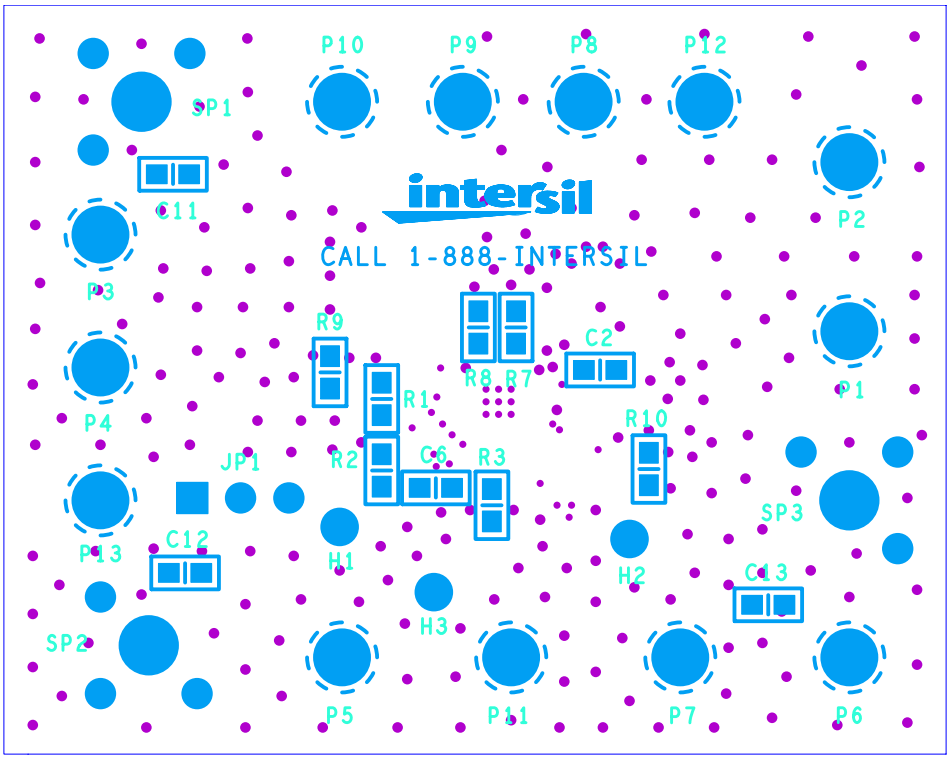


FIGURE 5. BOTTOM LAYER COMPONENTS (MIRRORED)

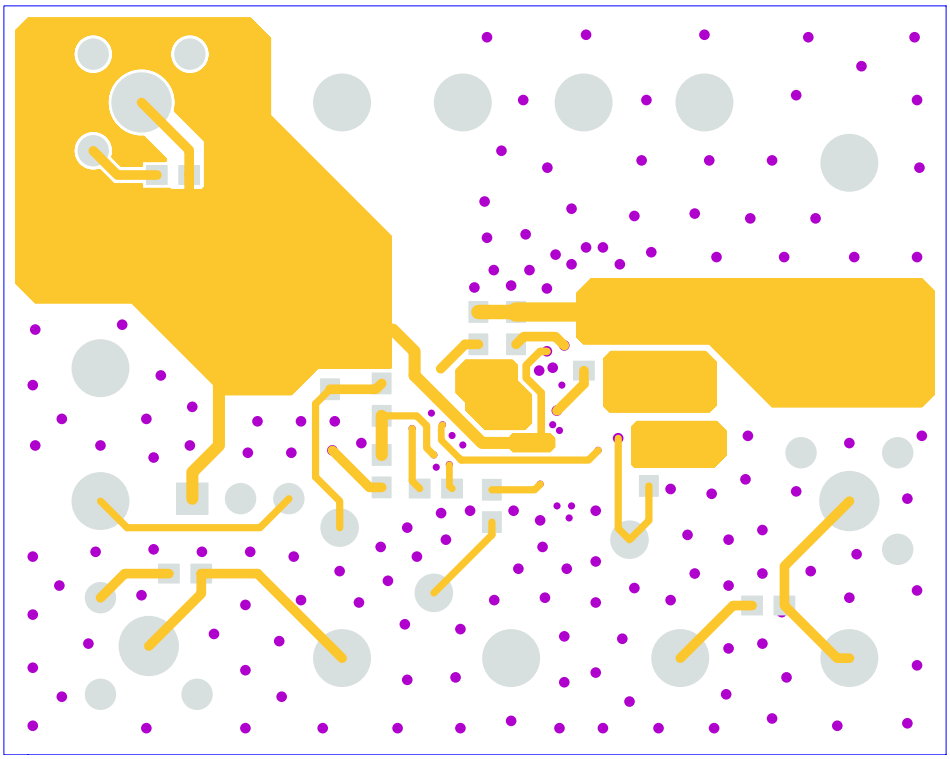


FIGURE 6. BOTTOM LAYER ETCH (MIRRORED)