

NP100P06PLG

-60V – -100A – P-channel Power MOS FET

Application : Automotive

R07DS1522EJ0100 Rev.1.00 Jun. 24, 2022

Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

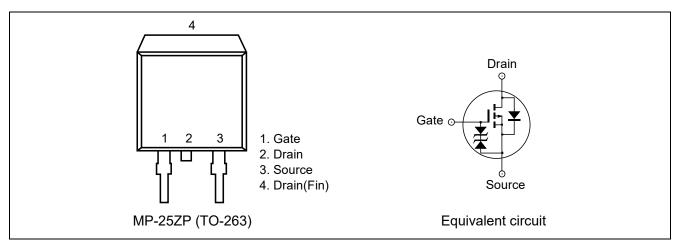
Features

• Super low on-state resistance : $R_{DS(on)}$ = 6.0 m Ω Max. (V_{GS} = -10 V, I_D = -50 A)

$$R_{DS(on)}$$
 = 7.8 m Ω Max. (V_{GS} = -4.5 V, I_D = -50 A)

- Low input capacitance : Ciss = 15000 pF Typ.
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



Absolute Maximum Ratings

			(Ta=25°C)
ltem	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 V$)	V _{DSS}	-60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	∓20	V
Drain Current (DC) $(T_c = 25 \degree C)$	I _{D(DC)}	∓100	A
Drain Current (pulse)	I _{D(pulse)} Notes1	∓300	А
Total Power Dissipation (T_c = 25 °C)	P _{T1}	200	W
Total Power Dissipation ($T_a = 25 \text{ °C}$)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to 175	°C
Single Avalanche Current	I _{AS} ^{Notes2}	64	A
Single Avalanche Energy	E _{AS} ^{Notes2}	420	mJ

Notes 1. PW \leq 10 μ s , Duty Cycle \leq 1%

2. Starting T_ch=25 $^\circ\!\mathrm{C}$, V_DD = -30V , R_G = 25 Ω , V_Gs = -20 \rightarrow 0V , L = 100 $\mu\mathrm{H}$



Thermal Resistance

Channel to Case Thermal Resistance	Rth(ch-c) Notes3	0.75	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ Notes3	83.3	°C/W

Electrical Characteristics

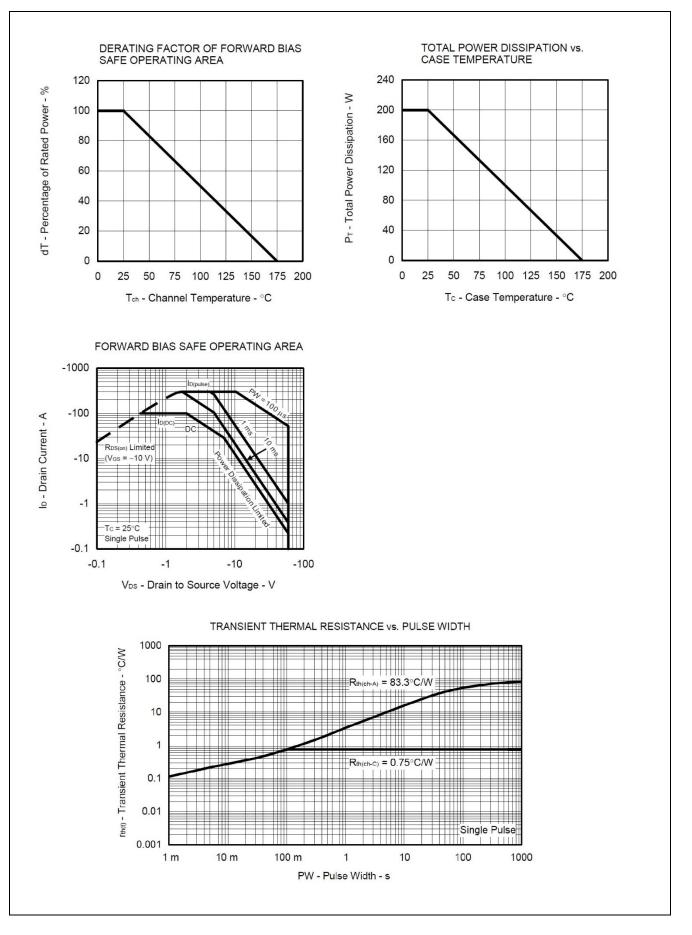
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	_	_	-10	μA	Vds = -60 V, Vgs = 0 V
Gate Leakage Current	I _{GSS}	—	_	∓10	μA	$V_{GS} = \mp 20 V, V_{DS} = 0 V$
Gate to Source Threshold Voltage	V _{GS(th)}	-1.0	-1.6	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	yfs ^{Notes4}	43	86	_	S	V _{DS} = -10 V, I _D = -50 A
Drain to Source On-state Resistance	R _{DS(on)1} Notes4	_	4.4	6.0	mΩ	V _{GS} = -10 V, I _D = -50 A
	R _{DS(on)2} Notes4	_	5.0	7.8	mΩ	V _{GS} = -4.5 V, I _D = -50 A
Input Capacitance	C _{iss}	_	15000	_	pF	V _{DS} = -10 V
Output Capacitance	C _{oss}	—	1810	—	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}	—	840	—	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}	—	28	—	ns	V _{DD} = -30 V
Rise Time	tr	—	35	—	ns	I⊳ = -50 A
Turn-off Delay Time	t _{d(off)}	—	275	—	ns	Vgs = -10 V
Fall Time	t _f	_	100	_	ns	R _G = 0 Ω
Total Gate Charge	Qg	_	300	_	nC	V _{DD} = -48 V
Gate to Source Charge	Q _{gs}	_	35	_	nC	V _{GS} = -10 V
Gate to Drain Charge	Q _{gd}	_	85	_	nC	I⊳ = -100A
Body Diode Forward Voltage	V _{F(S-D)} ^{Notes4}	_	0.92	1.5	V	IF = -100 A, VGS = 0 V
Reverse Recovery Time	t _{rr}	—	70	—	ns	I _F = -100 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	_	135	_	nC	di/dt = -100 A/ <i>µ</i> s

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

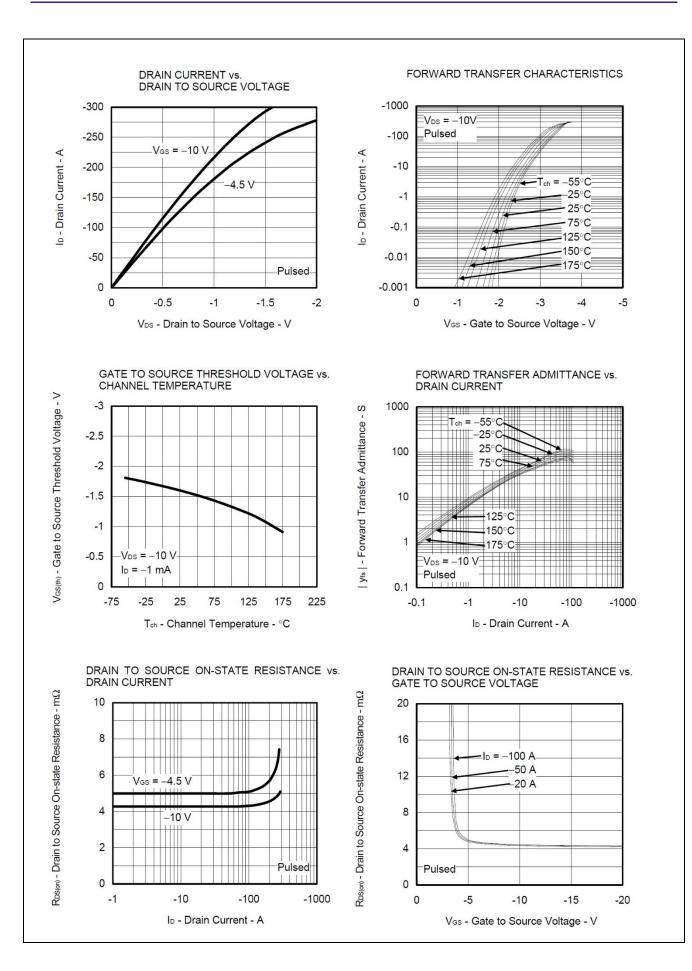
4. Pulse test.

(T_a=25°C)

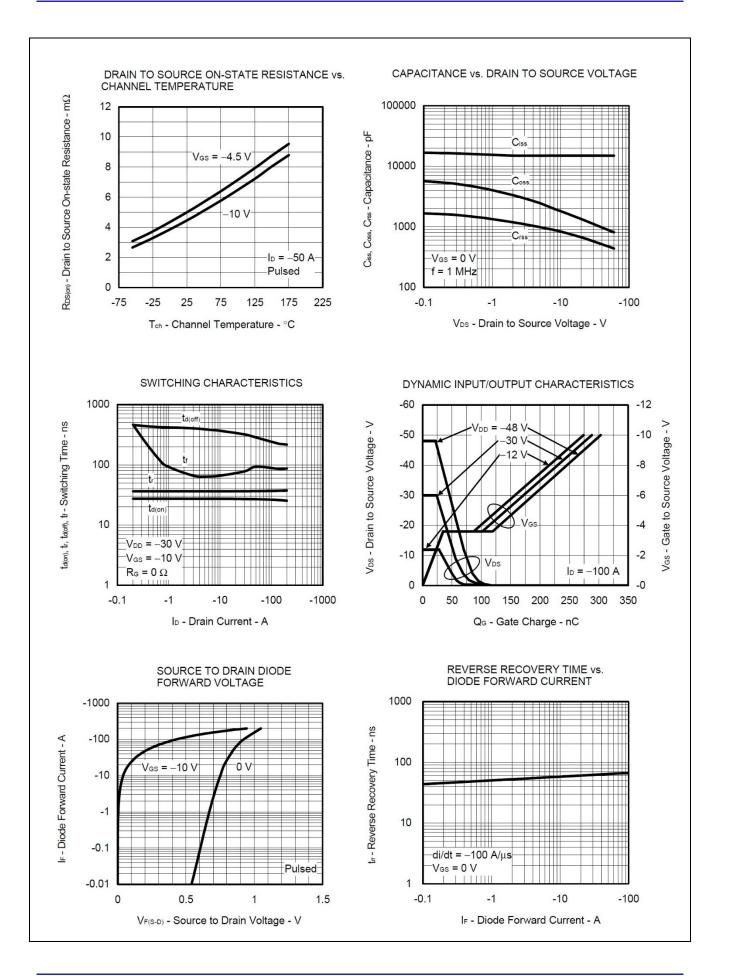
Typical Characteristics





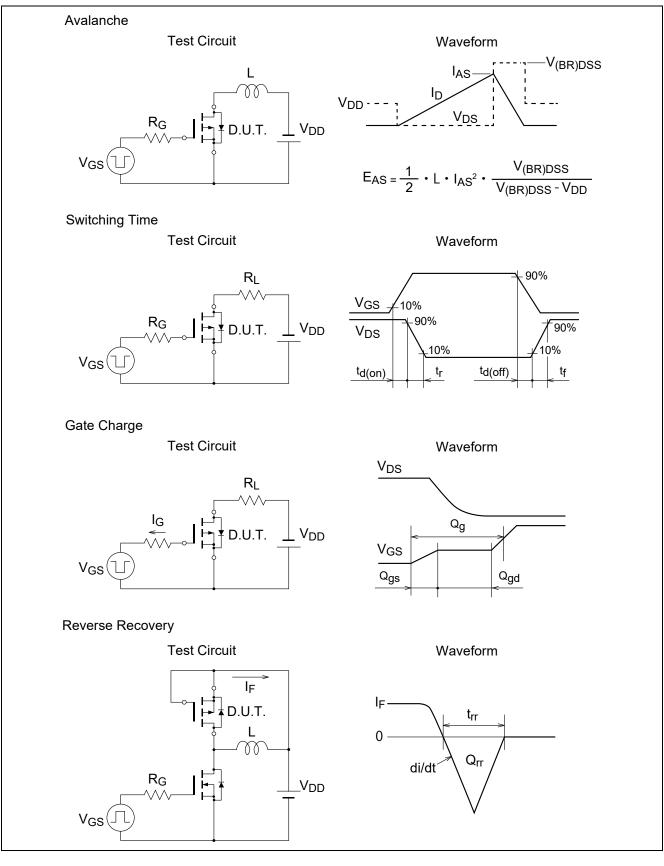




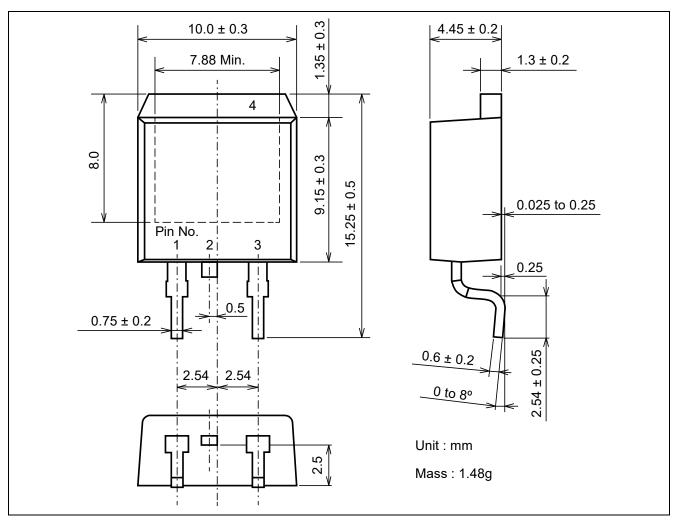


RENESAS

Test Circuit



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping container
NP100P06PLG-E1-AY	800pcs/reel	Taping

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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