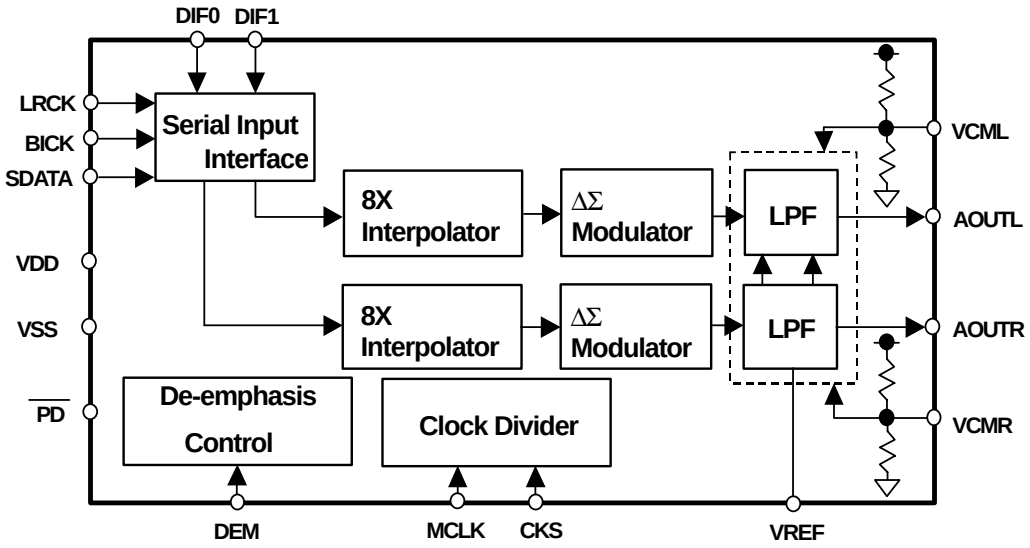
AK4352
2V & Low Power Multi-Bit ΔΣ DAC

GENERAL DESCRIPTION

The AK4352 is an 18bit low voltage & power stereo DAC for digital audio system. The AK4352 uses the new developed Multi-Bit ΔΣ architecture, this new architecture achieves DR=94dB at low voltage operation. The AK4352 includes post filter with single-ended output and does not need any external parts. The AK4352 is suitable for the portable audio system like MD, etc as low power and small package.

FEATURES

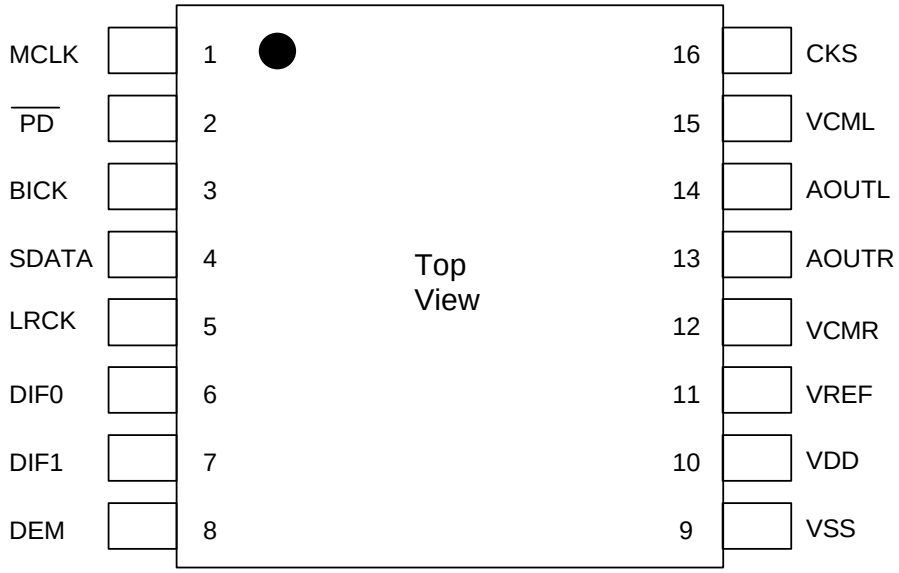
- **Multi-Bit ΔΣ DAC**
- **Sampling Rate Ranging: 8kHz ~ 50kHz**
- **On chip post filter**
- **On chip Buffer with Single-ended Output**
- **On chip Perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.06dB**
  - **Stopband Attenuation: 43dB**
- **Digital Audio I/F format: 2's compliment, MSB first**
  - **18bit MSB justified, 16/18bit LSB justified, I^2S**
- **Digital de-emphasis for 44.1kHz sampling**
- **Master clock: 256fs or 384fs**
- **THD+N: -83dB@2V, -89dB@3V**
- **D-Range: 94dB@2V, 96dB@3V**
- **Output Voltage: 1.10Vpp@2V**
- **Low Voltage Operation: 2V (1.8 ~ 3.6V)**
- **Low power Dissipation: 6mW@2V**
- **Very Small Package: 16pin TSSOP**



■ Ordering Guide

AK4352VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4352	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Pin
2	PD	I	Power-Down Pin When at "L", the AK4352 is in power-down mode and is held in reset. The AK4352 should always be reset upon power-up.
3	BICK	I	Serial Bit Input Clock Pin This clock is used to latch audio data.
4	SDATA	I	Audio Data Input Pin
5	LRCK	I	L/R Clock Pin This input determines which audio channel is currently being input on SDATA pin.
6 7	DIF0 DIF1	I I	Digital Input Format Pin These pins select one of four input modes.
8	DEM	I	De-emphasis Enable Pin When at "H", de-emphasis of fs=44.1kHz is enabled.
9	VSS	-	Ground Pin
10	VDD	-	Power Supply Pin
11	VREF	I	Reference Voltage Input Pin Normally connected to VDD.
12	VCMR	O	Rch Common Voltage Pin
13	AOUTR	O	Rch Analog Output Pin
14	AOUTL	O	Lch Analog Output Pin
15	VCML	O	Lch Common Voltage Pin
16	CKS	I	Master Clock Select Pin "L": 256fs "H": 384fs

Note: All input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V;Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	4.6	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V;Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	1.8	2.0	3.6	V
Voltage Reference (Note 2)	VREF		-	VDD	V

Note 1. All voltages with respect to ground.
Note 2. Analog output voltage scales with the voltage of VREF.
AOUT (typ.@0dB)=1.10Vpp*VREF/2.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=2.0V, VREF=VDD; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 18bit Input Data; Measurement frequency=10Hz ~ 20kHz; $R_L \geq 10k\Omega$; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics	(Note 3)				
THD+N	(0dB Output)		-83	-74	dB
Dynamic Range	(-60dB Output, A-weight)	88	94		dB
S/N	(A-weight)	88	94		dB
Interchannel Isolation		90	100		dB
DC Accuracy					
Interchannel Gain Mismatch			0.1	0.5	dB
Gain Drift		-	60	-	ppm/°C
Output Voltage	(Note 4)	1.02	1.10	1.18	Vpp
Load Resistance		10			kΩ
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$ = "H")					
VDD			3.0	4.7	mA
Power-Down Mode ($\overline{PD}$ = "L")					
VDD	(Note 5)		10	50	μA
Power Dissipation (VDD)					
Normal Operation			6.0	9.4	mW
Power-Down Mode	(Note 5)		20	100	μW
Power Supply Rejection		-	50	-	dB

Note 3. Measured by AD725C (SHIBASOKU). Averaging mode.
In case of VDD=3.0V,
THD+N: -89dB
DR: 96dB (A-weight)
S/N: 97dB (A-weight)

Note 4. Full-scale voltage (0dB). Output voltage scales with the voltage of VREF.
AOUT (typ.@0dB)=1.10Vpp*VREF/2.

Note 5. In case of power-down mode, all digital input pins including clock pins (MCLK,BICK and LRCK) are held VDD or VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD=1.8 ~ 3.6V; fs=44.1kHz; DEM= "L")

Parameter		Symbol	min	typ	max	Units
Digital filter						
Passband	-0.1dB (Note 6)	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband	(Note 6)	SB	24.1			kHz
Passband Ripple		PR			± 0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay	(Note 7)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter						
Frequency Response	0 ~ 20.0kHz		-	± 0.2	-	dB

Note 6. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@-0.1dB), SB=0.546*fs(@-43dB).

Note 7. The calculating delay time which occurred by digital filtering. This time is from setting the 18bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; VDD=1.8 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	75%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	25%VDD	V
Input Leakage Current	Iin	-	-	± 10	μA

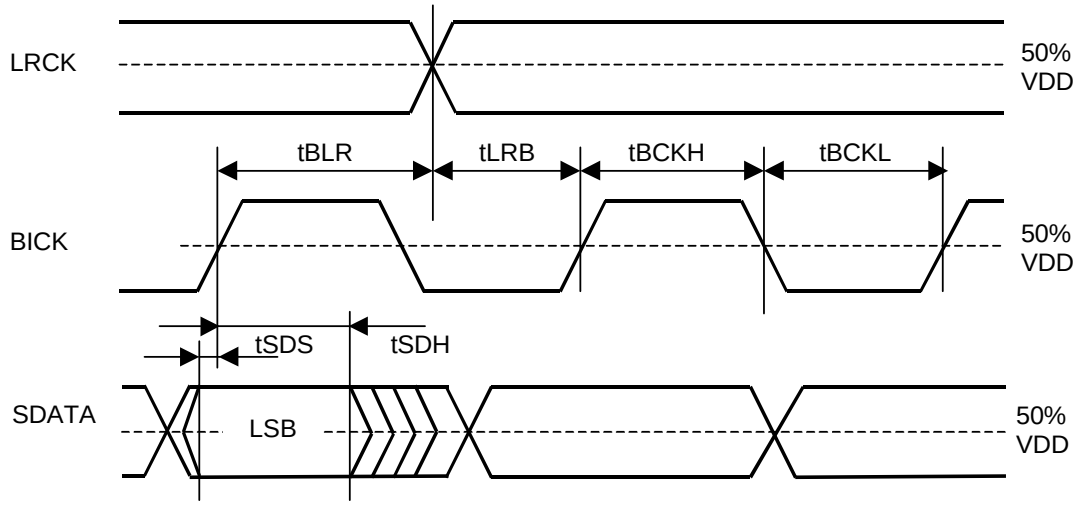
SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=1.8 ~ 3.6V)

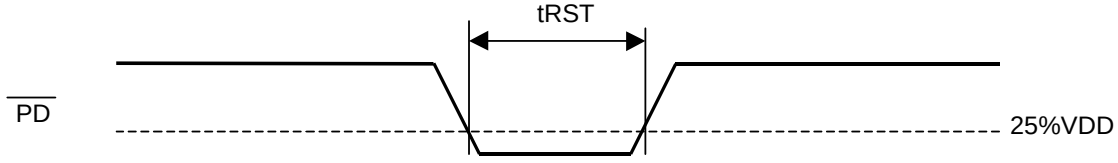
Parameter		Symbol	min	typ	max	Units
Master Clock Timing	256fs:	fCLK	2.048	11.2896	12.8	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	3.072	16.9344	19.2	MHz
	Pulse Width Low	tCLKL	23			ns
	Pulse Width High	tCLKH	23			ns
LRCK Frequency		fs	8	44.1	50	kHz
Serial Interface Timing	(Note 8)					
BICK Period		tBCK	312.5			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
BICK rising to LRCK Edge	(Note 9)	tBLR	50			ns
LRCK Edge to BICK rising	(Note 9)	tLRB	50			ns
SDATA Hold Time		tSDH	50			ns
SDATA Setup Time		tSDS	50			ns
Reset Timing						
$\overline{PD}$ Pulse Width	(Note 10)	tRST	300			ns

Note 8. Refer to the operating overview section “Audio Data Interface”.
Note 9. BICK rising edge must not occur at the same time as LRCK edge.
Note 10. The AK4352 can be reset by bringing $\overline{PD}$ = “L” to “H” only upon power up.

■ Timing Diagram



Audio Data Input Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4352 are MCLK (256fs/384fs) LRCK (fs), BICK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The frequency of MCLK is determined by the sampling rate (LRCK) and CKS pin. Setting CKS= "L" selects an MCLK frequency of 256fs while setting CKS= "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK4352.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4352 is in normal operation mode ($\overline{PD}$ = "H"). If these clocks are not provided, the AK4352 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4352 should be in the power-down mode($\overline{PD}$ = "L").

As the AK4352 includes the phase detection circuit for LRCK, the AK4352 adjusts the phase of LRCK automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

LRCK (fs)	MCLK		BICK (64fs)
	CKS= "L": 256fs	CKS= "H": 384fs	
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 1. Examples of System Clock

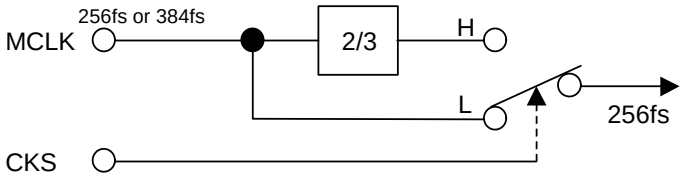


Figure 1. Internal Clock Circuit

■ Audio Serial Interface Format

The AK4352 interfaces with external system by using SDATA, BICK and LRCK pins. Four types of data format are available and one of them is selected by setting DIF0 and DIF1. Format 0 is compatible with existing 16bit DACs and digital filters. Format 1 is an 18bit version of format 0. Format 2 is similar to AKM ADCs and many DSP serial ports. Format 3 is compatible with the I^2S serial data protocol. In format 2 and 3, 16bit data followed by two zeros also could be input. In all modes, the serial data is MSB first and 2's complement format.

DIF1	DIF0	Mode	BICK	Figure
0	0	0: 16bit LSB Justified	≥32fs	Figure 2
0	1	1: 18bit LSB Justified	≥36fs	Figure 2
1	0	2: 18bit MSB Justified	≥36fs	Figure 3
1	1	3: I^2S Compatible	≥32fs or 36fs	Figure 4

Table 2. Digital Input Formats

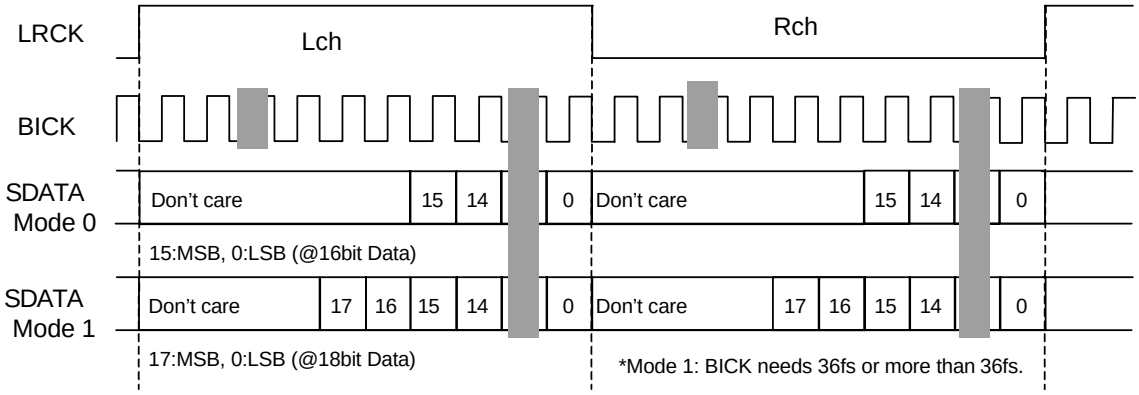


Figure 2. Mode 0,1 Timing

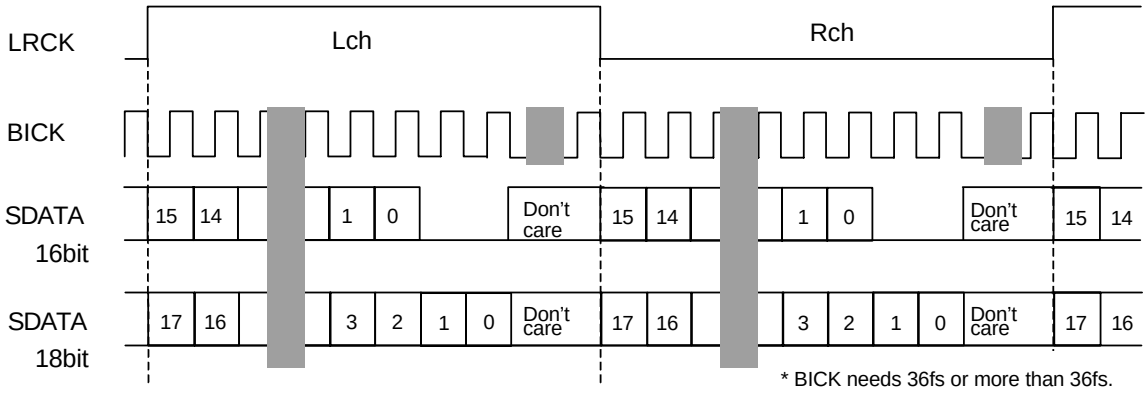


Figure 3. Mode 2 Timing

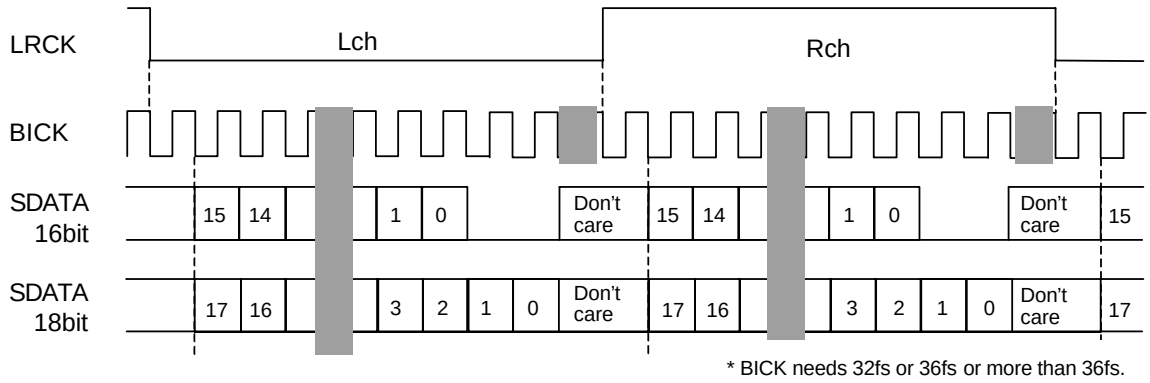


Figure 4. Mode 3 Timing

■ De-emphasis filter

The AK4352 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to 44.1kHz sampling. The de-emphasis is enabled by setting DEM pin "H".

■ Power-down

The AK4352 is placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the anlog outputs are floating(Hi-Z). Figure 5 shows an example of the system timing at the power-down and power-up.

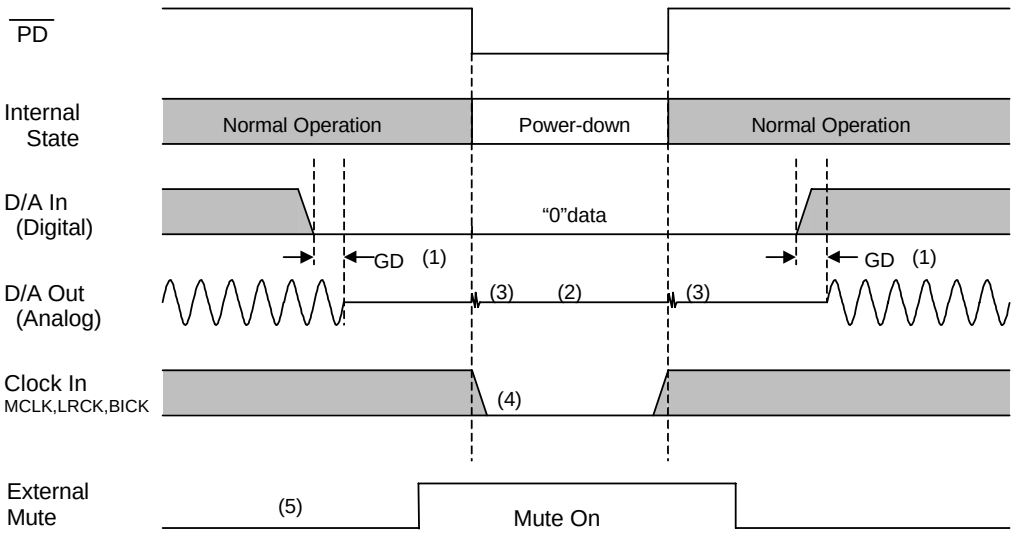


Figure 5. Power-down/up sequence example

Notes:

(1) Analog output corresponding to digital input have the group delay (GD).
(2) Analog outputs are floating(Hi-Z) at the power-down mode.
(3) Click noise occures at the edges("↑ ↓") of the falling edge of $\overline{PD}$ signal.
(4) When the external clocks(MCLK,BICK,LRCK) are stopped, the AK4352 should be in the power-down mode.
(5) Please mute the analog output externally if the click noise(3) influences system application. The timing example is shown in this figure.

■ System Reset

The AK4352 should be reset once by bringing $\overline{PD}$ = "L" upon power-up. The internal timing starts clocking by LRCK "↑" upon exiting reset.

SYSTEM DESIGN

Figure 6 shows the system connection diagram. An evaluation board [AKD4352] is available in order to allow an easy study on the layout of a surrounding circuit.

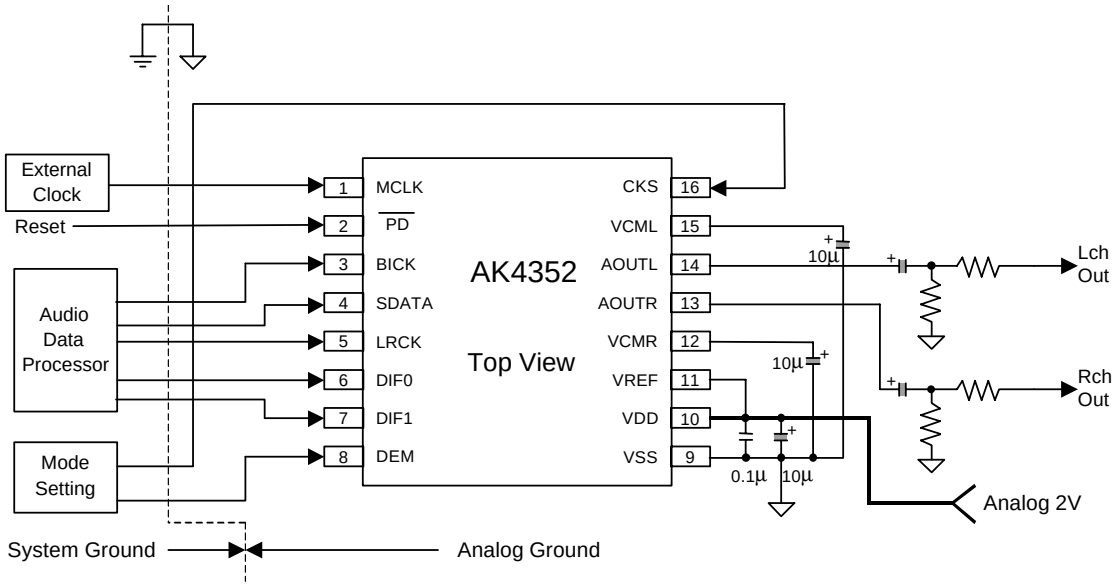


Figure 6. Typical Connection Diagram

Notes:
- LRCK = fs, BICK ≥ 32fs or 36fs, MCLK = 256fs/384fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

1. Grounding and Power Supply Decoupling

Figure 6 shows the power supply connection example. VDD is supplied from analog supply in system. Decoupling capacitors for high frequency should be as near to the AK4352 device as possible, with the low value ceramic capacitor between VREF and VSS being the nearest.

2. Voltage Reference

The differential Voltage between VREF and VSS sets the analog output range. VREF pin is normally connected to VDD. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor are attached between VREF and VSS pins. VCML and VCMR pins are a signal ground of this chip. An electrolytic capacitor less than 10μF parallel with a 0.1μF ceramic capacitor attached between VCML, VCMR pins and VSS eliminates the effects of high frequency noise. Especially, the ceramic capacitor should be connected to these pins as near as possible.

No load current may be drawn from VCML and VCMR pins. All signals, especially clocks, should be kept away from the VREF, VCML and VCMR pins in order to avoid unwanted coupling into the AK4352.

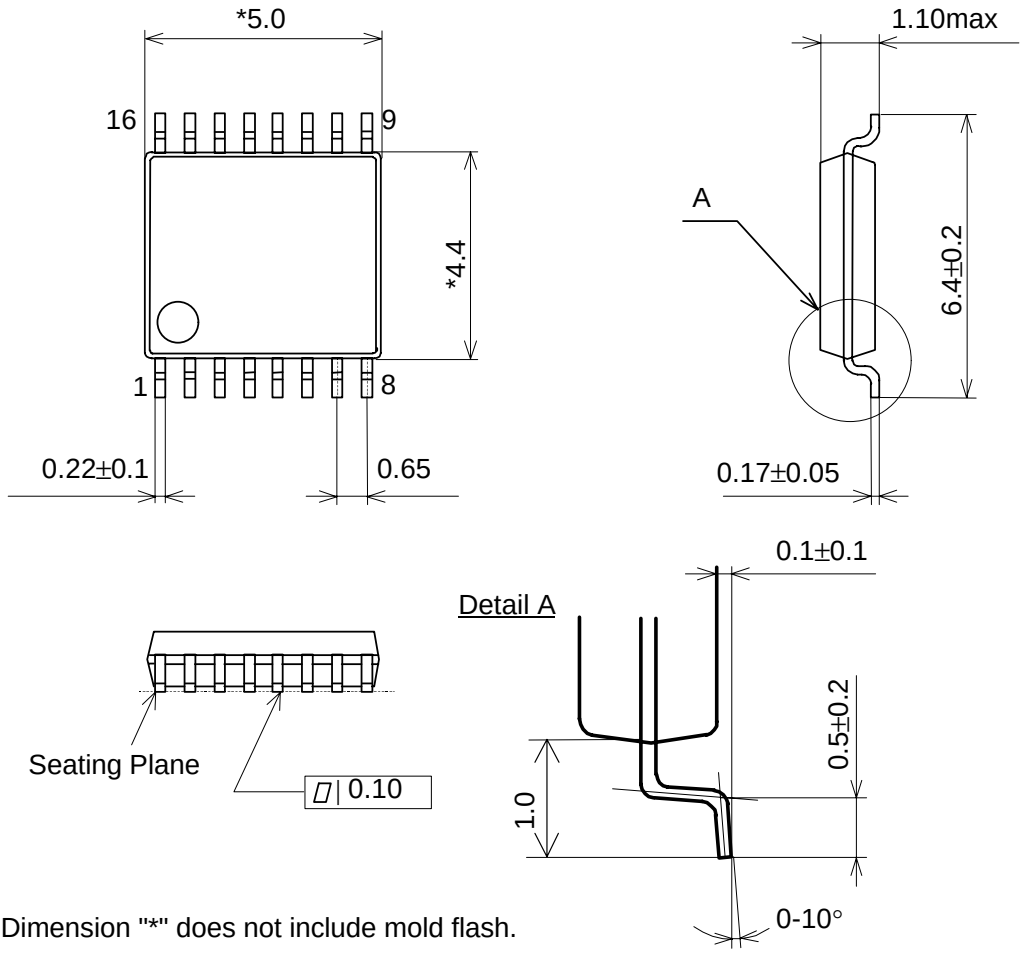
3. Analog Outputs

The analog outputs are single-ended and centered around the VCML, VCMR voltage. The output signal range is typically 1.10Vpp. If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCML, VCMR voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCML, VCMR voltage + a few mV.

PACKAGE

16pin TSSOP (Unit: mm)

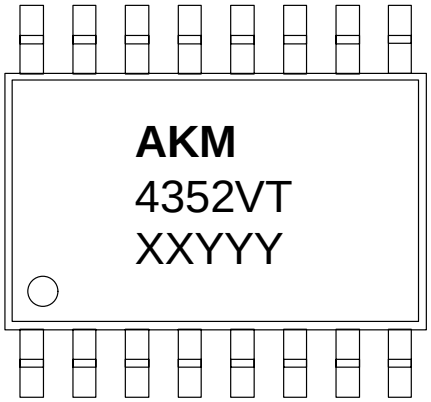


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of XXYYY
XX: Lot#
YYY: Date Code

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