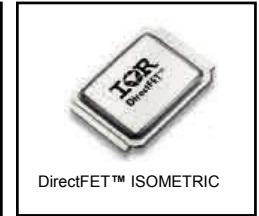
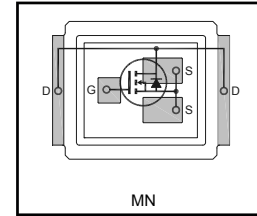


DirectFET® Power MOSFET②  
Typical values (unless otherwise specified)

<b>V<sub>DSS</sub></b>	<b>V<sub>GS</sub></b>	<b>R<sub>DS(on)</sub></b>
100V min	±20V max	5.3mΩ @ 10V
<b>Q<sub>g tot</sub></b>	<b>Q<sub>gd</sub></b>	<b>V<sub>gs(th)</sub></b>
36nC	13nC	2.9V



**Applications and Benefits**

- Ideal for High Performance Isolated Converter Primary Switch
- Optimized for Synchronous Rectification
- [RoHS Compliant, Halogen Free](#) ②
- [Lead-Free \(Qualified up to 260°C Reflow\)](#) ①
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- [Dual Sided Cooling Compatible](#) ①
- [Compatible with existing Surface Mount Techniques](#) ①
- Industrial Qualified

[Applicable DirectFET® Outline and Substrate Outline](#) ①

				<b>MN</b>				
--	--	--	--	-----------	--	--	--	--

**Description**

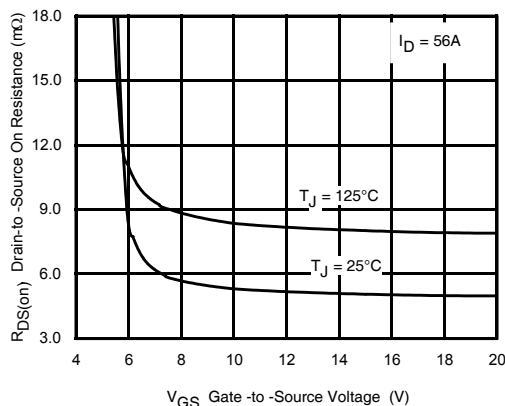
The IRF7171MTRPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET® packaging to achieve the lowest on-state resistance in a package that has a footprint smaller than a D2PAK and only 0.7 mm profile. The DirectFET® package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when [application note AN-1035](#) is followed regarding the manufacturing methods and processes. The DirectFET® package allows dual sided cooling to maximize thermal transfer in power systems. The IRF7171MTRPbF is optimized for high frequency switching and synchronous rectification applications. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance power converters.

**Ordering Information**

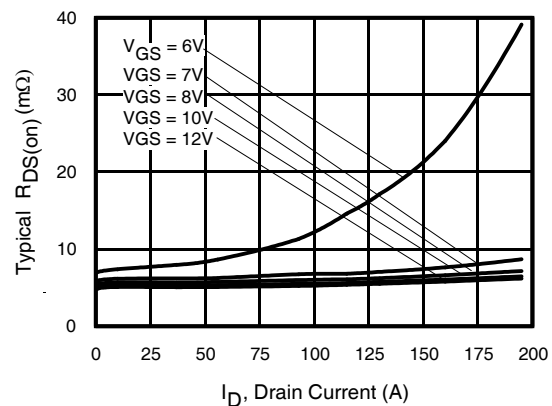
Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7171MTRPbF	DirectFET® Medium Can	Tape and Reel	4800	IRF7171MTRPbF

**Absolute Maximum Ratings**

	Parameter	Max.	Units
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)④	93	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)④	59	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)③	15	
I <sub>DM</sub>	Pulsed Drain Current⑤	330	
E <sub>AS</sub>	Single Pulse Avalanche Energy ⑥	86	mJ
I <sub>AR</sub>	Avalanche Current ⑥	56	A



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Typical On-Resistance vs. Drain Current

**Notes**


- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET® Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ TC measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T<sub>J</sub> = 25°C, L = 55μH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 56A.

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	40	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	5.3	6.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 56A ⑦	
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	3.6	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA	
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Temp. Coefficient	—	-6.2	—	mV/°C		
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1	μA	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0V	
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V	
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V	
g <sub>fs</sub>	Forward Transconductance	80	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 56A	
Q <sub>g</sub>	Total Gate Charge	—	36	54	nC	V <sub>DS</sub> = 50V V <sub>GS</sub> = 10V I <sub>D</sub> = 56A See Fig.8	
Q <sub>gs1</sub>	Pre- V <sub>th</sub> Gate-to-Source Charge	—	6.9	—			
Q <sub>gs2</sub>	Post- V <sub>th</sub> Gate-to-Source Charge	—	2.4	—			
Q <sub>gd</sub>	Gate-to-Drain Charge	—	13	—			
Q <sub>godr</sub>	Gate Charge Overdrive	—	13.7	—			
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	15.4	—			
Q <sub>oss</sub>	Output Charge	—	120	—			nC
R <sub>G</sub>	Gate Resistance	—	1.0	—	Ω		
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.3	—	ns	V <sub>DD</sub> = 50V, V <sub>GS</sub> = 10V⑦ I <sub>D</sub> = 56A R <sub>G</sub> = 1.8Ω	
t <sub>r</sub>	Rise Time	—	27	—			
t <sub>d(off)</sub>	Turn-Off Delay Time	—	15	—			
t <sub>f</sub>	Fall Time	—	20	—			
C <sub>iss</sub>	Input Capacitance	—	2160	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz	
C <sub>oss</sub>	Output Capacitance	—	970	—			
C <sub>rss</sub>	Reverse Transfer Capacitance	—	60	—			
C <sub>oss</sub>	Output Capacitance	—	4660	—			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	580	—			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V, f = 1.0MHz

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	95	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ⑤	—	—	330		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 56A, V <sub>GS</sub> = 0V ⑦
t <sub>rr</sub>	Reverse Recovery Time	—	66	—	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 56A, V <sub>DD</sub> = 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	126	—	nC	di/dt = 100A/μs ⑦

**Notes:**

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	104	W
$P_D @ T_C = 100^\circ\text{C}$	Power Dissipation ④	42	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-55 to + 150	
$T_{STG}$	Storage Temperature Range		

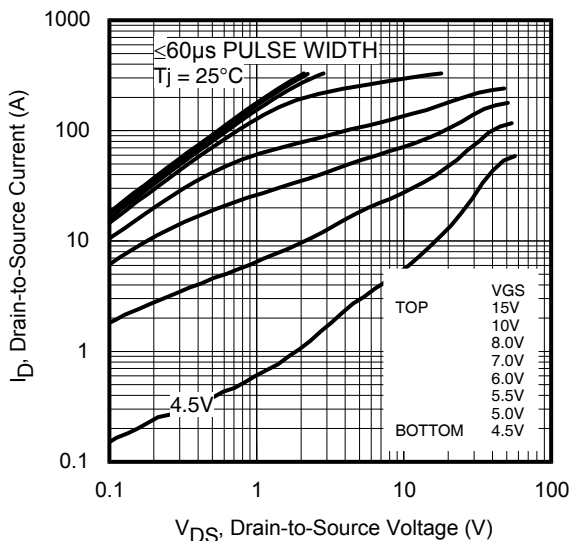
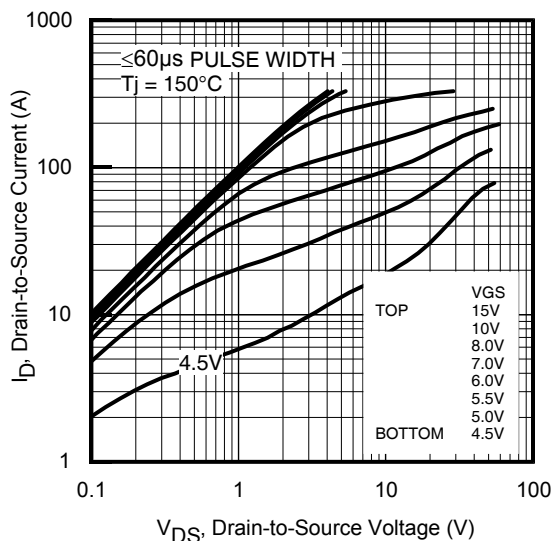
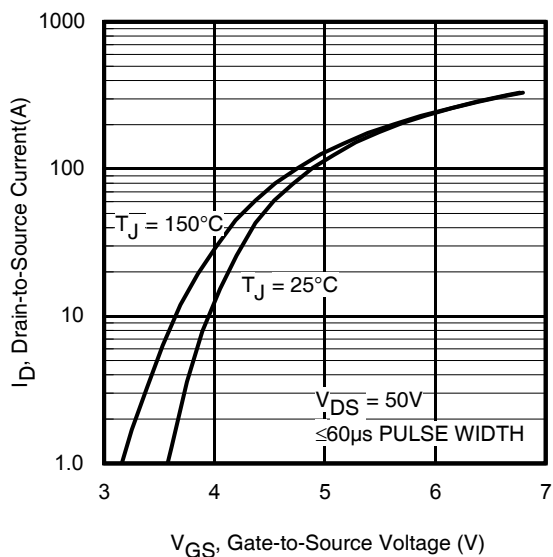
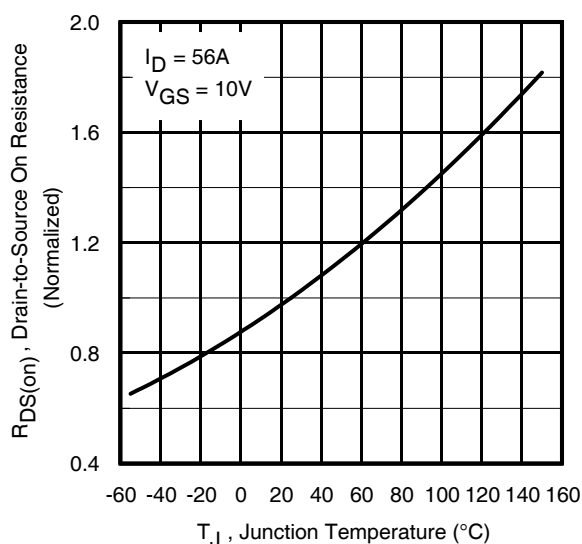
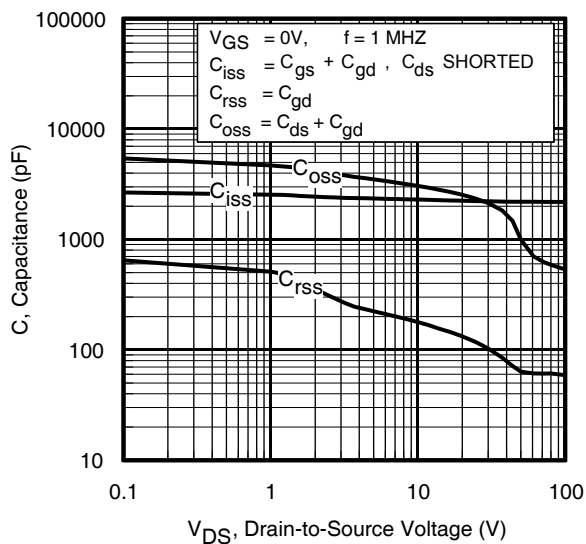
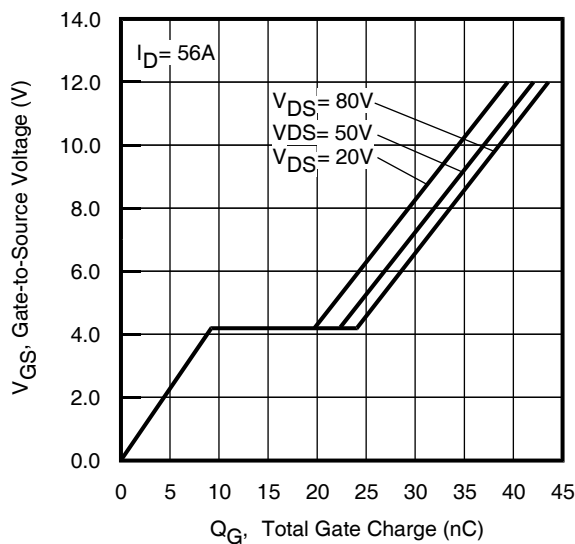
**Thermal Resistance**

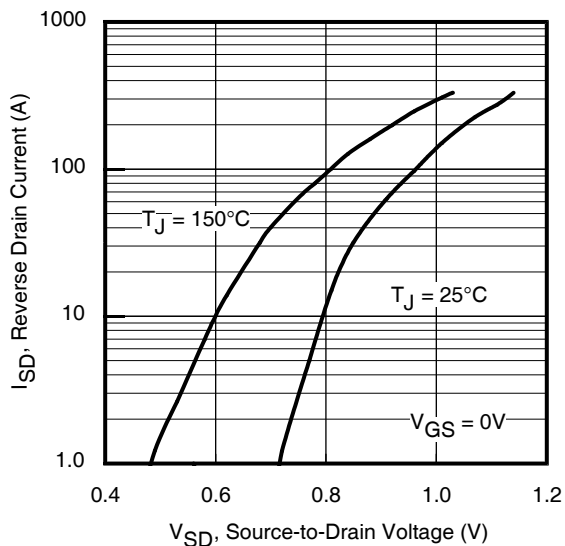
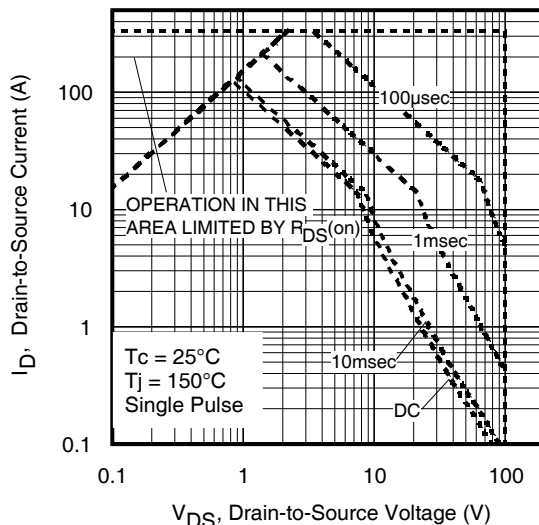
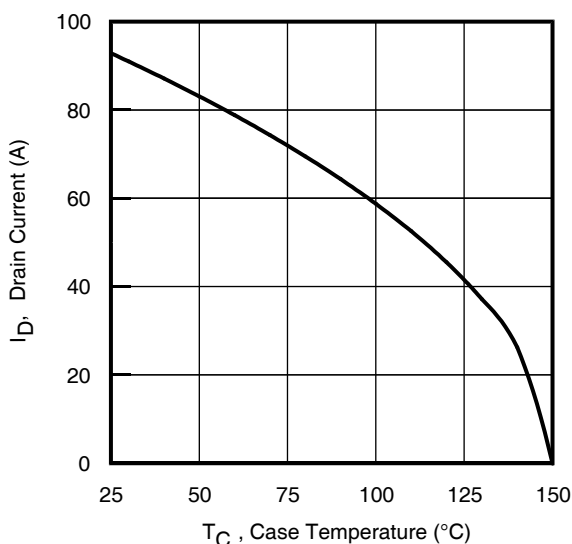
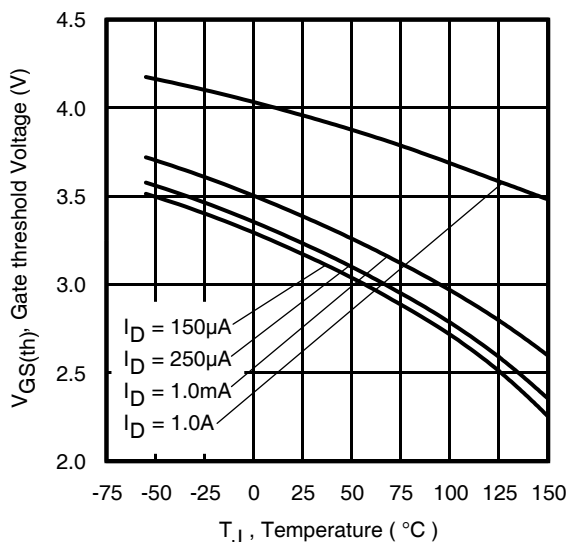
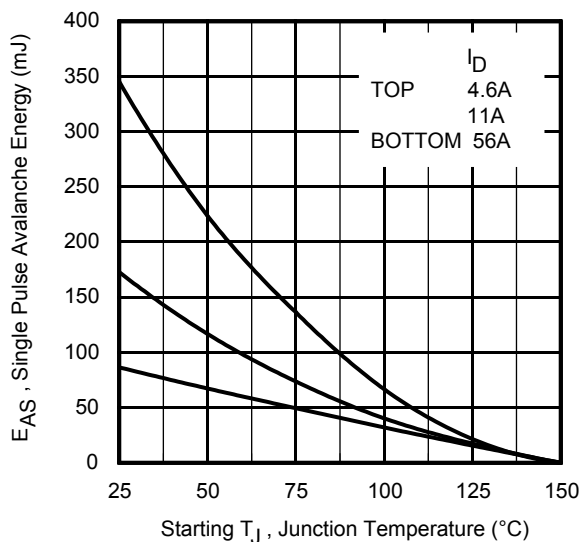
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑥	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	20	—	
$R_{\theta JC}$	Junction-to-Can ④ ⑩	—	1.2	
$R_{\theta JA-PCB}$	Junction-to-PCB Mounted	1.0	—	

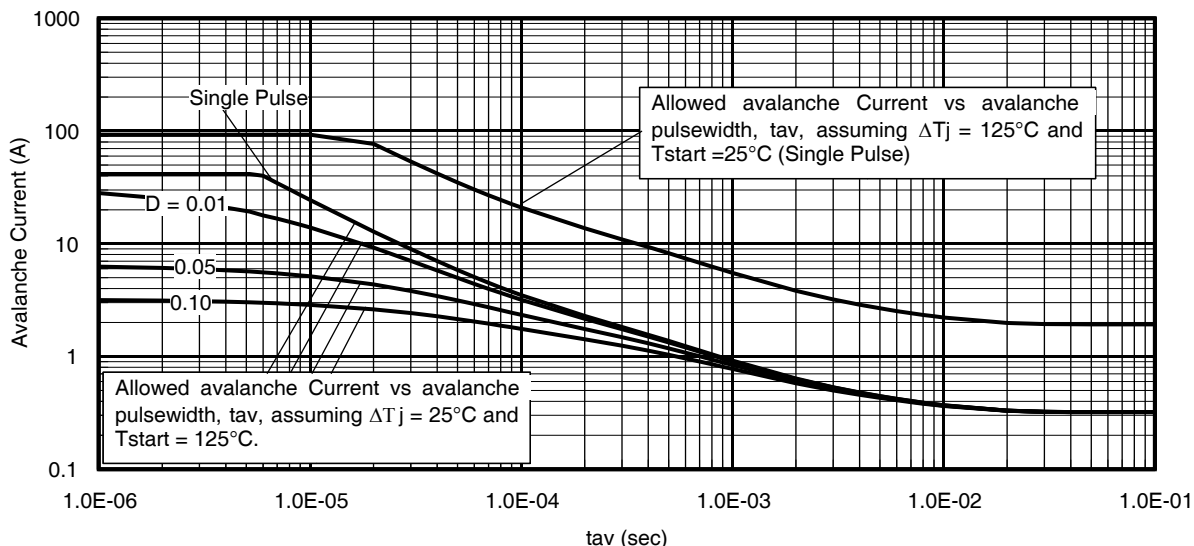
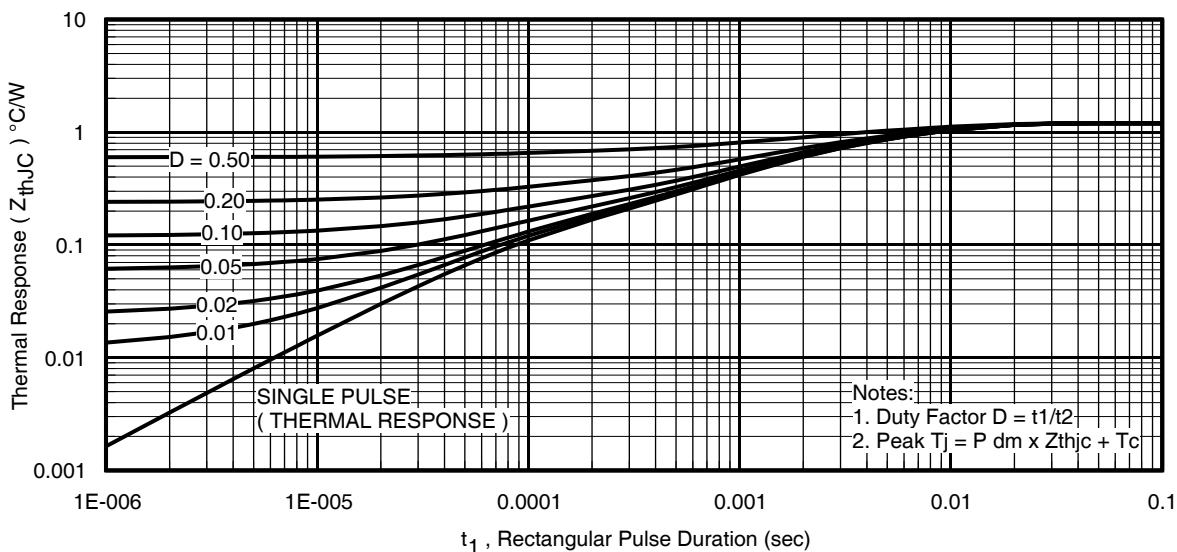
**Notes:**

- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple in contact with top (Drain) of part.

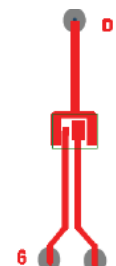
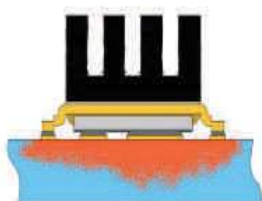
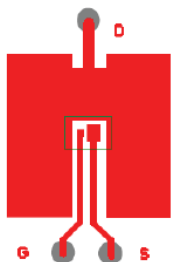
- ⑥ Used double sided cooling, mounting pad with large heat sink.
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heat sink.
- ⑩  $R_{\theta}$  is measured at  $T_J$  of approximately 90°C.


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**

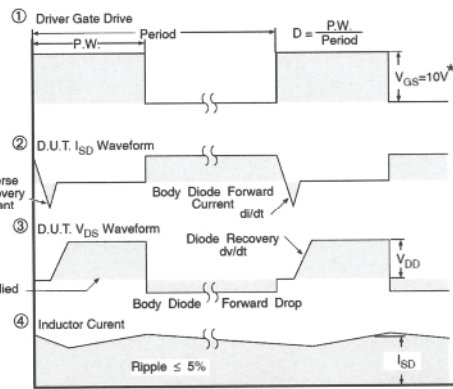
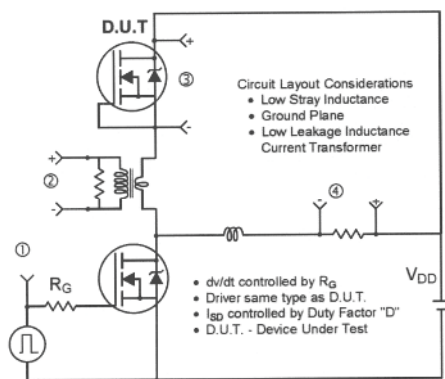

**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Maximum Drain Current vs. Case Temperature

**Fig 12.** Typical Threshold Voltage vs. Junction Temperature

**Fig 13.** Maximum Avalanche Energy vs. Drain Current


**Fig 14. Typical Avalanche Current vs. Pulse Width**

**Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case**
**Notes:**

- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_c$  measured with thermocouple incontact with top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Used double sided cooling, mounting pad with large heatsink.
- ⑦ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑧  $R_{\theta}$  is measured at  $T_j$  of approximately 90°C.

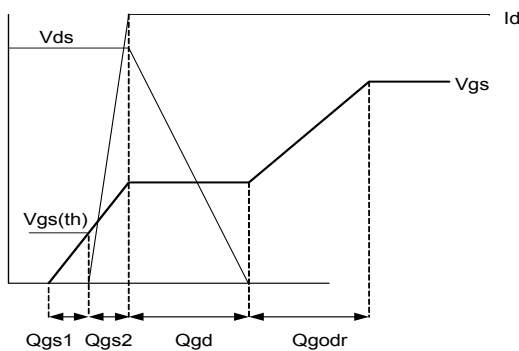
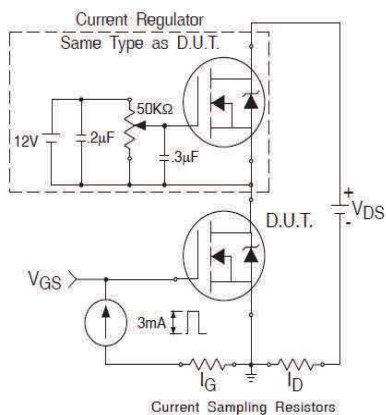


- ③ Surface mounted on 1 in. square Cu board (still air).
- ⑦ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)



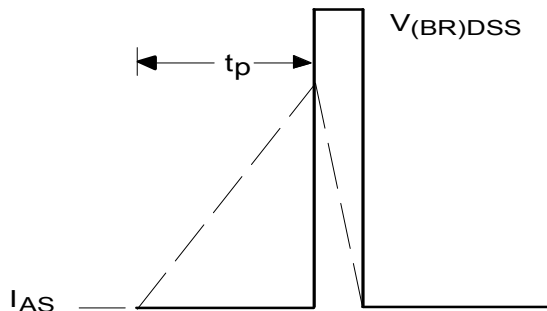
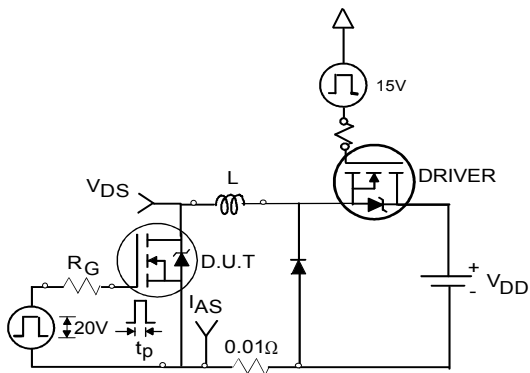
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 16.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



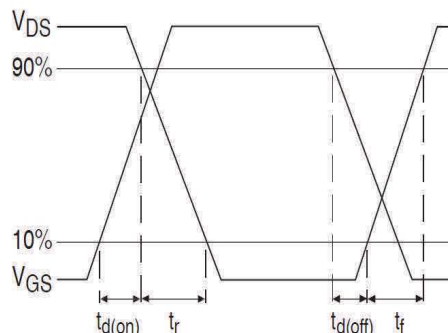
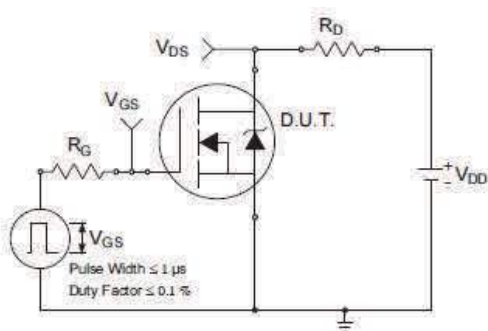
**Fig 17a.** Gate Charge Test Circuit

**Fig 17b.** Gate Charge Waveform



**Fig 18a.** Unclamped Inductive Test Circuit

**Fig 18b.** Unclamped Inductive Waveforms

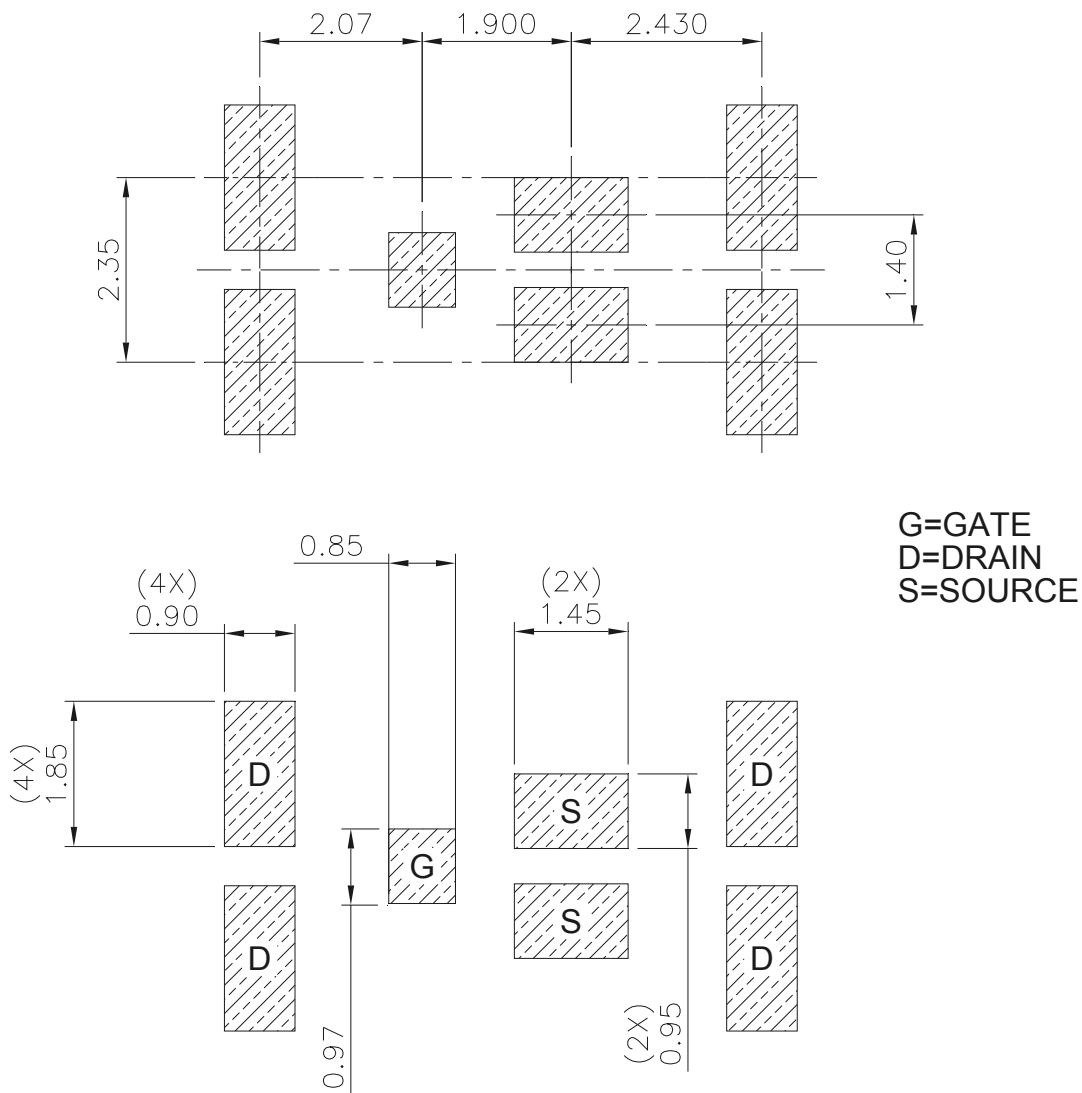


**Fig 19a.** Switching Time Test Circuit

**Fig 19b.** Switching Time Waveforms

**DirectFET® Board Footprint, MN Outline**

Please see DirectFET® application note [AN-1035](#) for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.

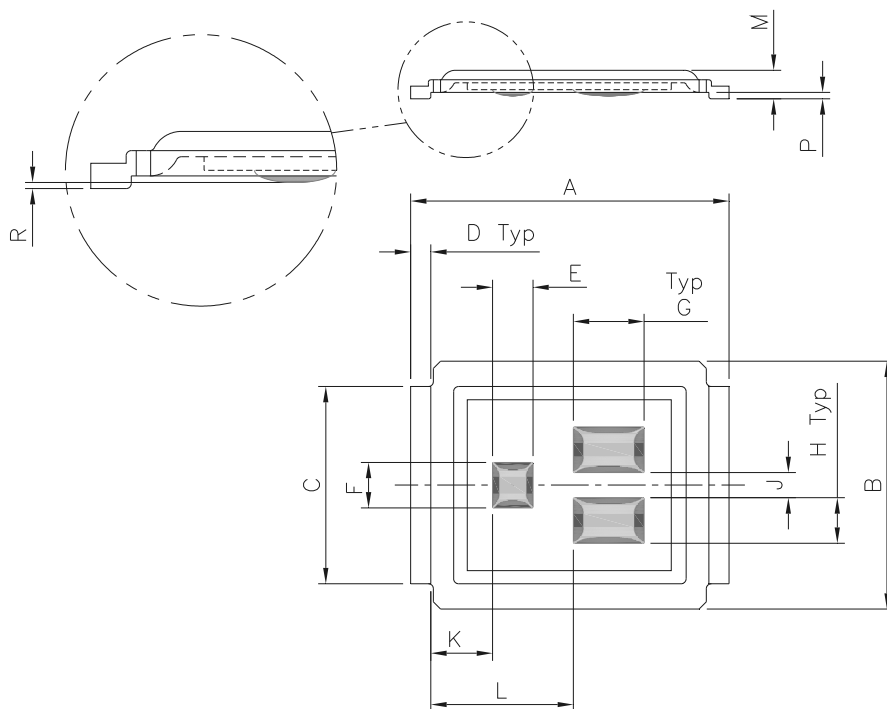


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



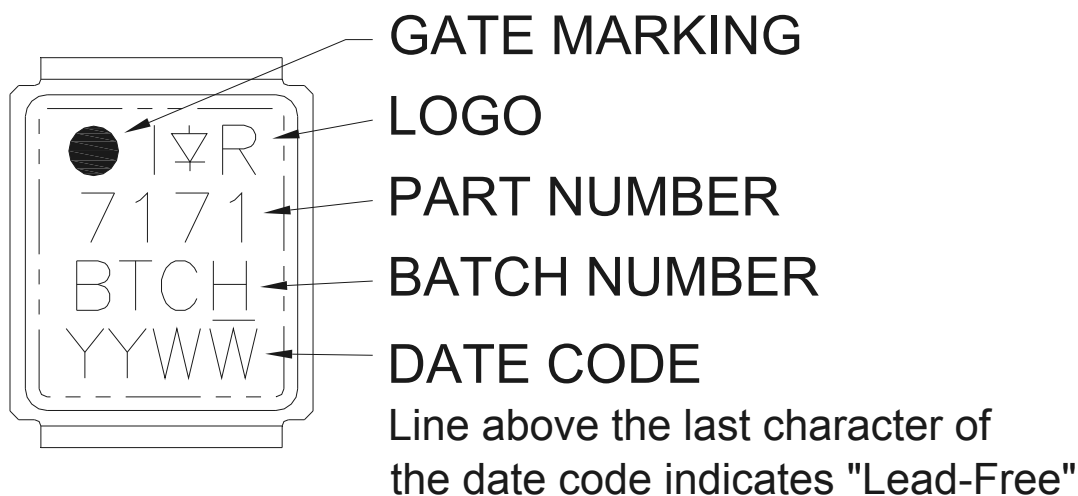
**DirectFET® Outline Dimension, MN Outline  
(Medium Size Can, N-Designation).**

Please see DirectFET® application note [AN-1035](#) for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.

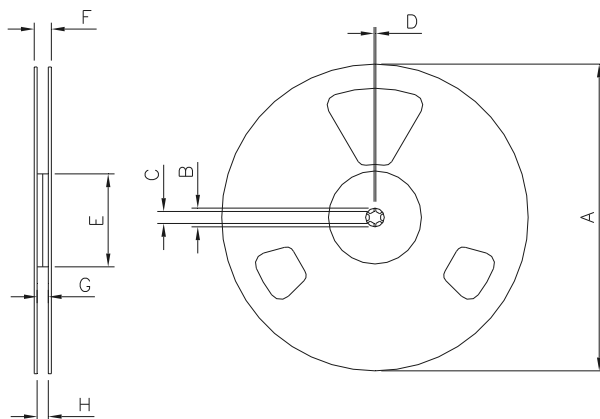


CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.78	0.82	0.031	0.032
F	0.88	0.92	0.035	0.036
G	1.38	1.42	0.054	0.056
H	0.88	0.92	0.035	0.036
J	0.48	0.52	0.019	0.020
K	1.17	1.27	0.046	0.050
L	2.77	2.87	0.109	0.113
M	0.535	0.595	0.021	0.023
R	0.02	0.08	0.0008	0.0031
P	0.08	0.17	0.003	0.007

Dimensions are shown in millimeters (inches)

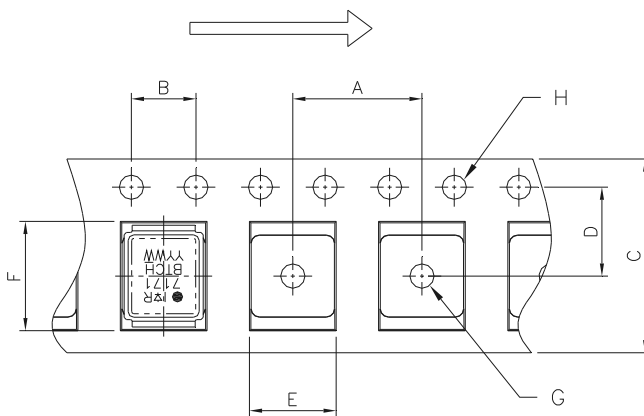
**DirectFET® Part Marking**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**DirectFET® Tape & Reel Dimension (Showing component orientation).**


NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. (ordered as IRF7171MTRPbF). For 1000 parts on 7" reel, order IRF7171MTR1PbF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

**LOADED TAPE FEED DIRECTION**


NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>†† *</sup>	
<b>Moisture Sensitivity Level</b>	DirectFET <sup>®</sup> Medium Can	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

\* Industrial qualification standards except autoclave test conditions.

**Revision History**

<b>Date</b>	<b>Comment</b>
12/3/2014	<ul style="list-style-type: none"> <li>Updated <math>R_{\theta JA}</math> from "60°C/W" to "45°C/W" on page 3.</li> <li>Updated <math>I_D @ T_A</math> and <math>P_D @ T_A</math> based on <math>R_{\theta JA}</math> corrected on page 1 &amp; page 3.</li> </ul>
3/25/2015	<ul style="list-style-type: none"> <li>Added "FastIRFET" on page 1.</li> </ul>