

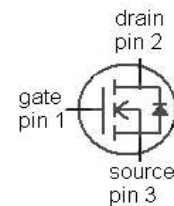
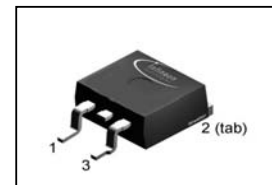
OptiMOS[®] 2 Power-Transistor
Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel - Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

Product Summary

| | | |
|------------------|-----|----|
| V_{DS} | 25 | V |
| $R_{DS(on),max}$ | 6.2 | mΩ |
| I_D | 50 | A |

PG-TO263-3-2



| Type | Package | Marking |
|--------------|--------------|---------|
| IPBH6N03LA G | PG-TO263-3-2 | H6N03LA |

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|-------------------------------------|----------------|---|-------------|-------------------|
| Continuous drain current | I_D | $T_C=25\text{ °C}^{2)}$ | 50 | A |
| | | $T_C=100\text{ °C}$ | 50 | |
| Pulsed drain current | $I_{D,pulse}$ | $T_C=25\text{ °C}^{3)}$ | 350 | |
| Avalanche energy, single pulse | E_{AS} | $I_D=50\text{ A}$, $R_{GS}=25\text{ Ω}$ | 150 | mJ |
| Reverse diode dv/dt | dv/dt | $I_D=50\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$ | 6 | kV/ μs |
| Gate source voltage ⁴⁾ | V_{GS} | | ± 20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 71 | W |
| Operating and storage temperature | T_j, T_{stg} | | -55 ... 175 | °C |
| IEC climatic category; DIN IEC 68-1 | | | 55/175/56 | |

¹⁾ J-STD20 and JESD22

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Thermal characteristics

| | | | | | | |
|-------------------------------------|------------|--|---|---|-----|-----|
| Thermal resistance, junction - case | R_{thJC} | | - | - | 2.1 | K/W |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ⁵⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25$ °C, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|-----|------|----|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0$ V, $I_D=1$ mA | 25 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}$, $I_D=30$ μA | 1.2 | 1.6 | 2 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=25$ V, $V_{GS}=0$ V, $T_j=25$ °C | - | 0.1 | 1 | μA |
| | | $V_{DS}=25$ V, $V_{GS}=0$ V, $T_j=125$ °C | - | 10 | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20$ V, $V_{DS}=0$ V | - | 10 | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=4.5$ V, $I_D=30$ A | - | 8.2 | 10.2 | mΩ |
| | | $V_{GS}=10$ V, $I_D=50$ A | - | 5.2 | 6.2 | |
| Gate resistance | R_G | | - | 1.3 | - | Ω |
| Transconductance | g_{fs} | $ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50$ A | 34 | 68 | - | S |

²⁾ Current is limited by bondwire; with an $R_{thJC}=2.1$ K/W the chip is able to carry 80 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150$ °C and duty cycle $D<0.25$ for $V_{GS}<-5$ V

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ Diagrams are related to straight lead versions.

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics

| | | | | | | |
|------------------------------|--------------|---|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$ | - | 1800 | 2390 | pF |
| Output capacitance | C_{oss} | | - | 690 | 920 | |
| Reverse transfer capacitance | C_{rss} | | - | 85 | 130 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$ | - | 7 | 10 | ns |
| Rise time | t_r | | - | 6 | 8 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 23 | 35 | |
| Fall time | t_f | | - | 4.2 | 6.3 | |

Gate Charge Characteristics⁶⁾

| | | | | | | |
|------------------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=15\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$ | - | 5.9 | 7.8 | nC |
| Gate charge at threshold | $Q_{g(th)}$ | | - | 2.9 | 3.8 | |
| Gate to drain charge | Q_{gd} | | - | 4.1 | 6.1 | |
| Switching charge | Q_{sw} | | - | 7.1 | 10 | |
| Gate charge total | Q_g | | - | 14 | 19 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.3 | - | |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | $V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$ | - | 13 | 17 | nC |
| Output charge | Q_{oss} | $V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$ | - | 15 | 20 | |

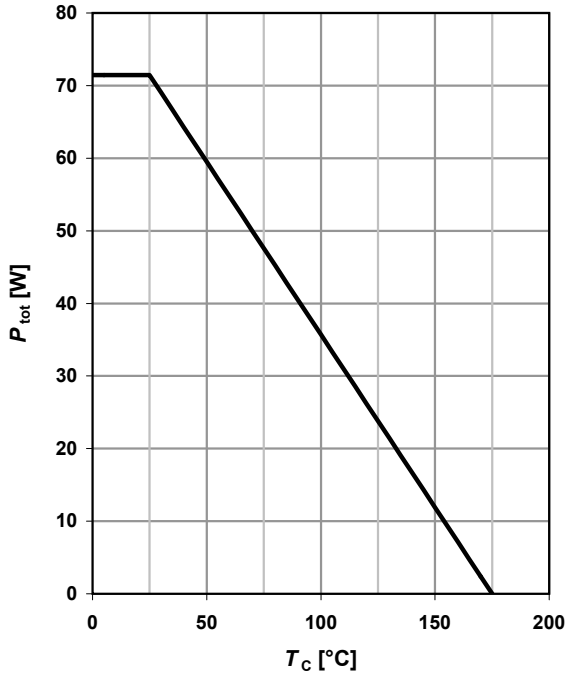
Reverse Diode

| | | | | | | |
|----------------------------------|---------------|---|---|------|-----|----|
| Diode continuous forward current | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 50 | A |
| Diode pulse current | $I_{S,pulse}$ | | - | - | 350 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$ | - | 0.94 | 1.2 | V |
| Reverse recovery charge | Q_{rr} | $V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$ | - | - | 10 | nC |

⁶⁾ See figure 16 for gate charge parameter definition

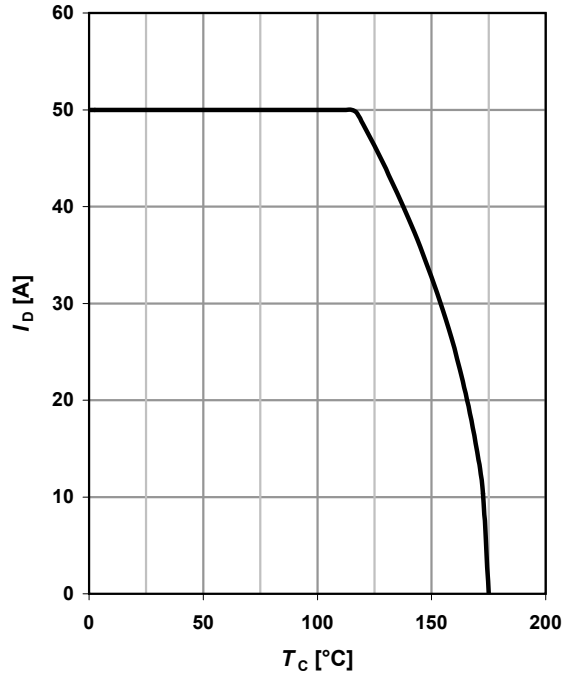
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Drain current

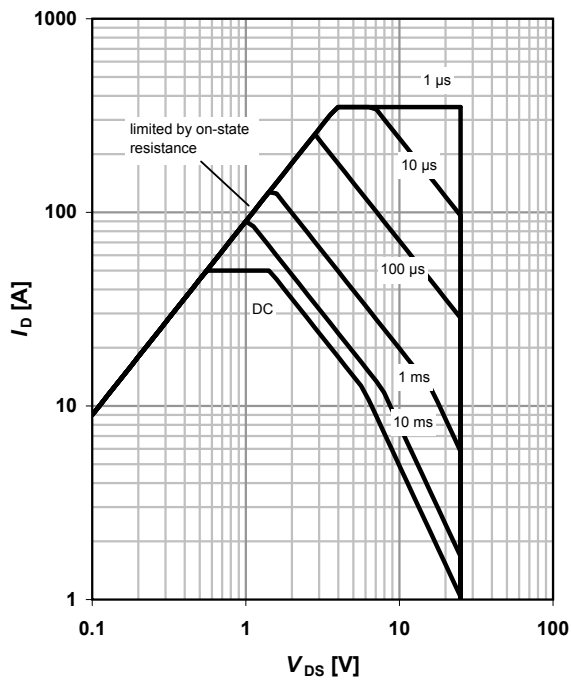
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

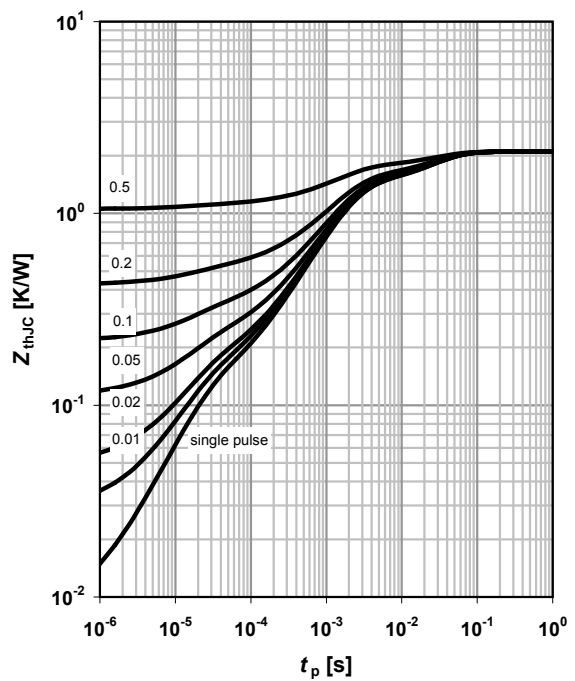
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

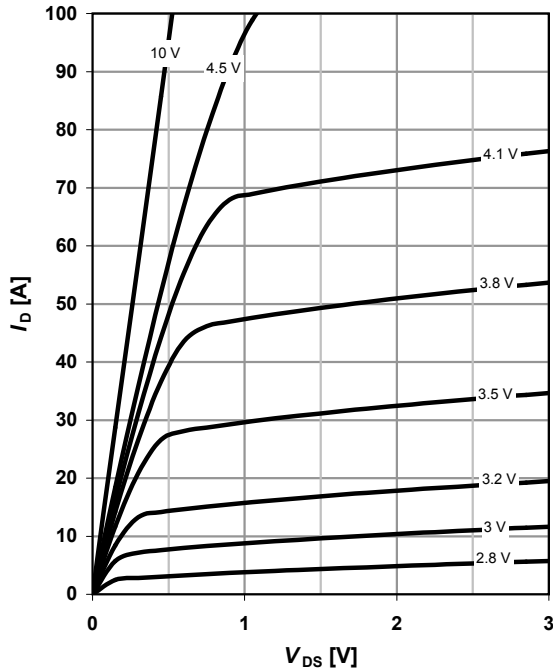
parameter: $D = t_p / T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

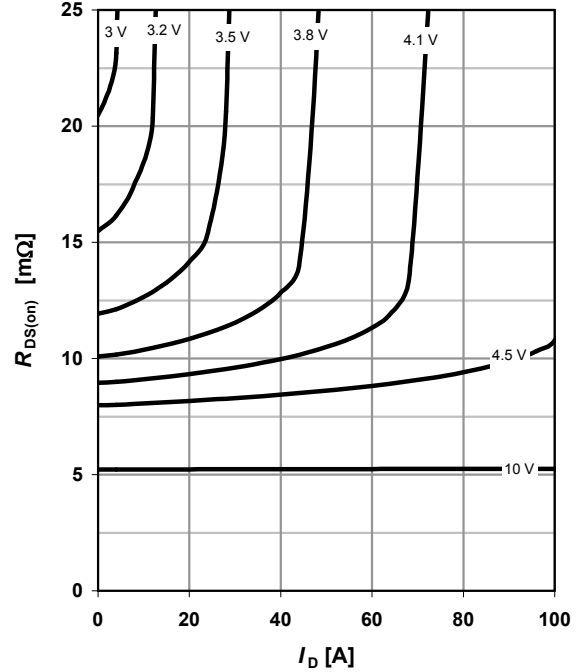
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

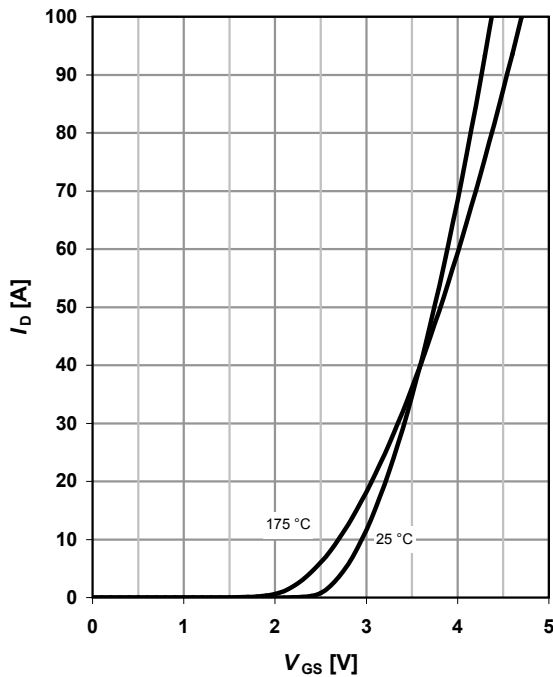
parameter: V_{GS}



7 Typ. transfer characteristics

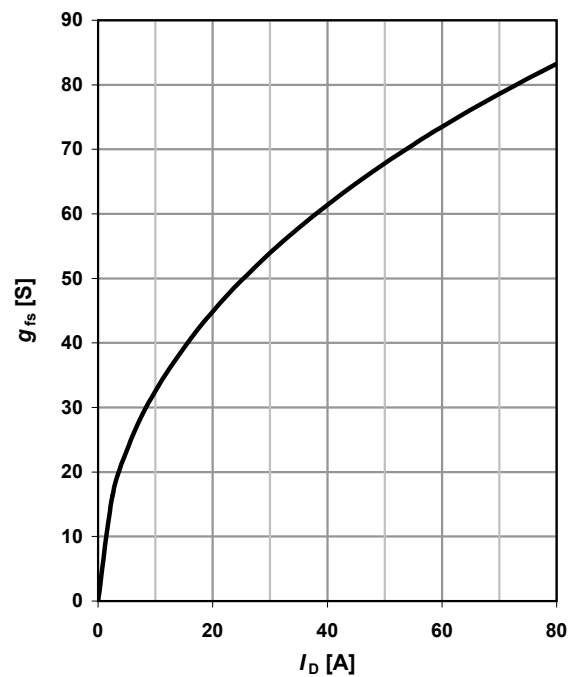
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



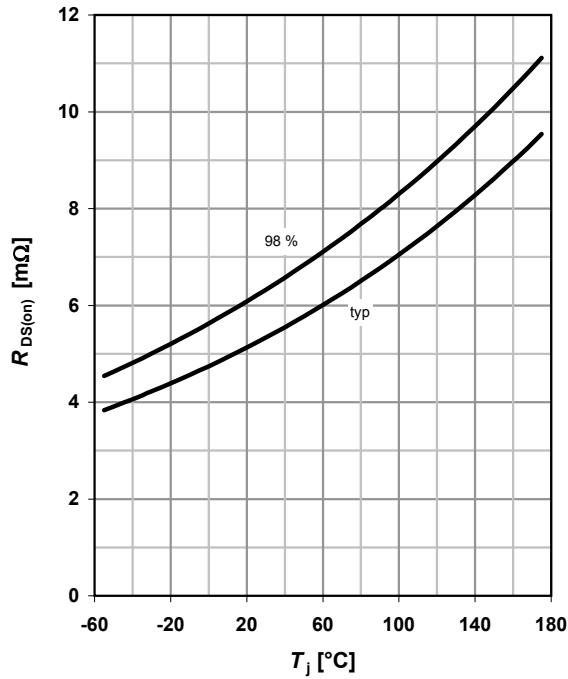
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

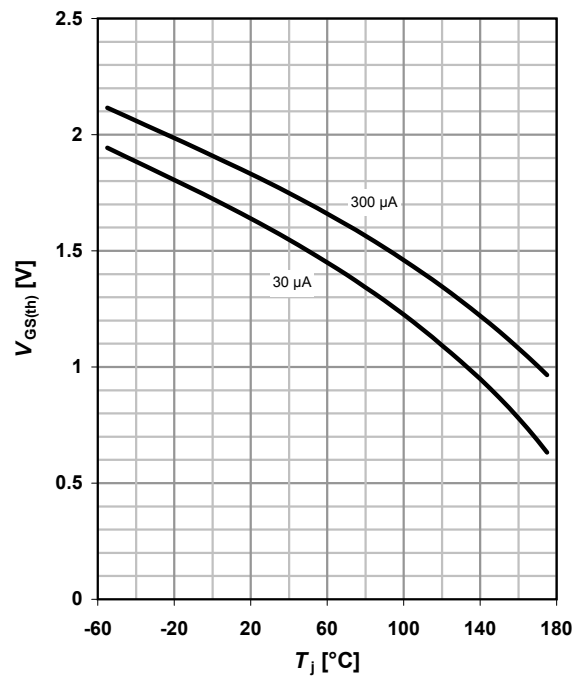
$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

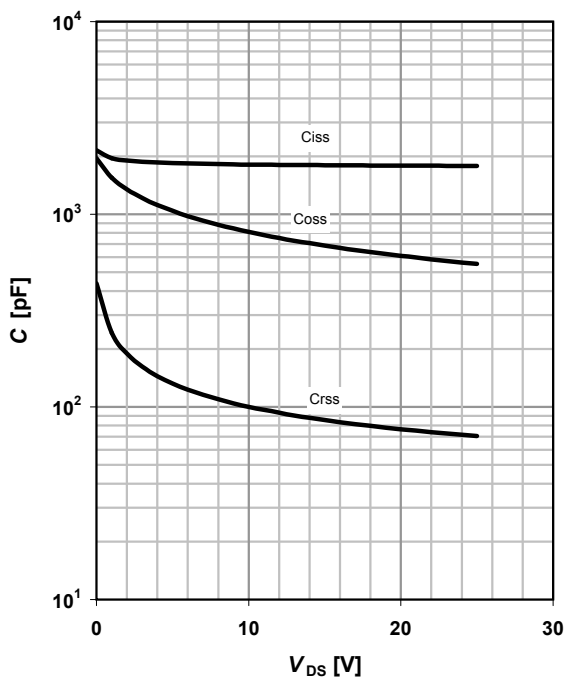
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

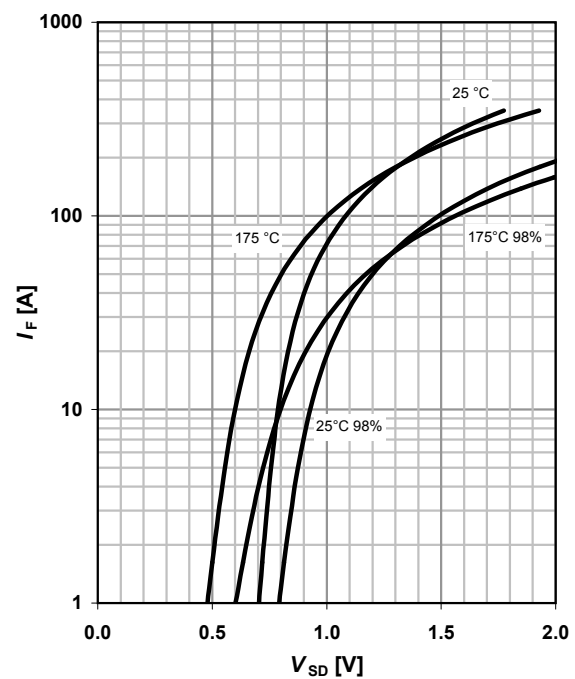
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

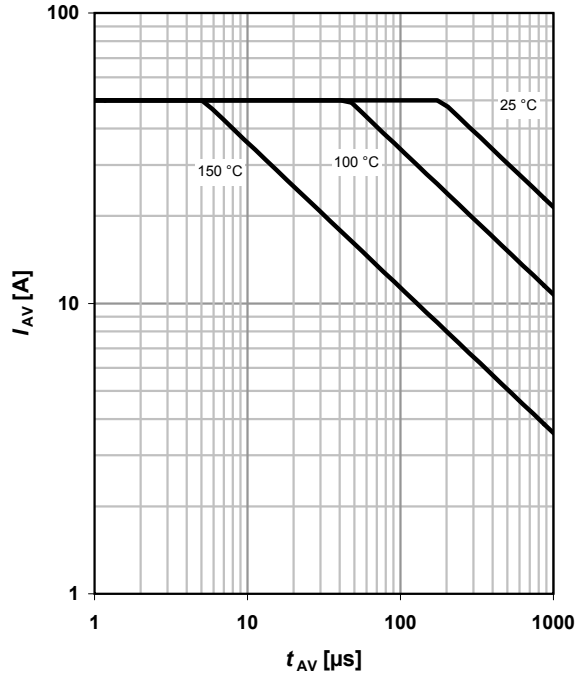
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

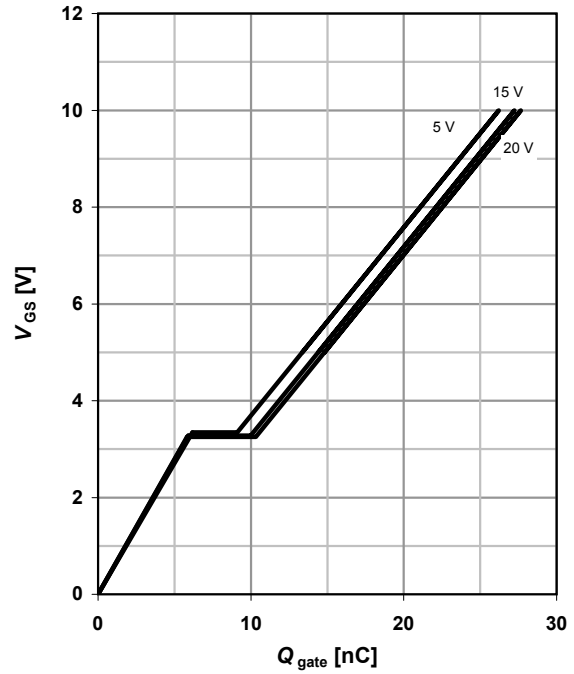
parameter: $T_{j(start)}$



14 Typ. gate charge

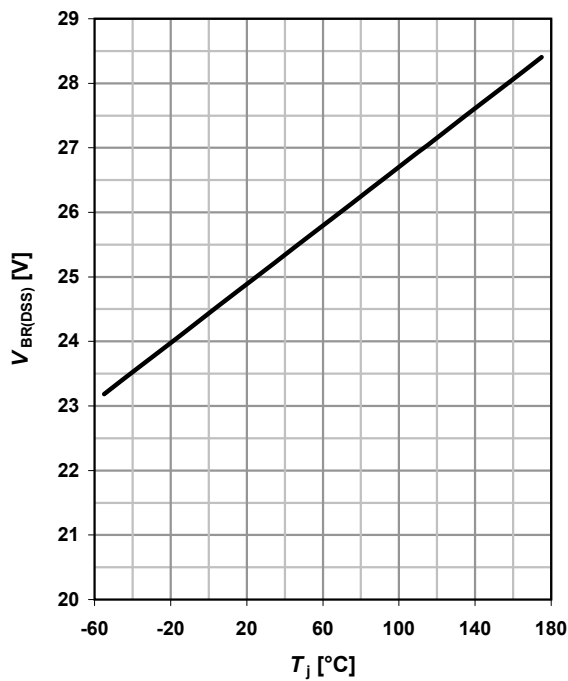
$V_{GS}=f(Q_{gate}); I_D=25 \text{ A pulsed}$

parameter: V_{DD}

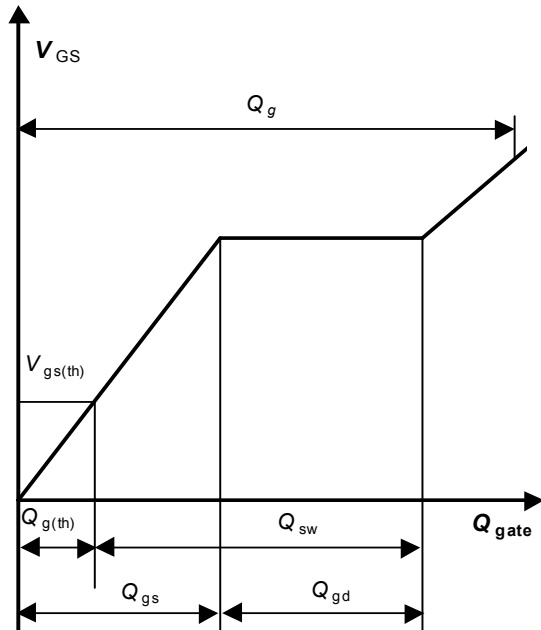


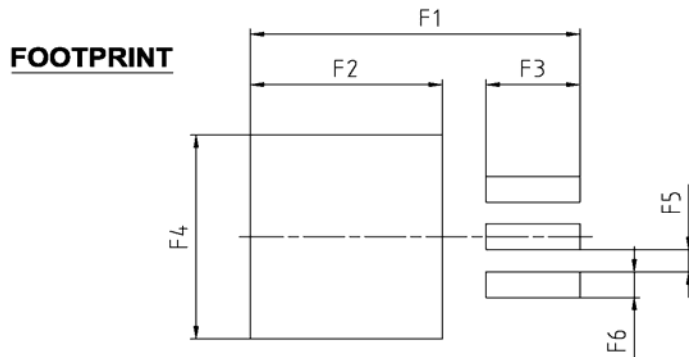
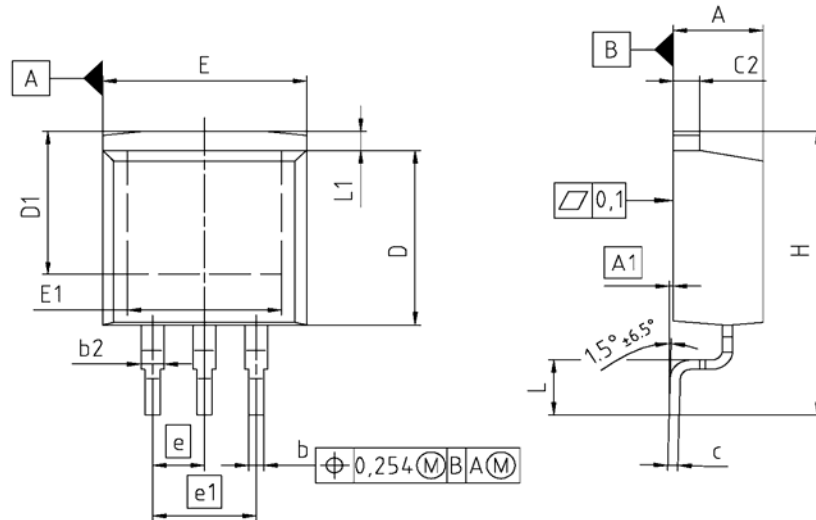
15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms



Package Outline
PG-TO263-3-2


| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|--------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.300 | 4.572 | 0.169 | 0.180 |
| A1 | 0.000 | 0.254 | 0.000 | 0.010 |
| b | 0.650 | 0.850 | 0.026 | 0.033 |
| b2 | 0.950 | 1.321 | 0.037 | 0.052 |
| c | 0.330 | 0.650 | 0.013 | 0.026 |
| c2 | 0.170 | 1.400 | 0.046 | 0.055 |
| D | 8.509 | 9.450 | 0.335 | 0.372 |
| D1 | 7.100 | - | 0.280 | - |
| E | 9.800 | 10.312 | 0.386 | 0.406 |
| E1 | 6.500 | - | 0.256 | - |
| e | 2.540 | | 0.100 | |
| e1 | 5.080 | | 0.200 | |
| N | 3 | | 3 | |
| H | 14.605 | 15.875 | 0.575 | 0.625 |
| L | 2.200 | 3.000 | 0.087 | 0.118 |
| L1 | - | 1.600 | - | 0.063 |
| F1 | 16.050 | 16.250 | 0.632 | 0.640 |
| F2 | 9.300 | 9.500 | 0.366 | 0.374 |
| F3 | 4.500 | 4.700 | 0.177 | 0.185 |
| F4 | 10.700 | 10.900 | 0.421 | 0.429 |
| F5 | 1.250 | 1.450 | 0.049 | 0.057 |
| F6 | 1.100 | 1.300 | 0.043 | 0.051 |

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