Mars MA3 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars MA3 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mars MA3 SoC module.

Summary

This document first gives an overview of the Mars MA3 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-MA3	Mars MA3 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-442-001	06	16.02.2021

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	16.03.2017
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Approved by	DIUN	Manager, BU SP	16.02.2021

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Document History

Version	Date	Author	Comment
06	16.02.2021	DIUN	Cleaned-up product variants, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
05	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, Linux how-to guide, JTAG interface, corrected EEPROM map, other style updates
04	28.08.2018	DIUN	Corrected description of SDIO issue, removed unused article numbers
03	17.08.2018	DIUN	Updated known issues and added corresponding article numbers
02	20.03.2018	DIUN	Updated for revision 2, corrected EEPROM map
01	19.05.2017	DIUN	Version 01, preliminary

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mars MA3 SoC module combines the Altera Cyclone® V ARM® processor-based SoC (System-on-Chip) device with fast DDR3L SDRAM, USB 2.0 On-The-Go PHY, Gigabit Ethernet, Fast Ethernet, eMMC flash, PCIe® Gen1 ×2, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The SO-DIMM form factor allows space-saving hardware designs and quick and simple integration of the module into the target application.

The use of the Mars MA3 SoC module, in contrast to building a custom SoC hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product.

Together with Mars base boards, the Mars MA3 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [15] is available for the Mars MA3 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mars MA3 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars MA3 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars MA3 SoC module.

1.1.5 Safety Recommendations and Warnings

Mars modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mars MA3 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

Warning!

Use the Mars MA3 SoC module only with base boards designed for the Enclustra Mars module family. Inserting the Mars MA3 SoC module into a SO-DIMM connector designed for memory (e.g. a computer main board) may damage the module and the carrier board.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars MA3 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Altera Cyclone V SOC 5CSEBA5U23C8N/5CSXFC6C6U23I7N
  - ARM dual-core Cortex A9
  - Altera Cyclone V 28 nm FPGA fabric
- Up to 104 user I/Os up to 3.3 V
  - 16 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART) from which 14 pins shared with FPGA I/Os
  - 76 FPGA I/Os (single-ended or differential)
  - 12 MGT signals (clock and data) for 5CSX devices or 4 additional FPGA I/Os for 5CSE devices
- *5CSX devices*: 2 MGTs @ 3.125 Gbit/sec and 2 reference input clock differential pairs
- *5CSX devices*: PCIe Gen1 ×2 (Altera PCIe hardened IP block)
- 1 GB DDR3L SDRAM
- 64 MB quad SPI flash
- 16 GB eMMC flash
- Gigabit Ethernet
- Fast Ethernet
- USB 2.0 On-The-Go (OTG)
- CAN, UART, SPI, I2C, SDIO/MMC
- Real-time clock
- SO-DIMM form factor (30 × 67.6 mm, 200 pins)
- The module can be operated using a single 3.3 V supply voltage

1.3 Deliverables

- Mars MA3 SoC module
- Mars MA3 SoC module documentation, available via download:
  - Mars MA3 SoC Module User Manual (this document)
  - Mars MA3 SoC Module Reference Design [2]
  - Mars MA3 SoC Module IO Net Length Excel Sheet [3]

- Mars MA3 SoC Module FPGA Pinout Excel Sheet [4]
- Mars MA3 SoC Module User Schematics (PDF) [5]
- Mars MA3 SoC Module Known Issues and Changes [6]
- Mars MA3 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
- Mars MA3 SoC Module 3D Model (PDF) [8]
- Mars MA3 SoC Module STEP 3D Model [9]
- Mercury Mars Module Pin Connection Guidelines [10]
- Mars Master Pinout [11]
- Mars Heatsink Mounting Guide [18]
- Enclustra Build Environment [15] (Linux build environment; refer to Section 1.4.2 for details)
- Enclustra Build Environment How-To Guide [16]

1.4 Accessories

1.4.1 Reference Design

The Mars MA3 SoC module reference design features an example configuration for the Cyclone V SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from the Enclustra download page [2].

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [15] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader/bootloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [16] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mars modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

1.4.4 Mars ST3 Base Board

- Mars 200-pin SO-DIMM socket
- MIPI D-PHY connector (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- USB 3.0 host connector
- RJ45 Ethernet connector
- 2 × 40-pin GPIO connector (Anios)
- 1 × 8-pin and 1 × 4-pin GPIO connectors (Pmod™ compatible pinout)
- FTDI USB 2.0 device controller with micro USB device connector

- microSD card holder
- User LEDs
- Integrated Xilinx compatible JTAG adapter
- Support for low I/O voltages (1.2 V, 1.8 V)
- Single 12 V DC supply voltage
- Form factor: 100 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.5 Mars EB1 Base Board

- Mars 200-pin SO-DIMM socket
- 2 × Mini Camera Link connectors (requires FPGA support)
- HDMI 1.3 connector (requires FPGA support)
- 40-pin GPIO connector (Anios)
- 3 × 12-pin GPIO connector (two of the connectors with Pmod™ compatible pinout)
- RJ45 Ethernet connector
- USB 2.0 A host connector
- Micro USB 2.0 device connector (shared)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- Various switches and LEDs
- Integrated Xilinx compatible JTAG adapter
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 120 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.6 Mars PM3 Base Board

Warning!

Please note that there are limitations when using the Mars MA3 SoC module in combination with the Mars PM3 base board.

By default, on power-up, the Mars MA3 SoC module equipped on the Mars PM3 base board will try to boot from the QSPI flash (even with SD card boot settings), but after pressing the POR button the module will boot as expected from the device configured by the boot selection pins. QSPI flash boot works normally.

If the SD card boot issue affects the target application, it is recommended to use a different Enclustra base board.

- Mars 200-pin SO-DIMM socket
- FMC LPC (Low Pin Count) connector (72 I/Os)
- 40-pin GPIO connector (optional, shared with FMC I/Os)
- RJ45 Gigabit Ethernet connector
- Mini HDMI connector for PCIe and LVDS applications (module dependent)
- Cypress FX3 USB 3.0 device controller (16-bit Slave-FIFO interface or 32-bit Slave-FIFO interface shared with FMC I/Os)
- USB 3.0 B device connector
- USB 2.0 A host connector
- Micro USB 2.0 B device connector with FTDI USB device controller
- Battery holder for the real-time clock
- microSD card holder

- Fan connector, various switches and LEDs
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 100 × 72 mm (pico-ITX)

Please note that the available features depend on the equipped Mars module type.

1.5 Intel Tool Support

The SoC devices equipped on the Mars MA3 SoC module are supported by the Quartus Prime Lite Edition (or Quartus II Web Edition, for older software versions), which is available free of charge. Please contact Intel for further information.

2 Module Description

2.1 Block Diagram

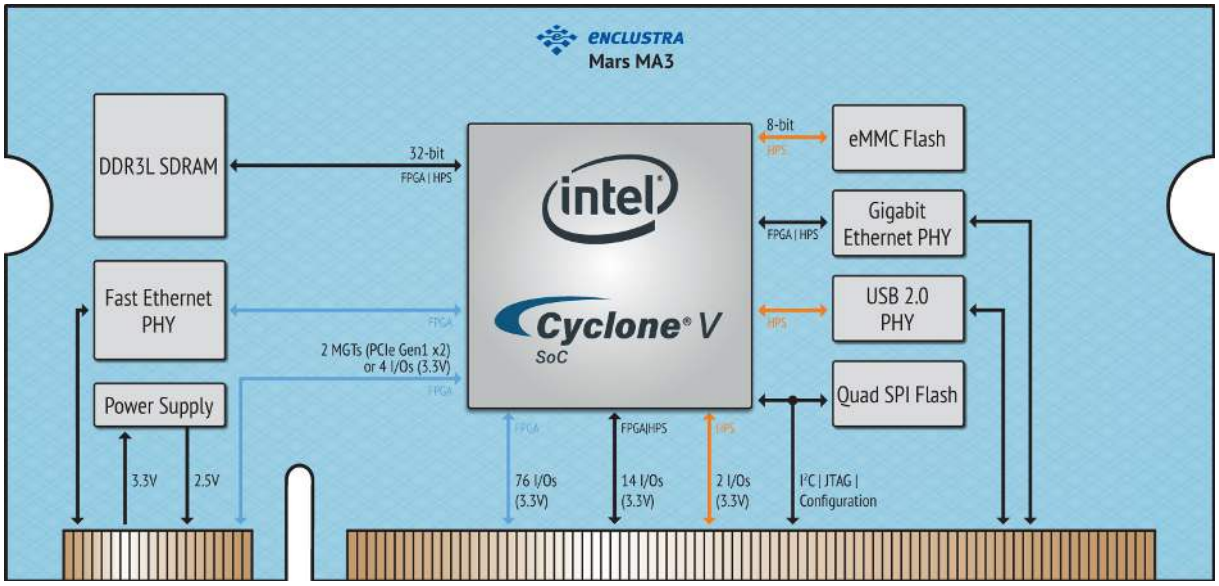

Figure 1: Hardware Block Diagram

The main component of the Mars MA3 SoC module is the Intel Cyclone V SoC device. Most of its I/O pins are connected to the Mars module connectors, making 92 regular user I/Os available to the user. Further, on modules equipped with 5CSX devices, two multi-gigabit transceivers with support for PCIe Gen1 ×2 are available on the module connector. On Mars MA3 SoC modules equipped with 5CSE devices, these transceivers are not available, but instead 4 additional I/Os are available.

The SoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mars module connector.

The memory subsystem is built from a 16 GB eMMC flash, a 64 MB QSPI flash and 1 GB DDR3L SDRAM in the standard configuration.

Further, the module is equipped with a Gigabit Ethernet PHY, a Fast Ethernet PHY and a USB 2.0 OTG PHY, making it ideal for communication applications.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 50 MHz crystal oscillator.

The module can be operated using a single input supply of 3.3 V DC. All other necessary supply voltages are generated on-board. Some of these voltages are available on the Mars module connector to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	SoC	DDR3L SDRAM	PCI Express	Temperature Range
MA-MA3-A5-8C-D10	5CSEBA5U23C8N	1 GB	✗	0 to +70° C
MA-MA3-C6-7I-D10	5CSXFC6C6U23I7N	1 GB	✓	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

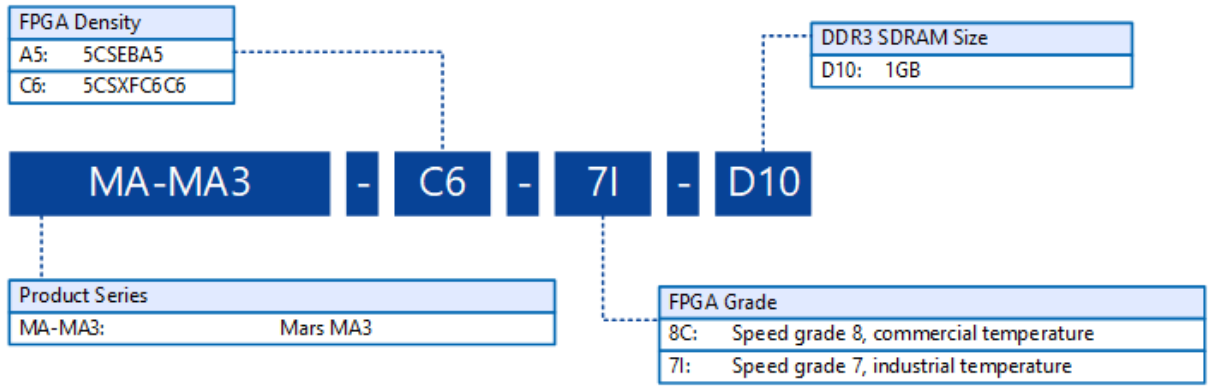

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

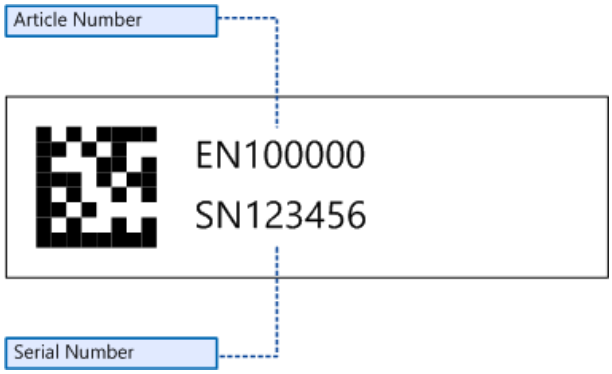

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars MA3 SoC Module Known Issues and Changes document [6].

Article Number	Article Code
EN101854	MA-MA3-C6-7I-D10-R1
EN101767	MA-MA3-A5-8C-D10-R1
EN102043	MA-MA3-A4-8C-D10-R2
EN102044	MA-MA3-A5-7I-D10-R2
EN102045	MA-MA3-C5-8C-D10-R2
EN102046	MA-MA3-C6-7I-D10-R2

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

Figure 4: Module Top View

2.4.2 Bottom View

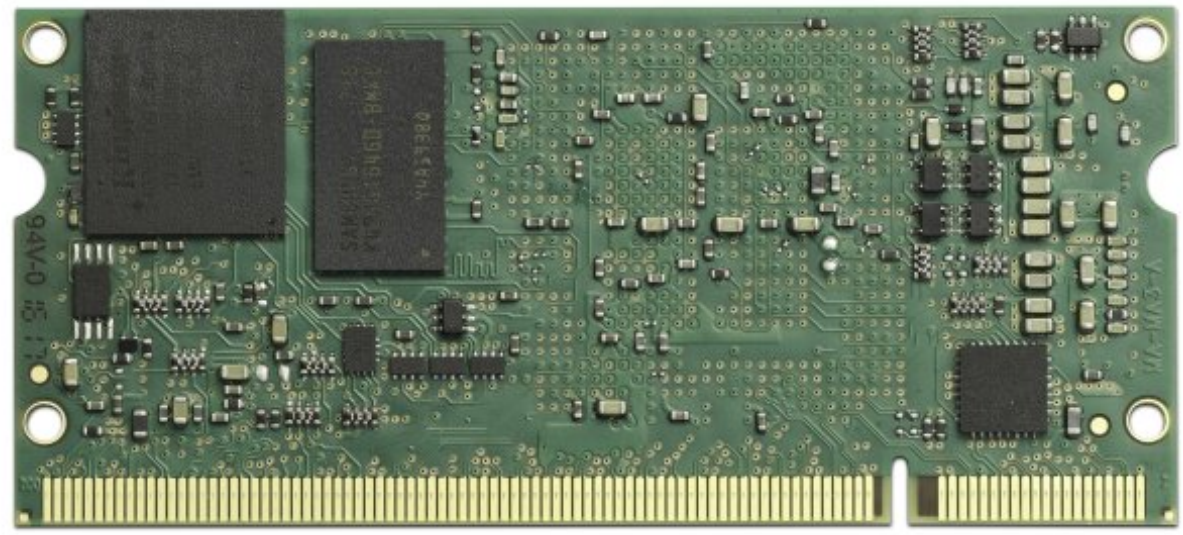

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

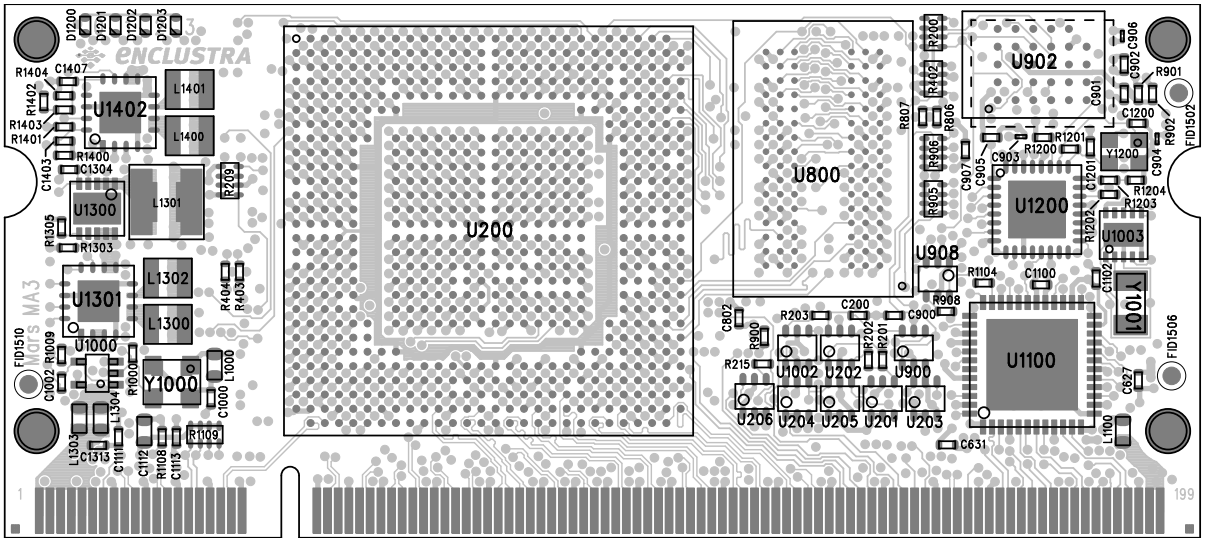

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

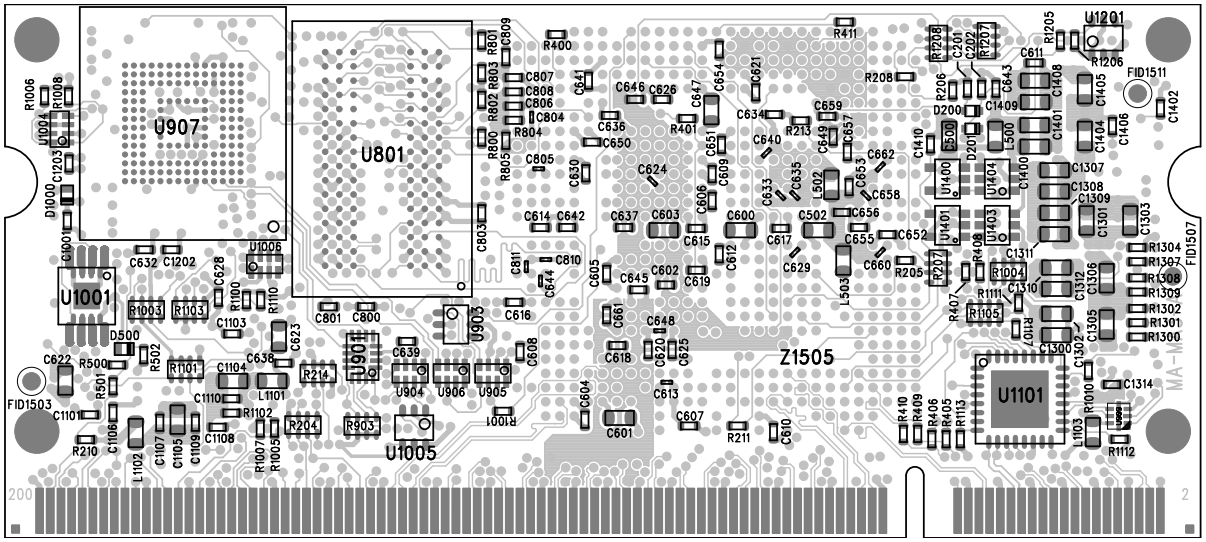

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

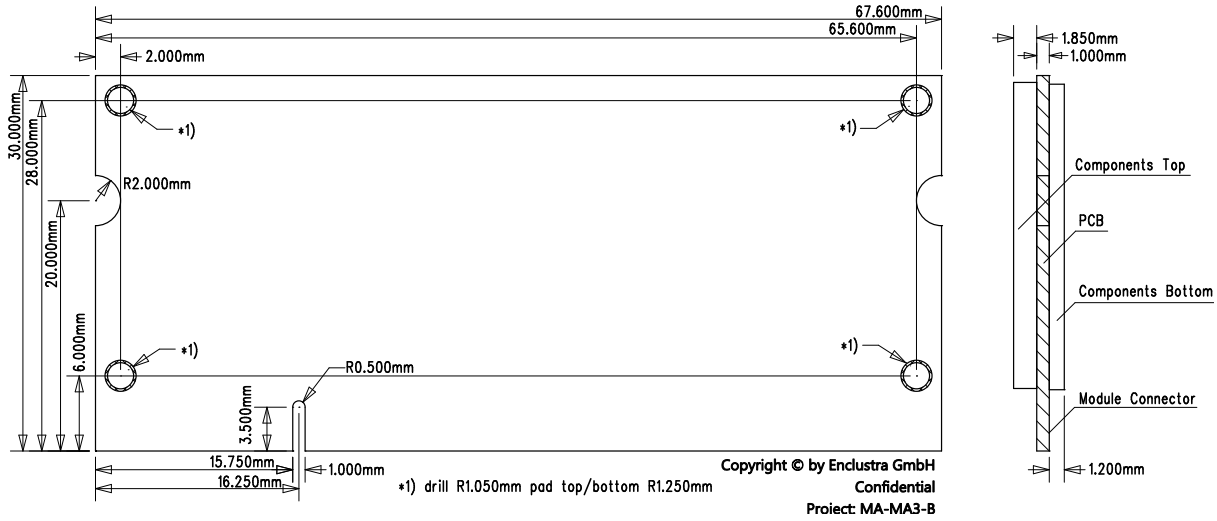

Figure 8: Module Footprint - Top View

The footprint of the module connector is available for different PCB design tools (Altium, Eagle, Orcad, PADS) [7].

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mars MA3 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	67.6 × 30 mm
Component height top	1.85 mm
Component height bottom	1.2 mm
Weight	9 g

Table 3: Mechanical Data

2.8 Module Connector

The Mars MA3 SoC module fits into a 200-pin DDR2 SO-DIMM (1.8 V) socket. Up to four M2 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mars Master Pinout Excel Sheet [11]. The connector to be mounted on the base board is available in different heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Height	Type	Description	Max component height under the module
4.0 mm	TE 292406-4	DDR2-SODIMM, 1.8 V	0 mm
5.2 mm	TE 1565917-4	DDR2-SODIMM, 1.8 V	1 mm
6.5 mm	TE 5-1746530-4	DDR2-SODIMM, 1.8 V	2 mm
8.0 mm	TE 1827341-4	DDR2-SODIMM, 1.8 V	4 mm

Table 4: Module Connector Types

2.9 User I/O

2.9.1 Pinout

Information on the Mars MA3 SoC module pinout can be found in the Enclustra Mars Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mars MA3 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_<FUNCTION>_<PIN_NAME>_<PACKAGE_PIN>_<POLARITY>

For example, IO_B3B_TX_B33_AF7_P is located on pin AF7 of I/O bank 3B, and when used in a differential pair it is a transmit pin and has positive polarity.

For the signal lines shared between FPGA logic and Hard Processing System (HPS), the naming convention is:
HPS_<HPS_FUNCTION>_<FUNCTION>_B<BANK>_<PACKAGE_PIN>

For example, HPS_SDCLK_RX_B3A_U10 is connected to FPGA pin U10 and in parallel to an HPS pin that may have the function of SDIO clock.

Please note that for the shared pins only one of the driving pins (FPGA pin, HPS pin) may be active.

The clock capable pins are marked with "CLK" in the signal name. For details on their function and usage, please refer to the Intel documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the signal name as differential inputs and only pins marked with "TX" as differential outputs. The I/O pins marked with "CLK" are receive-only differential signals and can be used as dedicated clock differential inputs. All pins can be used as single-ended inputs or outputs.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
HPS_<HPS_FUNCTION>_B3A_RX<...>	8	4	In	In/Out	3A
HPS_<HPS_FUNCTION>_B3A_TX<...>	6	3	Out	In/Out	3A
IO_B3B_RX<...>	12	6	In	In/Out	3B
IO_B3B_TX<...>	14	7	Out	In/Out	3B
IO_B3B_CLK<...>	2	1	In	In/Out	3B
IO_B4A_RX<...>	22	11	In	In/Out	4A
IO_B4A_CLK<...>	4	2	In	In/Out	4A
IO_B4A_TX<...>	22	11	Out	In/Out	4A
Total	**90**	**45**	-	-	-

Table 5: User I/Os

On Mars MA3 SoC modules equipped with 5CSE SoC devices there are no transceivers available, hence the MGT_RX and MGT_TX signals are not used.

On these devices there are 4 additional signals available on the module connector:

- 1 pair IO_B3B_CLK<..> (or 2 single-ended I/Os) located on connector pins 4 and 6
- 1 pair IO_B3B_TX<...> (or 2 single-ended I/Os) located on connector pins 10 and 12

The naming convention for the four I/Os that are rerouted depending on the type of equipped SoC device is:
MGT_REFCLK<0/1>_B<BANK_5CSE>_<FUNCTION_5CSE>_<PIN_NAME_5CSE>_<POLARITY>

On the 5CSX devices, these pins are MGT reference clock differential pairs.

2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mars boards they may have a specific role).

Table 6 lists the I/O pin exceptions on the Mars MA3 SoC module.

I/O Name	Module Connector Pin	Description
HPS_GPIO59_MISO_B3A_TX_AA4	148	Connected via a 47 kΩ resistor to FPGA_PERST# (FPGA pin W15) for PCIe PERST# connection implementation

Table 6: I/O Pin Exceptions

The PERST# connection to module connector pin 148 is implemented for future support of PCIe interface on Enclustra Mars base boards.

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mars MA3 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mars MA3 SoC module. Please use the information provided in the Mars MA3 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the signal name as differential inputs and only pins marked with "TX" as differential outputs. All pins can be used as single-ended inputs or outputs.

Warning!

Check Mars MA3 SoC module pinout with Quartus before producing your own base board hardware, to make sure that all pins are used according to the correct direction.

2.9.4 I/O Banks

Table 7 describes the main attributes of the FPGA and HPS I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
MGT Bank L0	Module connector	1.1 V	-
MGT Bank L1	Module connector	1.1 V	-
Bank 3A	Module connector, Fast Ethernet PHY	User selectable VCC_CFG_HPS_B3A	0 V
Bank 3B	Module connector	User selectable VCC_IO_B3B_B4A	0 V
Bank 4A	Module connector, Fast Ethernet PHY, I2C	User selectable VCC_IO_B3B_B4A	0 V
Bank 5A	Gigabit and Fast Ethernet PHYs	1.8 V	0 V
Bank 8A	Gigabit and Fast Ethernet PHYs	1.8 V	0 V
HPS Bank 6A	DDR3L SDRAM	1.35 V	0.68 V

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
HPS Bank 6B	DDR3L SDRAM	1.35 V	0.68 V
HPS Bank 7A	Configuration, I2C, LEDs, module connector	User selectable VCC_CFG_HPS_B3A	0 V
HPS Bank 7B	Gigabit and Fast Ethernet PHYs, QSPI flash	1.8 V	0 V
HPS Bank 7C	Gigabit and Fast Ethernet PHYs, eMMC flash, module connector	1.8 V	0 V
HPS Bank 7D	USB PHY, Gigabit Ethernet PHY	1.8 V	0 V

Table 7: I/O Banks

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mars base boards and modules, it is recommended to use a single I/O voltage.

Signal Name	SoC Pins	Supported Voltages	Connector Pins
VCC_CFG_HPS_B3A	VCCIO3A, VCCIO7A_HPS	1.8 V, 2.5 V - 3.3 V ±5%	137, 146
VCC_IO_B3B_B4A	VCCIO3B, VCCIO4A	1.2 V[1,2] - 3.3 V ±5%	53, 62, 73, 82, 117, 126

Table 8: VCC_IO Pins

Note that the VCCPD (I/O pre-driver power supply) for each bank is set automatically to 2.5 V (if the corresponding VCCIO is less than or equal to 2.5 V) or to VCCIO (if the corresponding VCCIO is higher or equal to 3.0 V).

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mars MA3 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mars MA3 SoC module.

[1] I2C bus access from the FPGA side is possible only when VCC_IO_B3B_B4A is 1.8 V or higher.
[2] Fast Ethernet MDIO interface is available when VCC_IO_B3B_B4A is 1.8 V or higher.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 9 illustrates the VCC_IO power requirements.

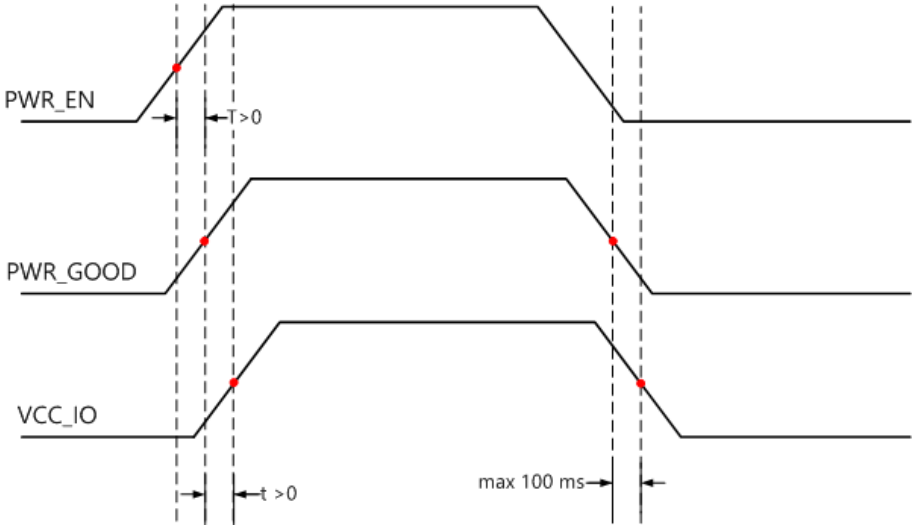

Figure 9: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mars MA3 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the name as differential inputs.

Single-Ended Outputs

There are no series termination resistors on the Mars MA3 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 HPS I/O Pins

Table 9 gives an overview over the HPS pin connections on the Mars MA3 SoC module. Only the pins marked with "user functionality" are available on the module connector.

The suggested functions below are for reference only - always verify your HPS pinout with the Intel device handbook.

HPS_GPIO	Function	Connection
0-8, 10-13	USB 2.0	USB 2.0 OTG PHY
9	Gigabit Ethernet PHY reset (output, active-low)	Gigabit Ethernet PHY
14-27	Gigabit Ethernet	Gigabit Ethernet PHY (RGMII)
28	HPS boot select 2	Boot mode selection
29-34	QSPI flash	QSPI flash
35	Fast Ethernet reset	Fast Ethernet PHY
36, 38-39, 45-47	SD card/eMMC/user functionality	Module connector/eMMC flash
37	Fast Ethernet interrupt/power down	Fast Ethernet PHY
40-43	eMMC	eMMC flash
44	Gigabit Ethernet PHY interrupt (input, active-low)	Gigabit Ethernet PHY
48-51	LEDs (connected in parallel with FPGA I/Os)	On-board LEDs
52	RTC interrupt (input, active-low)	RTC
53	eMMC enable signal (output, active-low)	Configuration multiplexers and level shifters
54-56	I2C	On-board I2C bus and module connector via level shifter
57-60	SPI/user functionality	Module connector
61-62	CAN/user functionality	Module connector
63 64	UART1 RX[3]/user functionality UART1 TX[3]/user functionality	Module connector
65 66	UART0 RX[3]/user functionality UART0 TX[3]/user functionality	Module connector

Table 9: HPS Pin Connections

2.10 Multi-Gigabit Transceiver (MGT)

On Mars MA3 SoC modules equipped with 5CSX SoC devices there are two Multi-Gigabit transceivers and two reference input clock differential pairs routed directly to the module connector.

[3]UART RX is an SoC input; UART TX is an SoC output.

On Mars MA3 SoC modules equipped with 5CSE SoC devices there are no MGT signals available. Instead, there are 4 additional signals available on the module connector. Refer to Section 2.9.1 and to the Mars MA3 SoC Module User Schematics [5] for details.

The transceivers on the SoC device support a data rate of 3.125 Gbit/sec.

The naming convention for the MGT I/Os is:
MGT_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGT_RX0_AF2_P is located on pin AF2, it is a receive pin and it has positive polarity.

The naming convention for the four I/Os that are have different functions depending on the type of equipped SoC device is described in Section 2.9.1.

Warning!

The maximum data rate on the MGT lines on the Mars MA3 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

Warning!

No AC coupling capacitors are placed on the Mars MA3 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mars MA3 SoC module uses a 3.3 - 5.0 V DC power input for generating the on-board supply voltages (1.1 V, 1.2 V, 1.35 V, 1.8 V, 2.5 V). Some of these internally-generated voltages are accessible on the module connector. In addition, a separate 3.3 V power input is used to supply peripherals, such as the Ethernet PHY, USB PHY, QSPI flash, eMMC flash, RTC, EEPROM and LEDs.

The Mars MA3 SoC module can be powered using a single power supply. In this case, the two voltage supply inputs VCC_MOD and VCC_3V3 must be connected together to a 3.3 V supply. Please refer to Section 2.11.3 for details on the voltage supply inputs.

Table 10 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V1	1.1 V	3 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	1 A	VCC_MOD	Yes	Yes
VCC_1V35	1.35 V	1 A	VCC_MOD	Yes	Yes
VCC_1V8	1.8 V	1.5 A	VCC_MOD	Yes	Yes
VCC_2V5	2.5 V	1.5 A	VCC_MOD	Yes	Yes

Table 10: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.11.2 Power Enable/Power Good

The Mars MA3 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.1 V, 1.2 V, 1.35 V, 1.8 V, and 2.5 V, leaving the SoC device and the DDR3 SDRAM unpowered.

The PWR_EN input is pulled to VCC_3V3 on the Mars MA3 SoC module with a 4.7 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mars MA3 SoC module with a 4.7 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	40	0 V: Module supply not ok 3.3 V: Module supply ok

Table 11: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mars MA3 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 9.

2.11.3 Voltage Supply Inputs

Table 12 describes the power supply inputs on the Mars MA3 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	1, 3, 5, 7, 9, 11	3.3 - 5.0 V ±10%	Supply for the 1.1 V, 1.2 V, 1.35 V, 1.8 V, and 2.5 V voltage regulators. The input current is rated at 1.8 A (0.3 A per connector pin).
VCC_3V3	197, 199	3.3 V ±5%	Supply for Ethernet PHY, USB PHY, QSPI flash, eMMC flash, RTC, EEPROM and LEDs
VCC_BAT	200	2.0 - 3.6 V	Battery voltage for the RTC and SoC encryption key storage

Table 12: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 13 presents the supply voltages generated on the Mars MA3 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[4]
VCC_1V1	42	1.0 V ±5%	0.3 A
VCC_1V35	41	1.35 V ±5%	0.3 A
VCC_2V5	89, 101	2.5 V ±5%	0.6 A (and max 0.3 A per connector pin)
VCC_1V8	94, 106	1.8 V ±5%	0.6 A (and max 0.3 A per connector pin)

Table 13: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mars MA3 SoC module.

2.11.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Intel PowerPlay Early Power Estimators (EPE) and Power Analyzer available on the Intel website.

[4] The maximum available output current depends on your SoC design. See sections 2.11.1 and 2.11.5 for details.

2.11.6 Heat Dissipation

High performance devices like the Intel Cyclone V SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mars modules an Enclustra heat sink is available for purchase along with the product. It represents an optimal solution to cool the Mars MA3 SoC module - it is low profile (less than 7 mm tall) and covers the whole module surface. It comes with a gap pad for the SoC device and four screws to attach it to the module PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, mounting material).

Table 14 lists the heat sink and thermal pad part numbers that are compatible with the Mars MA3 SoC module. Details on the Mars heat sink kit can be found in the Mars Heatsink Mounting Guide [18].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mars MA3	672-pin UBGA [25]	HS-MA2	ATS-52230G-C1-R0	TG-A6200-25-25-1

Table 14: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module in used in environments subject to vibrations, a heat sink with mounting screws or clips may be required for optimal fixation.

Warning!

Depending on the user application, the Mars MA3 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mars MA3 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 15 presents the VMON pins on the Mars MA3 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V2	198	VCC_1V2	1.2 V on-board voltage (default)/SoC battery voltage (assembly option)

Table 15: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 50 MHz oscillator is used for the Mars MA3 SoC module clock generation. The 50 MHz clock is fed to the HPS and to a clock divider. The 25 MHz divided clock is then fed to the Ethernet PHY and FPGA logic.

Signal Name	Frequency	Destination	Remark
CLK_HPS1	50 MHz	HPS_CLK1	HPS clock 1
CLK_FPGA	50 MHz[5]	IO_RX_T1P_CLK7P_8A (pin D12)	FPGA clock
CLK_ETH1	50 MHz	Fast Ethernet PHY	-
CLK_ETH0	25 MHz	Gigabit Ethernet PHY	-

Table 16: Module Clock Resources

2.13 Reset

The cold reset signal (POR) and the HPS warm reset signal (RST) of the SoC device are available on the module connector.

Pulling HPS_POR# low resets the SoC device and the flash devices. Further, the CONFIG# pin is pulled low to re-trigger the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling HPS_RST# low resets the SoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the HPS_NPOR and HPS_NRST signals refer to the Intel documentation.

Table 17 presents the available reset signals. Both signals, HPS_POR# and HPS_RST#, have on-board 4.7 kΩ pull-up resistors to VCC_CFG_HPS_B3A.

Signal Name	Connector Pin	FPGA Pin Type	Description
HPS_POR#	196	HPS_NPOR	Cold reset
HPS_RST#	192	HPS_NRST	Warm reset

Table 17: Reset Resources

Please note that HPS_POR# is automatically asserted if PWR_GOOD is low.

[5] On revision 1 modules, the frequency of the clock signal available on CLK_FPGA is 25 MHz, instead of 50 MHz.

2.14 LEDs

The four LEDs on the Mars MA3 SoC module are connected to the FPGA logic and the HPS in parallel; it is recommended to drive the FPGA pins to a high impedance state before driving the HPS pins and vice versa.

Signal Name	HPS GPIO	FPGA Pin	Remarks
LED0#	48	AH12	User function/active-low
LED1#	49	AF18	User function/active-low
LED2#	50	AG21	User function/active-low
LED3#	51	AH21	User function/active-low

Table 18: LEDs

2.15 DDR3L SDRAM

There is a single DDR3 SDRAM channel on the Mars MA3 SoC module attached directly to the HPS side and is available only as a shared resource to the FPGA side.

The DDR3L SDRAM is connected to HPS I/O banks 6A and 6B, and it is always operated at 1.35 V (low power mode). Two 16-bit memory chips are used to build a 32-bit wide memory.

The maximum memory bandwidth on the Mars MA3 SoC module is:
800 Mbit/sec × 32 bit = 3200 MB/sec

2.15.1 DDR3L SDRAM Type

Table 19 describes the memory availability and configuration on the Mars MA3 SoC module.

Module	SDRAM Type	Density	Configuration	Manufact.
MA-MA3-D10 (commercial)	NT5CC256M16CP-DI	4 Gbit	256 M × 16 bit	Nanya
MA-MA3-D10 (industrial)	NT5CC256M16CP-DII	4 Gbit	256 M × 16 bit	Nanya
MA-MA3-D10 (industrial)	NT5CC256M16ER-EKI	4 Gbit	256 M × 16 bit	Nanya
MA-MA3-D10 (industrial)	K4B4G1646D-BMK0	4 Gbit	256 M × 16 bit	Samsung
MA-MA3-D10 (industrial)	K4B4G1646E-BMMA	4 Gbit	256 M × 16 bit	Samsung
MA-MA3-D10 (industrial)	H5TC4G63CFR-RDI	4 Gbit	256 M × 16 bit	SK Hynix

Table 19: DDR3L SDRAM Types

Warning!

Other DDR3L memory devices may be equipped in future revisions of the Mars MA3 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Please refer to the Mars MA3 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3L SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data signals on the Mars MA3 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.15.4 Parameters

Please refer to the Mars MA3 SoC module reference design [2] for DDR3 settings guidelines. The DDR3L SDRAM parameters to be set in Quartus project are presented in Tables 20.

The values given in Table 20 are for reference only. Depending on the equipped memory device on the Mars MA3 SoC module and on the DDR3L SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
SDRAM protocol	DDR3
Memory clock frequency	400 MHz
PHY settings - supply voltage	1.35 V DDR3L
Memory device speed grade	800 MHz
Total interface width	32 bit
Number of chip select/depth expansion	1
Number of clocks	1
Row bits	15
Column bits	10
Bank bits	3
Memory CAS latency setting	6
Output drive strength setting	RZQ/6
ODT Rtt nominal value	RZQ/6
Memory write CAS latency setting	5
Dynamic ODT (Rtt_WR) value	RZQ/4
tRAS	37.5 ns
tRCD	15 ns
tRP	15 ns
tREFI	7.8 us
tRFC	260.0 ns
tWR	15.0 ns
tWTR	4 cycles
tFAW	40.0 ns
tRRD	10 ns
tRTP	10 ns

Table 20: DDR3L SDRAM Parameters

2.16 QSPI Flash

The QSPI flash can be used to boot the HPS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 QSPI Flash Type

Table 21 describes the memory availability and configuration on the Mars MA3 SoC module.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 21: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mars MA3 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.16.2 Signal Description

The QSPI flash is connected to the HPS pins 29-34 and to the FPGA SPI configuration port. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the SoC and the flash device.

2.16.3 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [26], [27].

2.17 SD Card

An SD card can be connected to the HPS pins or to the FPGA bank 3A pins available on the module connector. Connecting the card to the HPS pins allows the Mars MA3 SoC module to boot from the SD card, as well as data access after booting. Information on SD card boot is available in Section 3.6.

The SDIO interface may also be configured to the FPGA pins in bank 3A, but this configuration does not allow the user to boot from the SD card. Refer to Section 3.2 for details on the available boot modes and corresponding connections.

When booting from the QSPI flash, the access to the SD card is possible via FPGA or HPS pins, depending on the EMMC_EN# signal and on how the SDIO controller is mapped in Quartus.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_HPS_B3A, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

On modules revision 1 and 2, booting from SD card when VCC_CFG_HPS_B3A is 1.8 V is not fully supported, due to the level shifters that require a voltage of minimum 2.3 V on VCCB pin. Enclustra tests have shown that the SoC device can boot at 1.8 V, but this voltage is out of the recommended range for the level shifter. Please refer to the Mars MA3 SoC Module Known Issues and Changes document [6] for details on this issue and its solution.

2.17.1 Signal Description

Table 22 describes the SD card pin mappings to the HPS, respectively FPGA pins.

HPS Pin (SD Card Boot)	FPGA Pin (SD Card Access, No Boot)	SD Card Signal	Module Connector Pin
36	V10	CMD	141
38	W8	D0	143
39	Y8	D1	145
45	U10	CLK	139
46	U9	D2	149
47	T8	D3	151

Table 22: SD Card Signals

2.18 eMMC Flash

The eMMC flash can be used to boot the HPS, and to store the FPGA bitstream, ARM application code and other user data.

2.18.1 eMMC Flash Type

Table 23 describes the memory availability and configuration on the Mars MA3 SoC module.

Flash Type	Size	Manufacturer
H26M52208FPRI	16 GB	SK Hynix
EMMC16G-W525-X01U	16 GB	Kingston
EMMC16G-IB29-PZ90	16 GB	Kingston

Table 23: eMMC Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mars MA3 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.18.2 Signal Description

The eMMC flash signals are connected to the HPS pins 36, 38-43, 45-47. Some of the pins are multiplexed between eMMC and SD interfaces. The clock signal is equipped with a 10 kΩ pull-up resistor. The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data lines have 47 kΩ pull-up resistors to 1.8 V.

The eMMC flash clock is interrupted when the eMMC flash enable signal, EMMC_EN#, is inactive (for example, when booting from SD card).

2.19 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mars MA3 SoC module, connected to the HPS and FPGA logic via RGMII interface.

2.19.1 Ethernet PHY Type

Table 24 describes the equipped Ethernet PHY device type on the Mars MA3 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 24: Gigabit Ethernet PHY Type

2.19.2 Signal Description

The RGMII interface is connected to HPS pins for use with the hard macro MAC, and in parallel to FPGA banks 5A and 8A pins for use with the FPGA logic. The reset pin has a pull-down resistor and needs to be driven high to release the PHY from reset. A detailed list of the HPS connections is found in Section 2.9.7.

The Gigabit Ethernet connections are presented in Table 25. All listed pins are operated at 1.8 V.

Signal Name	HPS Pin	FPGA Pin
ETH0_RESET#	HPS9	-
ETH0_INT#	HPS44	-
ETH0_MDC[6]	HPS21	-
ETH0_MDIO[6]	HPS20	-
ETH0_RX_CLK	HPS24	E11
ETH0_RX_CTL	HPS22	AE25
ETH0_RXD0	HPS19	AA20
ETH0_RXD1	HPS25	Y19
ETH0_RXD2	HPS26	Y17
ETH0_RXD3	HPS27	Y18
ETH0_TX_CLK	HPS14	V16
ETH0_TX_CTL	HPS23	AB23
ETH0_TXD0	HPS15	AC24
ETH0_TXD1	HPS16	AE26
ETH0_TXD2	HPS17	AA24
ETH0_TXD3	HPS18	AA23

Table 25: Gigabit Ethernet Signal Description

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3.

The MDIO interface is connected to the HPS pins 20-21.

On revision 1 modules, the MDIO interface is shared between the Gigabit Ethernet PHY and the Fast Ethernet PHY, allowing the PHYs to be configured individually by using the corresponding addresses.

Starting with revision 2, the MDIO is completely separated between PHYs: HPS pins 20-21 are used for the configuration of the Gigabit Ethernet PHY, while FPGA pins AA18 and AA19 are used for the configuration of the Fast Ethernet PHY.

[6] On revision 1 modules, the MDIO interface is shared between the Gigabit Ethernet PHY and the Fast Ethernet PHY. Starting with revision 2, the MDIO is completely separated between PHYs: the Gigabit Ethernet PHY can be configured from the HPS side, while the Fast Ethernet PHY can be configured from the FPGA logic.

2.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 26.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the patch for the Preloader (SPL) provided in the Mars MA3 SoC module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 26: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.20 Fast Ethernet

A 10/100 Mbit Ethernet PHY is equipped on the Mars MA3 SoC module, connected to FPGA I/Os via RMII interface.

2.20.1 Ethernet PHY Type

Table 27 describes the equipped Ethernet PHY device type on the Mars MA3 SoC module.

PHY Type	Manufacturer	Type
DP83822I	Texas Instruments	10/100 Mbit

Table 27: Fast Ethernet PHY Type

2.20.2 Signal Description

The RMII interface is connected to the FPGA pins in banks 5A and 8A (optionally bank 3A) for use with a soft Ethernet MAC IP core.

A 50 MHz clock is generated by the on-board oscillator and fed to the FPGA (CLK_FPGA signal on pin D12) and to the Fast Ethernet PHY.

On revision 1 modules, the 50 MHz clock for the Fast Ethernet PHY must be supplied via FPGA pin E8, as the clock is not provided by the oscillator. This FPGA pin is not used on the module starting with revision 2.

Some of the RMII signals have pull-up or pull-down resistors for bootstrapping. Starting with revision 2 modules, the bootstrap resistors have been optimized to accommodate the presence of weak the pull resistors in the FPGA, and ensure that the PHY is properly configured regardless of the FPGA programming status. Make sure that any additional resistors on the FPGA side are disabled.

The reset signal of the Fast Ethernet PHY has a pull-down resistor and is connected to HPS GPIO 35. It needs to be driven high to release the PHYs from reset.

The Fast Ethernet interrupt/power down pin is connected to HPS GPIO 37 and has a pull-up resistor.

The Fast Ethernet connections are presented in Table 28. All listed pins are operated at 1.8 V. Details on connections are available in the Mars MA3 SoC Module User Schematics [5] and in the FPGA Pinout Excel Sheet [4].

There are two optional Ethernet signals (ETH1_RXDV and ETH1_COL) routed to FPGA bank 3A, but they are not required in RMII mode. If these signals are used, the VCC_CFG_HPS_B3A I/O voltage must be configured to 1.8 V.

Signal Name	HPS Pin	FPGA Pin
ETH1_RESET#	HPS35	-
ETH1_INT#_PWDN#	HPS37	-
ETH1_MDC[7]	-	AA18
ETH1_MDIO[7]	-	AA19
ETH1_RXD0	-	C12
ETH1_RXD1	-	D11
ETH1_RXER	-	D8
ETH1_TXEN	-	Y16
ETH1_TXD0	-	AF26
ETH1_TXD1	-	V15
ETH1_CRSDV	-	AD26

Table 28: Fast Ethernet Signal Description

2.20.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.20.4 MDIO Address

The MDIO address assigned to the Fast Ethernet PHY A is 1.

The MDIO interface is connected to the FPGA pins AA18 and AA19.

[7] On revision 1 modules, the MDIO interface is shared between the Gigabit Ethernet PHY and the Fast Ethernet PHY. Starting with revision 2, the MDIO is completely separated between PHYs: the Gigabit Ethernet PHY can be configured from the HPS side, while the Fast Ethernet PHY can be configured from the FPGA logic.

On revision 1 modules, the MDIO interface is shared between the Gigabit Ethernet PHY and the Fast Ethernet PHY, allowing the PHYs to be configured individually by using the corresponding addresses.

Starting with revision 2, the MDIO is completely separated between PHYs: HPS pins 20-21 are used for the configuration of the Gigabit Ethernet PHY, while FPGA pins AA18 and AA19 are used for the configuration of the Fast Ethernet PHY.

Part of the first production batch of Mars MA3 SoC modules revision 2 is missing pull-up resistors on the MDIO lines of the Fast Ethernet interface, on the PHY side. Please refer to the Mars MA3 SoC Module Known Issues and Changes document [6] for details on this issue and its solution.

For better signal integrity it is also recommended activating the FPGA internal pull-ups on the Fast Ethernet MDIO signals.

2.20.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

Starting with revision 2 modules, the bootstrap resistors have been optimized to accommodate the presence of weak the pull resistors in the FPGA, and ensure that the PHY is properly configured regardless of the FPGA programming status.

The bootstrap options of the Ethernet PHY are set as indicated in Table 29.

Pin	Signal Value	Description
RMII_EN	1	RMII mode enabled, 50 MHz clock
PHYAD[4-0]	00001	PHY0: MDIO address 1
LED_CFG	0	LED0 on for good link, blink for TX/RX activity
LED_SPEED	1	LED1 on for 100 Mbps
AMDIX_EN	1	Auto-MDIX enabled
AN_0	1	Auto-negotiation enabled

Table 29: Fast Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.21 USB 2.0

The Mars MA3 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host, USB device and USB On-The-Go (host and device capable) operations.

2.21.1 USB PHY Type

Table 30 describes the equipped USB PHY device type on the Mars MA3 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 30: USB 2.0 PHY Type

2.21.2 Signal Description

The ULPI interface is connected to HPS pins for use with the integrated USB controller. The USB reset has a pull-down resistor and needs to be driven high to release the PHY from reset.

A detailed list of the HPS connections is found in Section 2.9.7.

2.22 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. VCC pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Refer to Section 4 for details on the I2C bus on the Mars MA3 SoC module.

The interrupt output of the RTC is connected to HPS pin 52 and has a 4.7 kΩ pull-up resistor to VCC_CFG_HPS_B3A. A detailed list of the HPS connections is found in Section 2.9.7.

2.22.1 RTC Type

Table 31 describes the equipped RTC device type on the Mars MA3 SoC module.

Type	Manufacturer
PCF85063ATL/1,118	NXP Semiconductors

Table 31: RTC Type

An example demonstrating how to use the RTC is included in the Mars MA3 SoC module reference design [2].

2.23 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.23.1 EEPROM Type

Table 32 describes the equipped EEPROM device type on the Mars MA3 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 32: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mars MA3 SoC module reference design [2].

3 Device Configuration

3.1 Configuration Signals

Table 33 describes the most important configuration pins. The flash signals are connected to the module connector via level shifters.

Signal Name	FPGA Pin	HPS Pin	QSPI Flash Pin	Module Connector Pin	Comments
FLASH_CLK	DCLK	GPIO 34	CLK	182	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
FLASH_CS#	-	GPIO 33	CS#	188	Depending on the boot mode
FLASH_DI	ASDATA0_ASDO	GPIO 29	SI/IO0	186	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
FLASH_DO	-	GPIO 30	SO/IO1	184	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
FLASH_IO2_LV	-	GPIO 31	IO2	-	4.7 kΩ pull-up to VCC_1V8
FLASH_IO3_LV	-	GPIO 32	IO3	-	4.7 kΩ pull-up to VCC_1V8
HPS_RST#	-	HPS_RST#	-	192	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
HPS_POR#	CONFIG#	HPS_POR#	RESET#	196	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
FPGA_CONFDONE	CONFDONE	-	-	194	1 kΩ pull-up to VCC_CFG_HPS_B3A
BOOT_MODE0	-	-	-	190	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
BOOT_MODE1	-	-	-	170	4.7 kΩ pull-up to VCC_CFG_HPS_B3A

Table 33: FPGA and HPS Configuration Pins

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mars MA3 SoC module.

HPS and FPGA Configuration Pins

The BSEL and CSEL pins determine in which memory interface is the boot loader stored and how to clock the interface; details on BSEL and CSEL pins when using the HPS boot are available in the Booting and Configuration Introduction document [21]. The MSEL pins, which are used to select an FPGA configuration scheme, are described in the Cyclone V Device Handbook [20].

3.2 Boot Mode

The BOOT_MODE signals determine whether the SoC device boots from the QSPI flash, from the eMMC flash or from an external SD card connected to the SD pins on the HPS bank.

The eMMC flash clock is interrupted when the eMMC flash enable signal, EMMC_EN#, is inactive (for example, when booting from SD card). When booting from the QSPI flash, it is possible to access either the SD card or the eMMC flash, depending on the EMMC_EN# signal and on how the SDIO controller is mapped in Quartus.

EMMC_EN# signal is driven by the boot mode signals. This signal is also mapped to HPS pin 53 and can be toggled to switch between eMMC and SD card interfaces, provided that the SDIO devices are not used at the moment of switching (for example for the filesystem).

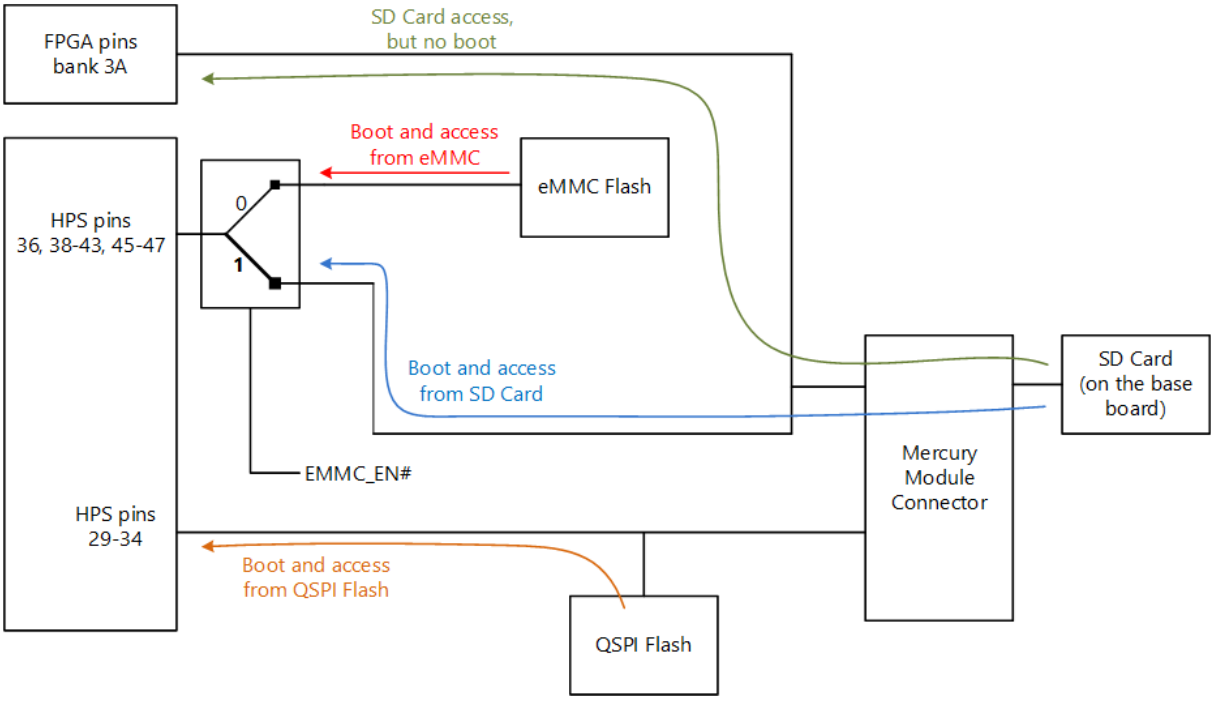

Figure 10: Boot Modes

Table 34 describes the available boot modes and the corresponding boot mode signals. By default, SD card boot mode is active.

BOOT_ MODE1	BOOT_ MODE0	EMMC_EN#	HPS boot	FPGA boot	MSEL[4:0]	CSEL[1:0]	BSEL[2:0]
0	0	0	reserved	reserved	10000	00	001
0	1	0	eMMC	from HPS	00010	00	100
1	0	1	QSPI	from HPS	00010	00	110
1	1	1	SDIO	from HPS	00010	00	100

Table 34: Boot Modes

3.3 JTAG

The FPGA and the HPS JTAG interfaces are connected into one single chain available on the module connector.

The SoC device and the QSPI flash can be configured via JTAG using Intel tools.

The Mars MA3 SoC module is compatible with Intel FPGA download cable (Blaster) I and II. Terasic USB Blaster is compatible with the module, provided that the VCC_CFG_HPS_B3A is in the 2.5 V - 3.3 V voltage range.

3.3.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	158	4.7 kΩ pull-down
JTAG_TMS	162	4.7 kΩ pull-up to VCC_CFG_HPS_B3A
JTAG_TDI	160	-
JTAG_TDO	164	4.7 kΩ pull-up to VCC_CFG_HPS_B3A

Table 35: JTAG Interface

3.3.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VCC pin of the programmer must be connected to VCC_CFG_HPS_B3A.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.4 eMMC Boot Mode

In the eMMC boot mode, the HPS boots from the eMMC flash located on the module and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Cyclone V datasheet [19].

3.5 QSPI Boot Mode

In the QSPI boot mode, the HPS boots from the QSPI flash and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Cyclone V datasheet [19].

When booting from the QSPI flash, it is possible to access either the SD card or the eMMC flash, depending on the EMMC_EN# signal and on how the SDIO controller is mapped in Quartus.

3.6 SD Card Boot Mode

In the SD card boot mode, the HPS boots from the SD card located on the base board and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Cyclone V datasheet [19].

3.7 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

3.8 QSPI Flash Programming via JTAG

The Intel Quartus software offers QSPI flash programming support via JTAG. For more information, please refer to the Quartus user manual [23].

The process of programming the QSPI flash via JTAG using “quartus_hps” tool can take up to 30 minutes.

3.9 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the HPS_RST# signal to GND followed by a pulse on HPS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. HPS_RST# must be low when HPS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and HPS_RST# must be tri-stated and another reset impulse must be applied to HPS_POR#.

Figure 11 shows the signal diagrams corresponding to flash programming from an external master.

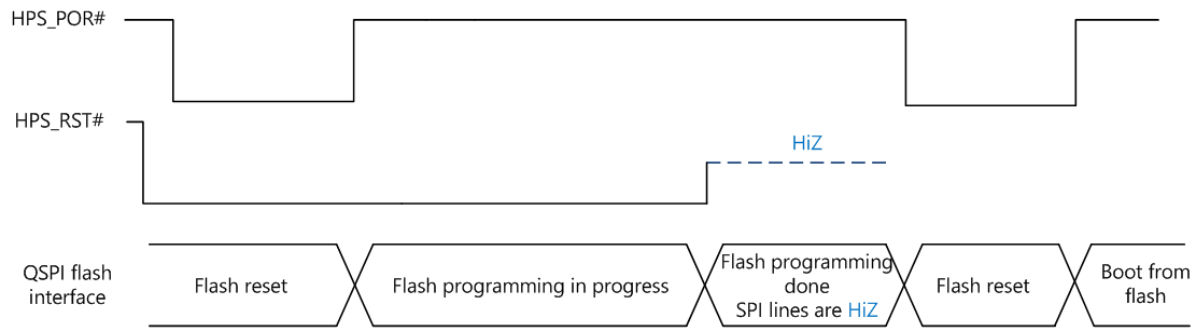

Figure 11: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mars MA3 SoC module.

3.10 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using the Enclustra Module Configuration Tool (MCT) [17].

4 I2C Communication

4.1 Overview

The I2C bus on the Mars MA3 SoC module is connected to the SoC device, EEPROM and RTC, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 36 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

Starting with revision 2 modules, the I2C bus is connected to both HPS and FPGA sides (and not only to the HPS), to offer extra flexibility and help on future development. I2C on FPGA side is functional only when the VCC_IO_B3B_B4A voltage is 1.8 V or higher.

Level shifters are used between the I2C bus and the HPS and FPGA pins, to allow I/O voltages lower than 3.3 V.

Signal Name	HPS Pin	FPGA Pin	Connector Pin	Resistor
I2C_SDA_HPS	HPS_GPIO55	I2C_SDA_FPGA	176	2.2 kΩ pull-up
I2C_SCL_HPS	HPS_GPIO56	I2C_SCL_FPGA	178	2.2 kΩ pull-up
I2C_INT#_HPS	HPS_GPIO54	I2C_INT#_FPGA	174	4.7 kΩ pull-up

Table 36: I2C Signal Description

4.3 I2C Address Map

Table 37 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.23)
0x51	RTC registers

Table 37: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mars MA3 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 38: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mars MA3 SoC module	0x0331	0x[XX]	0x[YY]	0x0331 [XX][YY]

Table 39: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC type	0	3	See SoC type table (Table 41)
	3-0	SoC device speed grade	6	8	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low power)	
	5	Gigabit Ethernet port count	0	1	
	4	Fast Ethernet port count	0	1	
	3	RTC equipped	0	1	
	2-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR3L RAM size (GB)	0 (0 GB)	2 (2 GB)	Resolution = 1 GB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	Reserved	-	-	
	3-0	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB

Table 40: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 1 GB, DRAM=2: 2 GB, DRAM=3: 4 GB, etc).

Table 41 shows the available SoC types.

Value	SoC Device Type
0	5CSEBA4U23
1	5CSEBA5U23
2	5CSXFC5C6U23
3	5CSXFC6C6U23

Table 41: SoC Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 42 indicates the absolute maximum ratings for Mars MA3 SoC module. The values given are for reference only; for details please refer to the Cyclone V Datasheet [19].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 6	V
VCC_3V3	3.3 V supply voltage relative to GND	-0.5 to 3.6	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCIO}+0.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 42: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 43 indicates the recommended operating conditions for Mars MA3 SoC module. The values given are for reference only; for details please refer to the Cyclone V Datasheet [19].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	3.0 to 5.5	V
VCC_3V3	3.3 V supply voltage relative to GND	3.15 to 3.45	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCIO}+0.2	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 43: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

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References

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