User's Guide

TPS54824 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54824EVM-779 evaluation module (PWR779) as well as for the TPS54824 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS54824EVM-779.

Table of Contents

List of Figures

List of Tables

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1 Introduction

1.1 Background

The TPS54824 dc/dc converter is a synchronous buck converter designed to provide up to an 8-A output. The input (VIN) is rated for 4.5 V to 17 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54824 regulator. The RT/CLK pin is configured for 700-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS54824 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54824 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS54824 provides adjustable soft start and undervoltage lockout inputs and a power-good output.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54824EVM-779	V_{IN} = 4.5 V to 17 V	0 A to 8 A

1.2 Performance Specification Summary

A summary of the TPS54824EVM-779 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54824EVM-779 is designed and tested for V_{IN} = 4.5 V to 17 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54824EVM-779 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			4.5	12	17	V
V_{IN} start voltage				4.4		V
V_{IN} stop voltage				4		V
Output voltage setpoint				1.8		V
Output current range	V_{IN} = 4.5 V to 17 V		0		8	A
Load regulation	V_{IN} = 4.5 V to 17 V, I_O = 8 A			–0.1%		
Load transient response	I_O = 2 A to 6 A	Voltage change		–50		mV
		Recovery time		75		µs
	I_O = 6 A to 2 A	Voltage change		55		mV
		Recovery time		75		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 4 A			116		kHz
Phase margin	V_{IN} = 12 V , I_O = 4 A			58		degree

Table 1-2. TPS54824EVM-779 Performance Specification Summary (continued)

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input ripple voltage	I_O = 8 A		270		mVPP
Output ripple voltage	I_O = 8 A		11		mVPP
Output rise time			1.1		ms
Operating frequency (f_{SW})			700		kHz
Maximum efficiency	TPS54824EVM-779, V_{IN} = 5 V, I_O = 2 A		94.3%		

1.3 Evaluating the TPS54824EVM-779 at –40°C

The TPS54824EVM-779 was designed and optimized at room temperature of 25°C. For evaluation down -40 °C, the compensation must be adjusted to provide sufficient gain and phase margin. Recommended compensation changes for –40°C evaluation are: R5 = 5.36 kΩ, C18 = 5.6 nF, and C17 = 68 pF.

1.4 Modifications

These evaluation modules are designed to provide access to the features of the TPS54824. Some modifications can be made to this module. When modifications are made to the components on the EVM, the compensation components connected to the COMP pin may need to be changed. Changes to the f_{SW}, output voltage, output inductor, and output capacitors can require a change in the external compensation. Table 1-3 gives some example values for different applications.

1.4.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R8 and R6. R6 is fixed at 6.04 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R6 can change the output voltage above the 0.6-V reference voltage V_{REF}. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = R6 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \tag{1}$$

1.4.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R2 and R9. See the *TPS54824 4.5-V to 17-V (19-V Max.) Input, 8-A Synchrns Step-Down SWIFT™ Converter Data Sheet* for detailed instructions on setting the external UVLO.

1.4.3 Example Component Values For Common Output Voltages

Table 1-3 shows recommended modifications to the EVM for evaluating different output voltages. Depending on the load step response requirements in the application, the output capacitors may need to be different from the values shown in this table. More or less output capacitance can be used. If the output capacitors are changed, the compensation may need to be adjusted. Additionally, if a different f_{SW} is needed, the inductance value (L) may need to be changed. The TPS54824 datasheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW}, and inductance.

Table 1-3. Recommended Component Value Changes For Common Output Voltages

V_{OUT} (V)	f_{SW} (kHz)	R_T (R7) (kΩ)	L (µH)	C_{OUT} (µF)	R_{FBT} (R8) (kΩ)	R_C (R5) (kΩ)	C_C (C18) (nF)	C_P (C17) (pF)	C_{FF} (C19) (pF)
1	500	100	1.0	4x 47	4.02	3.32	10	180	470
1.8	500	100	1.5	4x 47	12.1	5.36	5.6	100	150
3.3	500	100	2.2	2x 47	27.4	3.32	10	180	68

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54824EVM-779 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes.

2.1 Input/Output Connections

The TPS54824EVM-779 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying greater than 5 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP7 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP9 as the ground reference.

Table 2-1. TPS54824EVM-779 EVM Connectors and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	VIN input voltage connector (see Table 1-1 for V_{IN} range)
J2	VOUT terminal to connect load
J3	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J4	2-pin header for power good resistor pullup connection. Add a shunt to pull up to VOUT.
TP1	VIN test point
TP2	EN test point
TP3	SW node test point
TP4	1.8-V test point
TP5	PGOOD pullup test point
TP6	PGOOD test point
TP7	PGND test point
TP8	SS/TRK test point
TP9	PGND test point
TP10	Test point between voltage divider network and output of TPS54824 converter. Used for loop response measurements.
TP11	PGND test point
TP12	AGND test point
TP13	AGND test point
TP14	PGND test point
TP15	Test point for supplying external CLK for synchronization. C20 and R10 should be populated to use.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 4 A and then decreases as the load current increases toward full load. Figure 2-1 shows the efficiency for the TPS54824EVM-779 at an ambient temperature of 25°C.

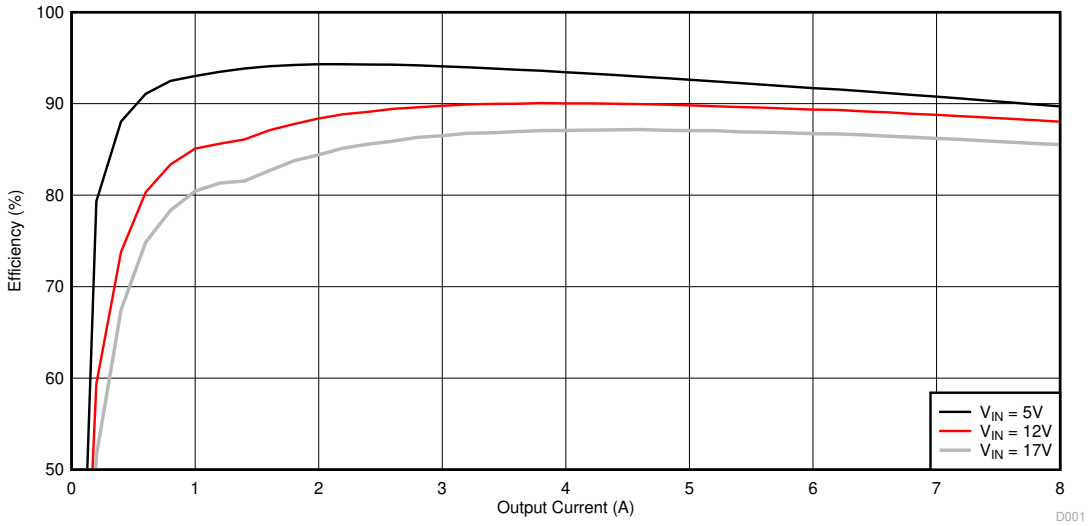

Figure 2-1. TPS54824EVM-779 Efficiency - Cyntec Inductor

Figure 2-2 shows the efficiency for the TPS54824EVM-779 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

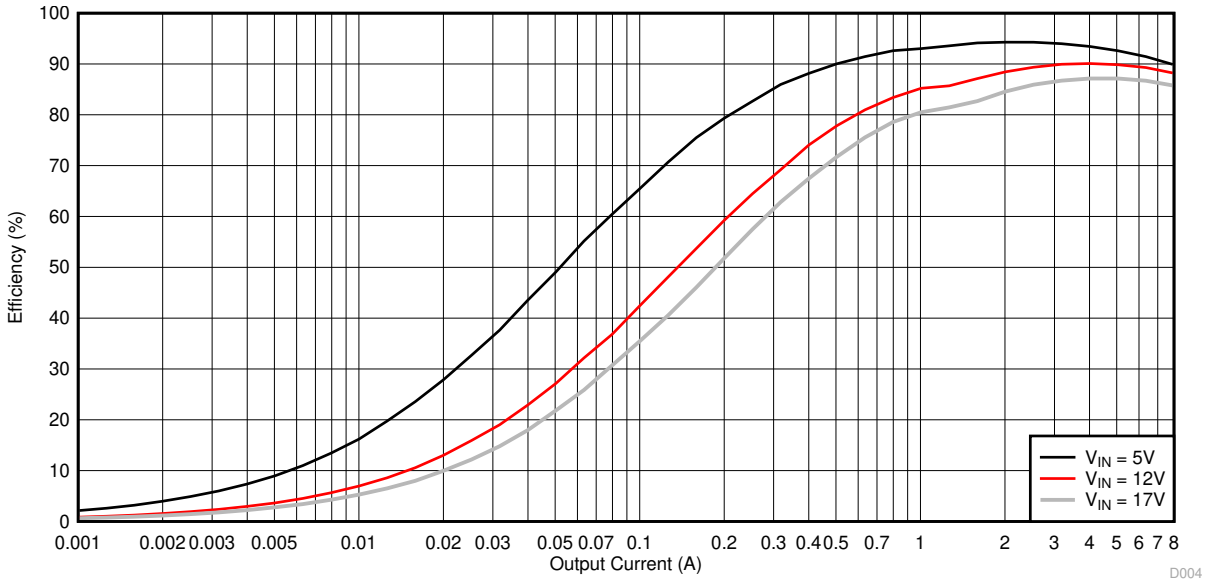

Figure 2-2. TPS54824EVM-779 Low Current Efficiency - Cyntec Inductor

Figure 2-3 shows the efficiency for the TPS54824EVM-779 with a WE 744311100 inductor. The ambient temperature is 25°C.

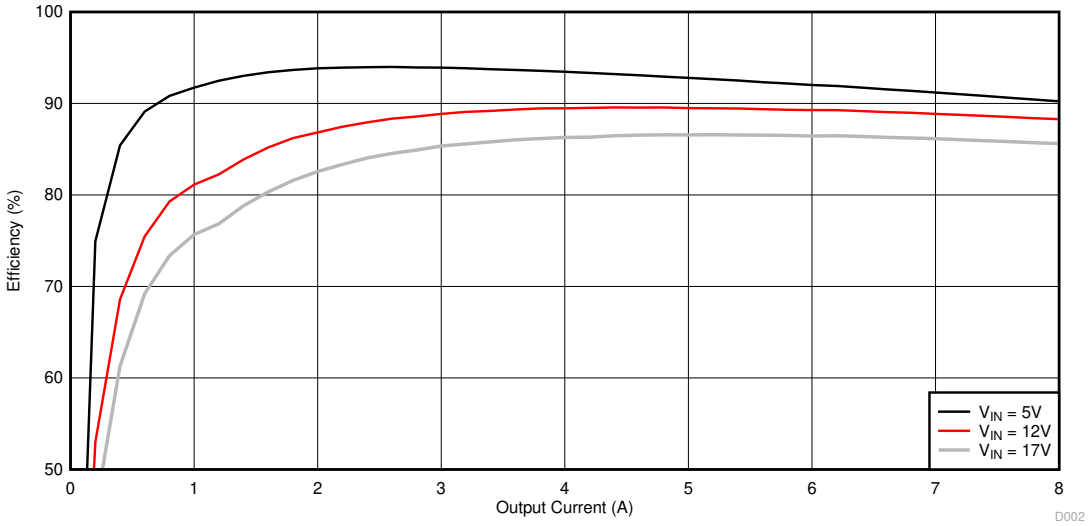

Figure 2-3. TPS54824EVM-779 Efficiency - Wurth Electronics 744311100 Inductor

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFETs.

2.3 Output Voltage Load Regulation

Figure 2-4 shows the load regulation for the TPS54824EVM-779.

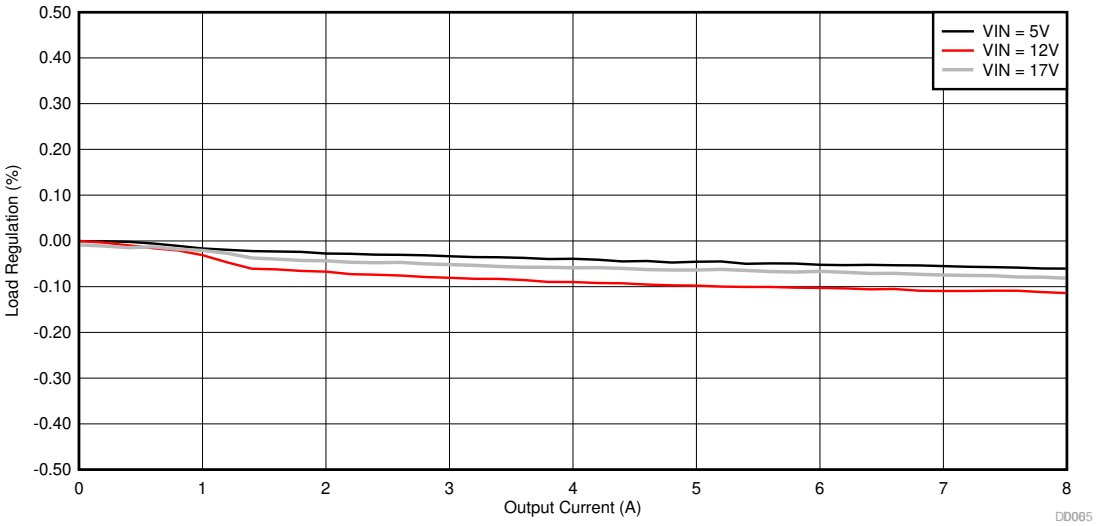

Figure 2-4. TPS54824EVM-779 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-5 shows the line regulation for the TPS54824EVM-779.

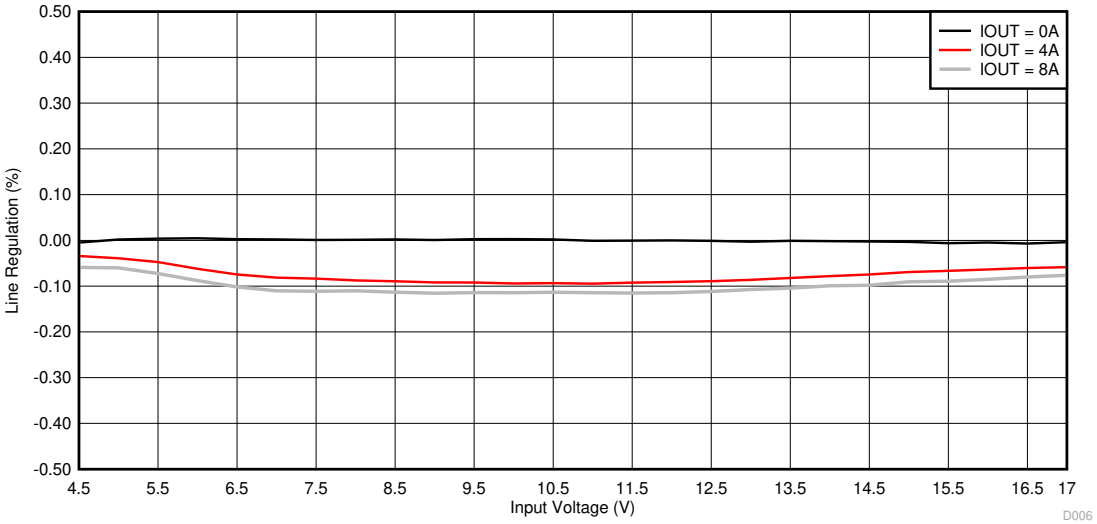

Figure 2-5. TPS54824EVM-779 Line Regulation

2.5 Load Transients

Figure 2-6 shows the TPS54824EVM-779 response to load transients. The current step is from 2 A to 6 A. The current step slew rate is 1 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

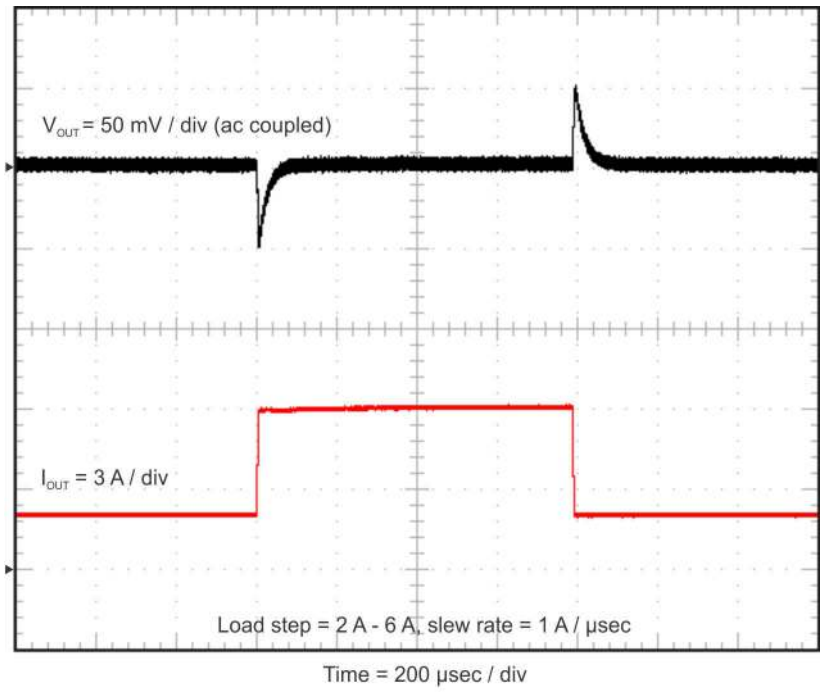

Figure 2-6. TPS54824EVM-779 Transient Response

2.6 Loop Characteristics

Figure 2-7 shows the TPS54824EVM-779 loop-response characteristics. Gain and phase plots are shown for V_{IN} = 12 V. Load current for the measurement is 4 A.

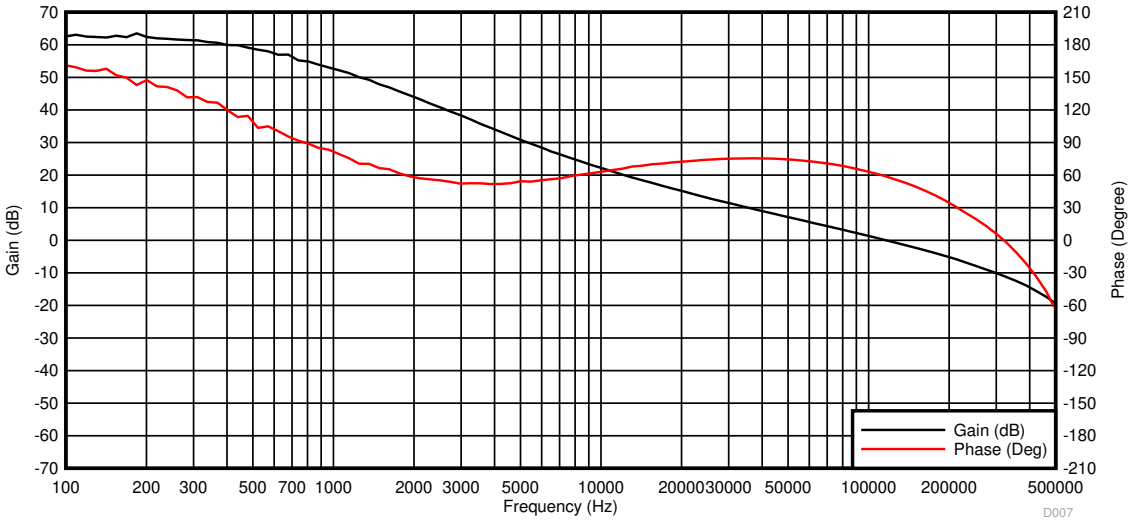

Figure 2-7. TPS54824EVM-779 Loop Response

2.7 Output Voltage Ripple

Figure 2-8 and Figure 2-9 show the TPS54824EVM-779 output voltage ripple. The load currents are no load and 8 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP9 and TP4.

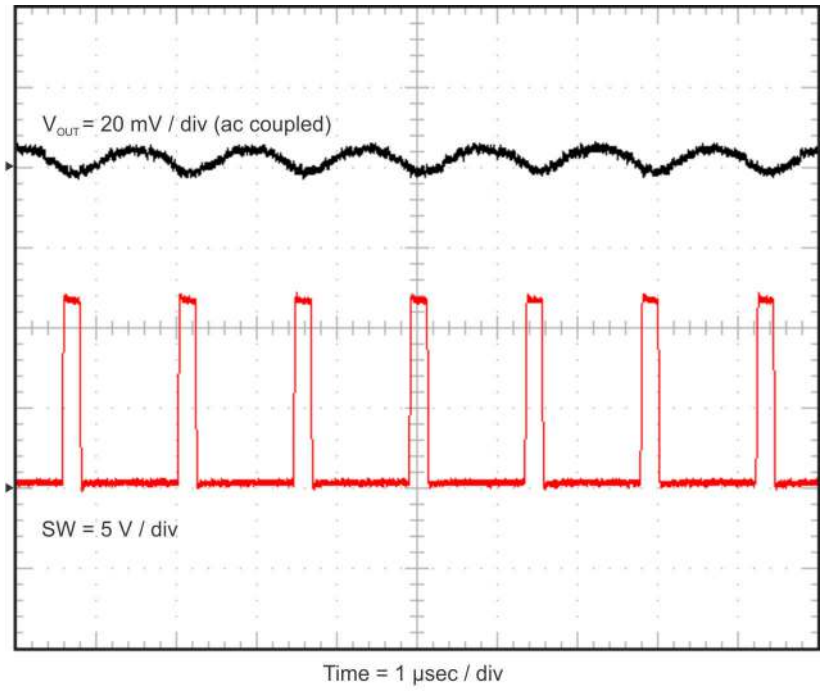

Figure 2-8. TPS54824EVM-779 Output Ripple, No Load

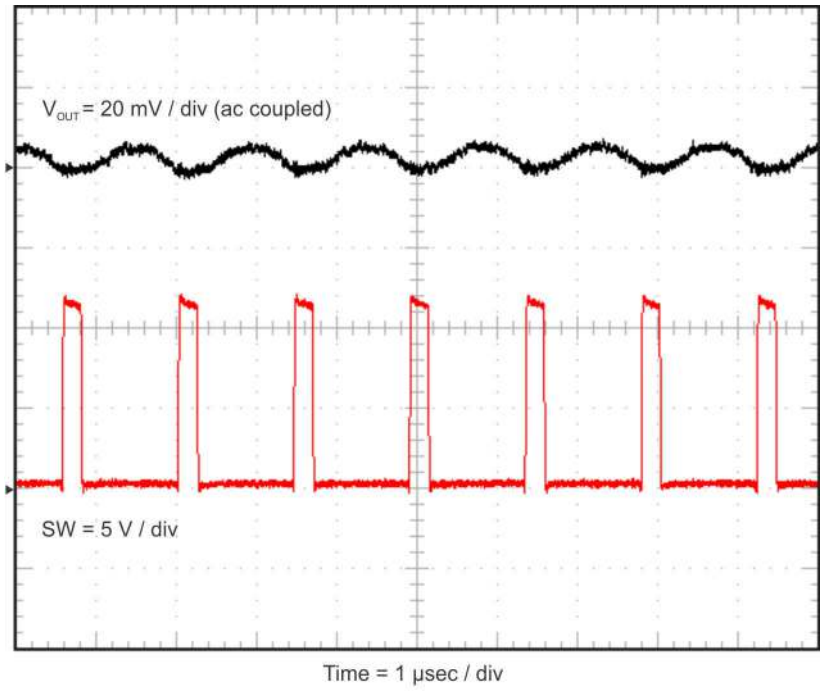

Figure 2-9. TPS54824EVM-779 Output Ripple, 8-A Load

2.8 Input Voltage Ripple

Figure 2-10 and Figure 2-11 show the TPS54824EVM-779 input voltage ripple. The load currents are no load and 8 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP1 and TP7.

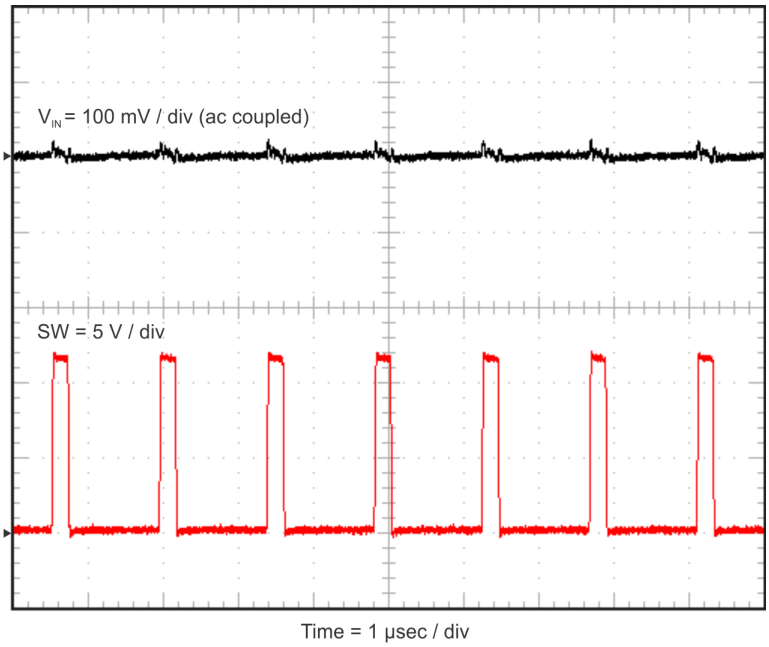

Figure 2-10. TPS54824EVM-779 Input Ripple, No Load

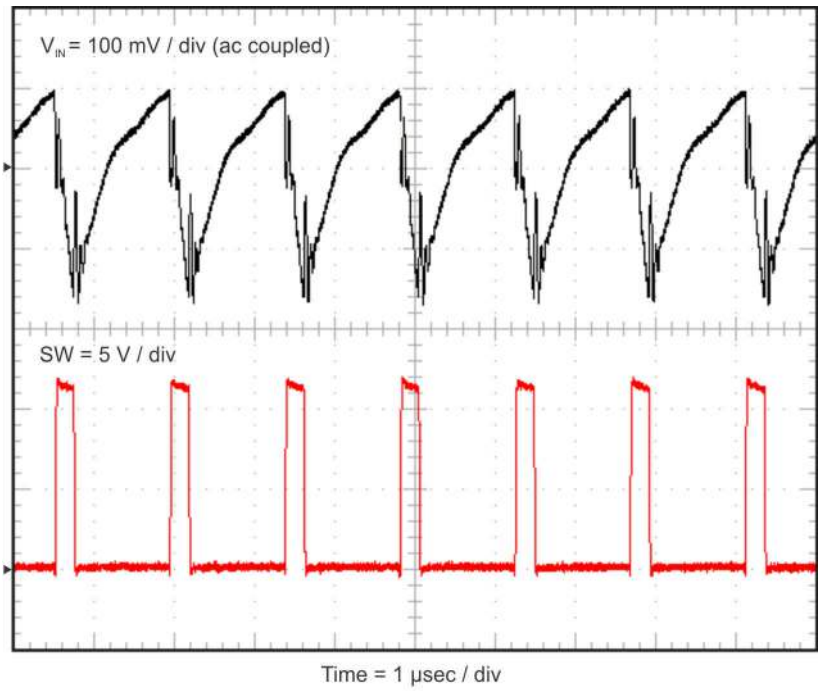

Figure 2-11. TPS54824EVM-779 Input Ripple, 8-A Load

2.9 Powering Up

Figure 2-12 and Figure 2-13 show the start-up waveforms for the TPS54824EVM-779. In Figure 2-12, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 2-13, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 12 V and the load is 1 Ω. Alternatively, a jumper at J3 to tie EN to GND can also be used. When the jumper is removed, EN is released and the start-up sequence will begin.

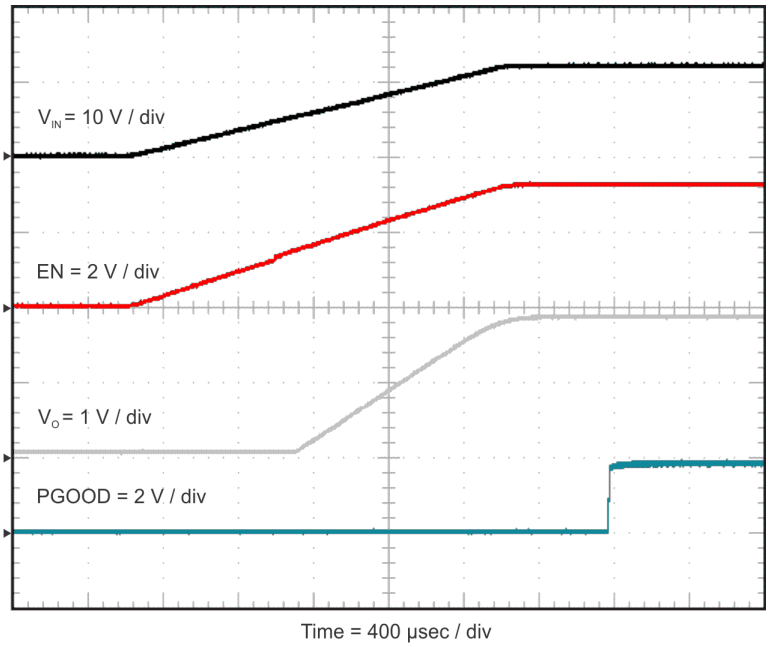

Figure 2-12. TPS54824EVM-779 Start-Up Relative to V_{IN}

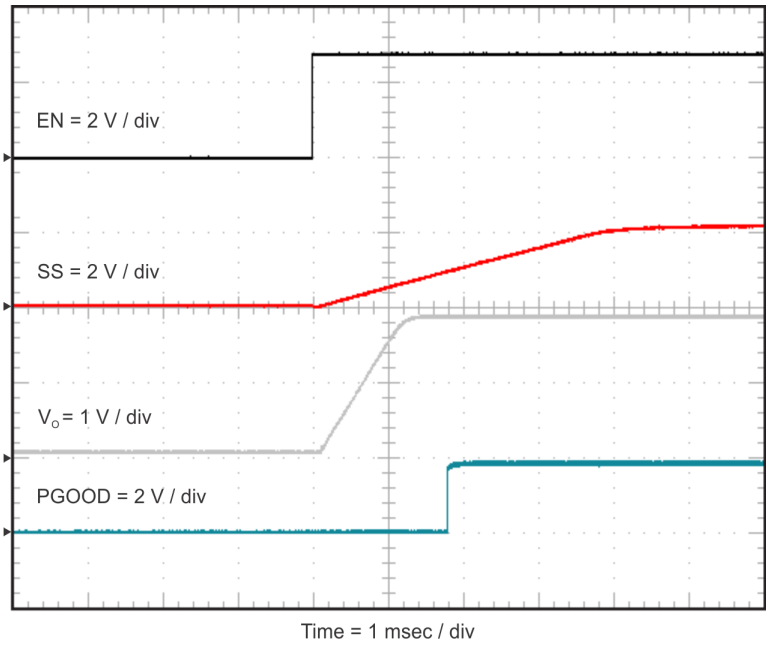

Figure 2-13. TPS54824EVM-779 Start-Up Relative to Enable

2.10 Powering Down

Figure 2-14 and Figure 2-15 show the TPS54824EVM-779 shutdown. The input voltage for these plots is 12 V and the load is 1 Ω.

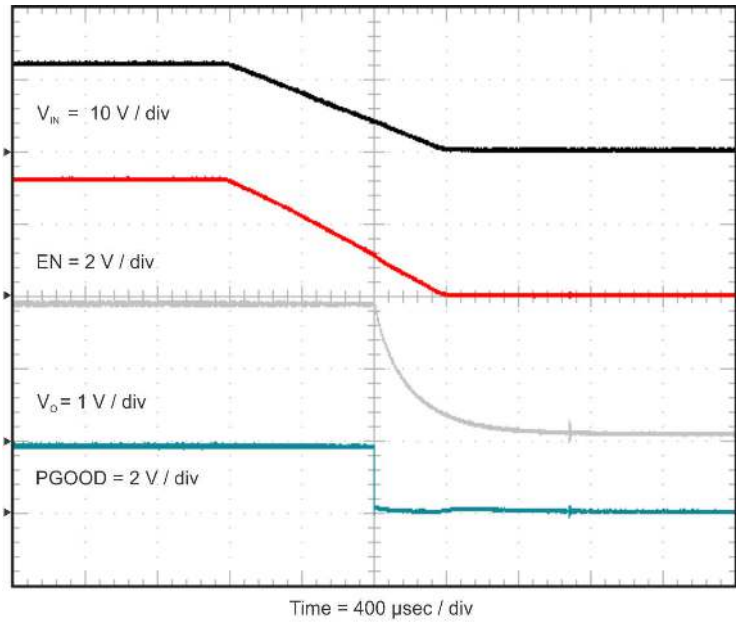

Figure 2-14. TPS54824EVM-779 Shutdown Relative to V_{IN}

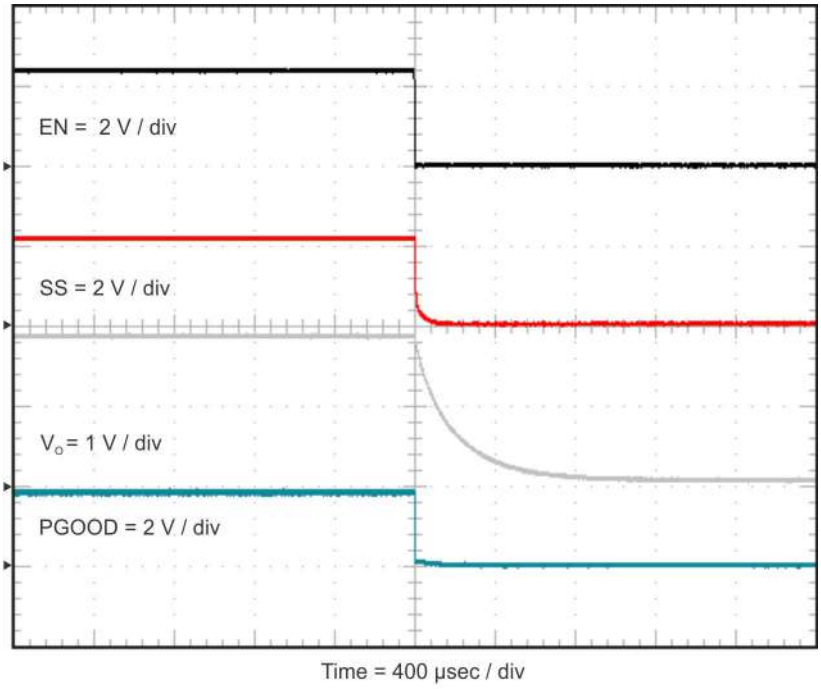

Figure 2-15. TPS54824EVM-779 Shutdown Relative to Enable

2.11 Start-Up Into Pre-Bias

Figure 2-16 shows the TPS54824EVM-779 start up into a pre-biased output. The output voltage is pre-biased to 1 V.

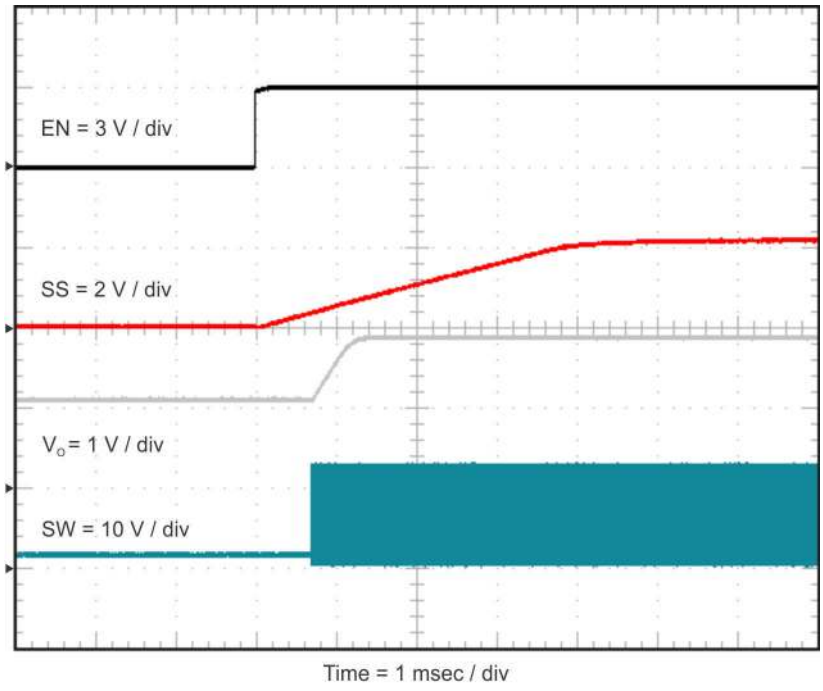

Figure 2-16. TPS54824EVM-779 Start-Up Into Pre-Bias

2.12 Hiccup Mode Current Limit

Figure 2-17, Figure 2-18, and Figure 2-19 show the TPS54824EVM-779 hiccup mode current limit feature. When an overcurrent event occurs, the TPS54824EVM-779 shuts down and restarts. Figure 2-17 shows the restart sequence in an overcurrent condition. Figure 2-18 shows the TPS54824EVM-779 entering hiccup mode and Figure 2-19 shows the TPS54824EVM-779 exiting hiccup mode.

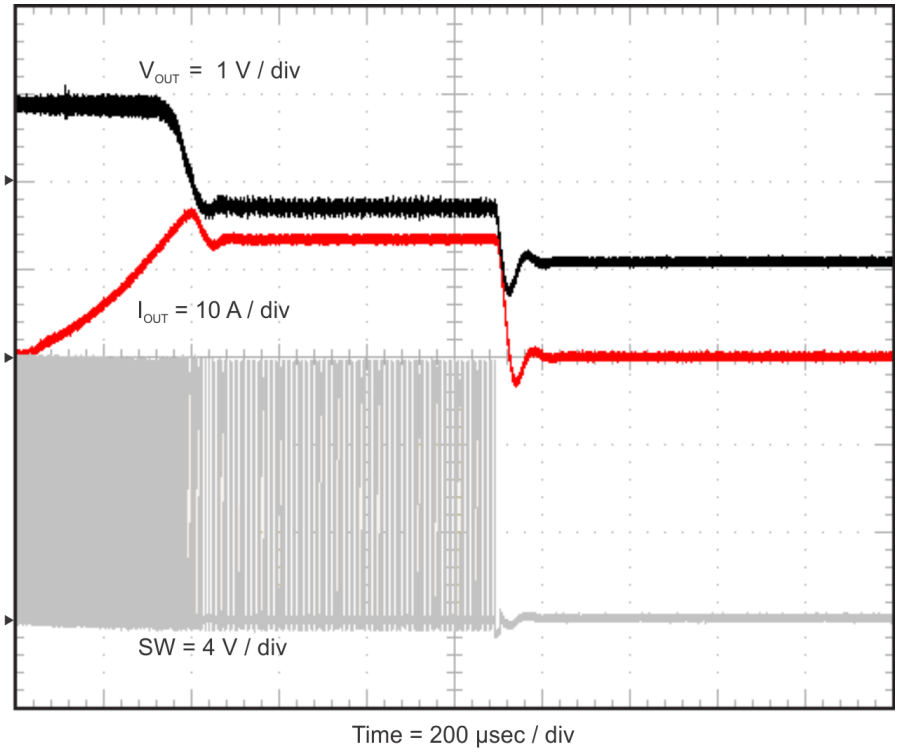

Figure 2-17. TPS54824EVM-779 Hiccup Mode Current Limit

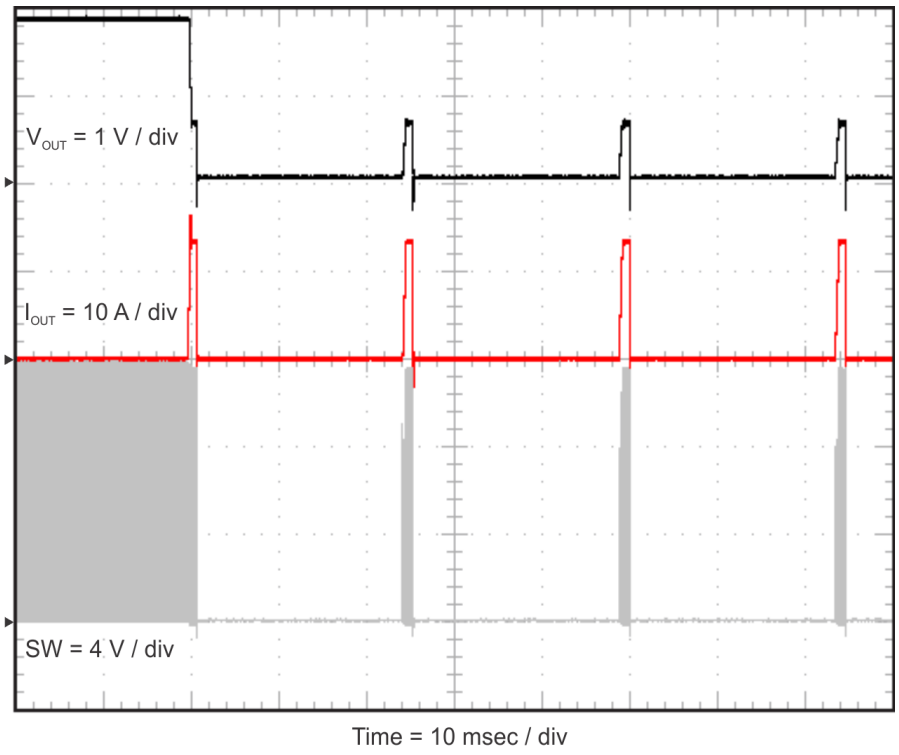

Figure 2-18. TPS54824EVM-779 Hiccup Mode Start

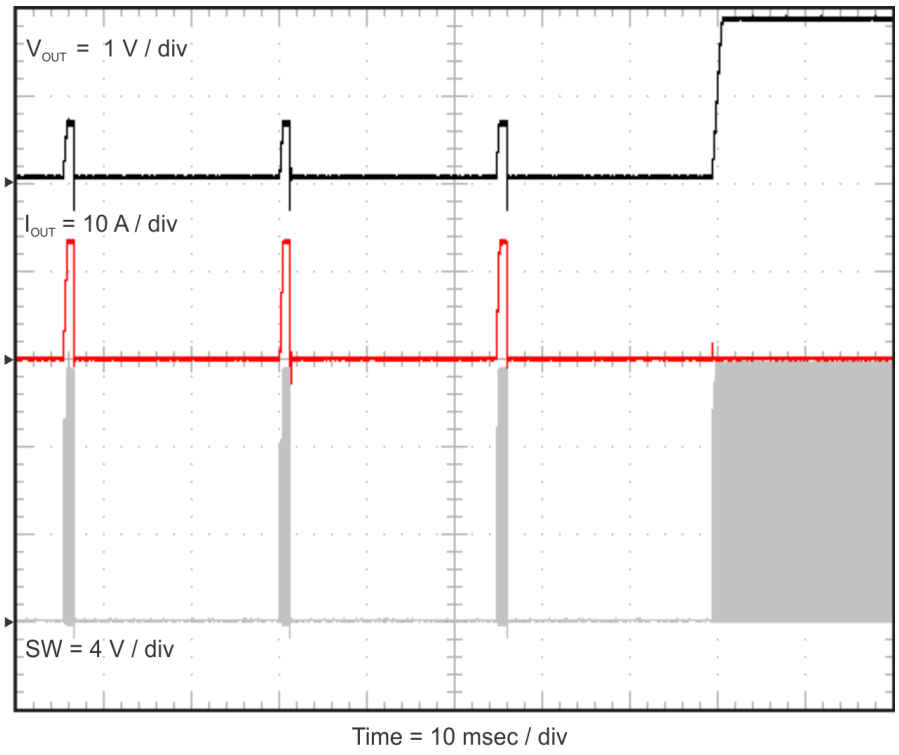

Figure 2-19. TPS54824EVM-779 Hiccup Mode Stop

3 Board Layout

This section provides a description of the TPS54824EVM-779 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54824EVM-779 is shown in Figure 3-1 through Figure 3-4. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for VIN, VOUT, and SW. Also on the top layer are connections for the remaining pins of the TPS54824 and the majority of the signal traces. The top layer has a dedicated ground plane for quiet analog ground that is connected to the main power ground plane at a single point. The internal layer-1 is a large ground plane and also routes signals to test points. The internal layer-2 contains an additional large ground copper area as well as an additional VIN and VOUT copper fill. The bottom layer is another ground plane with two additional traces for the output voltage feedback. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP4 test point. An additional input bulk capacitor is used to limit the noise entering the converter from the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS/TRK capacitor, RT/CLK resistor, and COMP pin are terminated to the quiet analog ground island on the top layer.

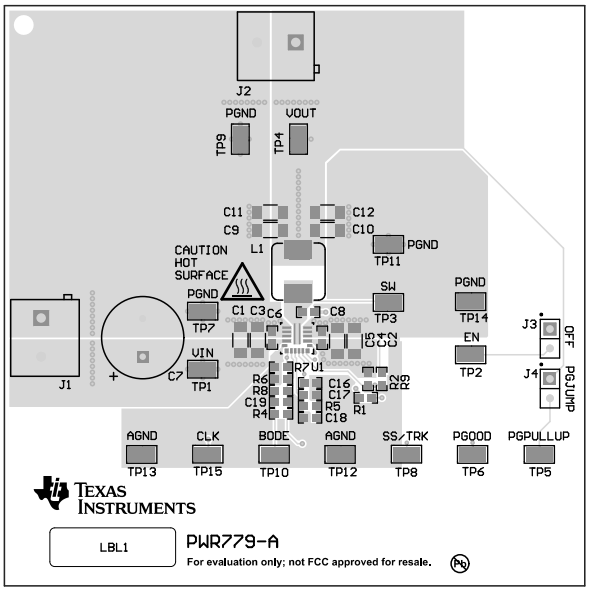

Figure 3-1. TPS54824EVM-779 Top-Side Layout

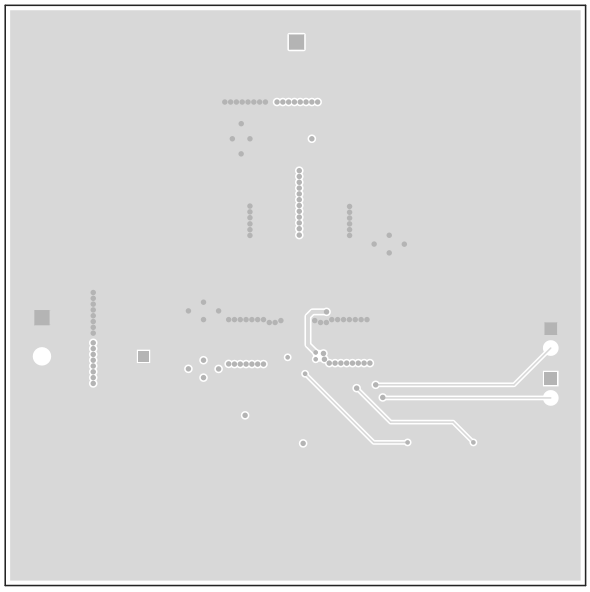

Figure 3-2. TPS54824EVM-779 Internal Layer-1 Layout

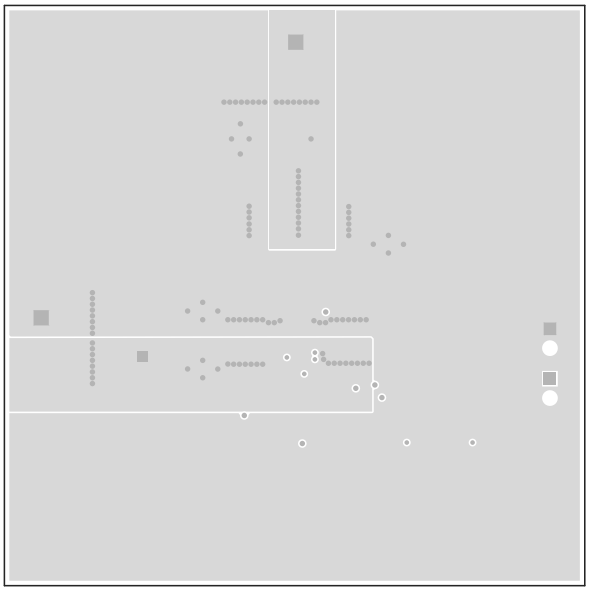

Figure 3-3. TPS54824EVM-779 Internal Layer-2 Layout

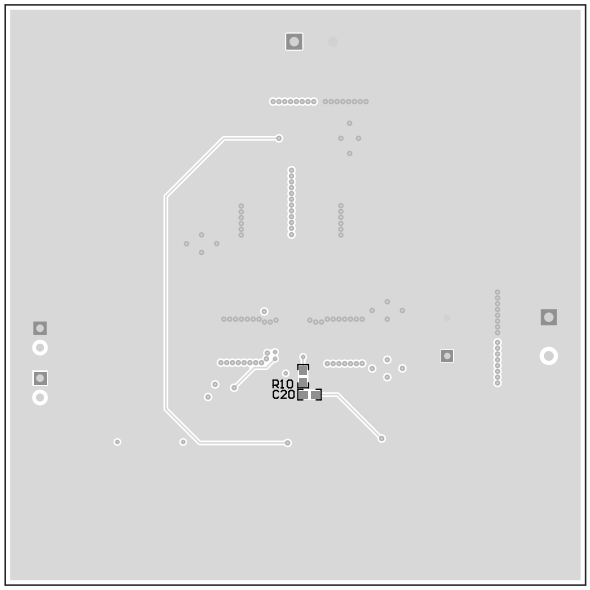

Figure 3-4. TPS54824EVM-779 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS54824EVM-779 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54824EVM-779.

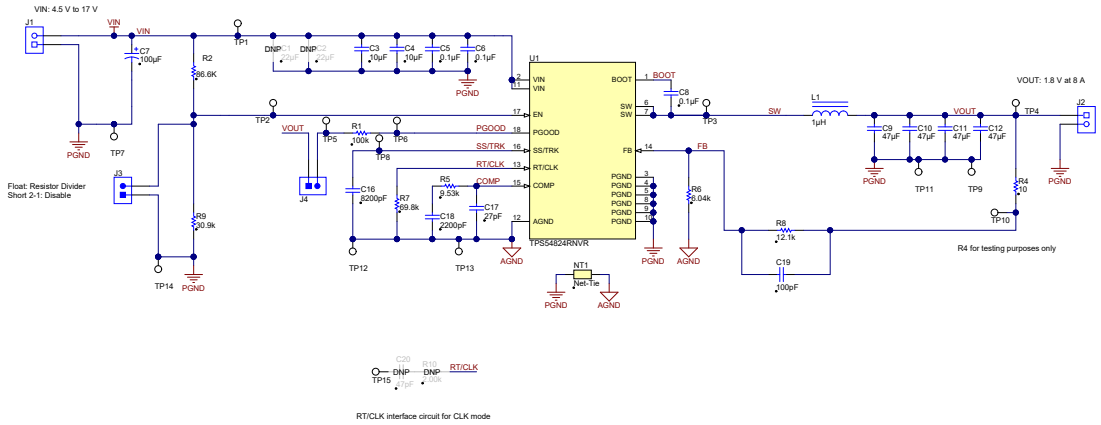

Figure 4-1. TPS54824EVM-779 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54824EVM-779.

Table 4-1. TPS54824EVM-779 Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C3, C4	2	10 µF	CAP, CERM, 10 µF, 35 V, ±20%, X5R, 1206	1206	C3216X5R1V106M160AB	TDK
C5, C6, C8	3	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±10%, X7R, 0603	0603	06033C104KAT2A	AVX
C7	1	100 µF	CAP, AL, 100 µF, 50 V, ±20%, 0.18 Ω, TH	Cap, 10x12.5mm	UBT1H101MPD1TD	Nichicon
C9, C10, C11, C12	4	47 µF	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 1206	1206	GRM31CR60J476ME19L	Murata
C16	1	8200 pF	CAP, CERM, 8200 pF, 25 V, ±10%, X7R, 0603	0603	GRM188R71E822KA01D	Murata
C17	1	27 pF	CAP, CERM, 27 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H270JA01D	Murata
C18	1	2200 pF	CAP, CERM, 2200 pF, 25 V, ±10%, X7R, 0603	0603	GRM188R71E222KA01D	Murata
C19	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	885012006057	Wurth Elektronik
J1, J2	2		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J3, J4	2		Header, 100 mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
L1	1	1 µH	Inductor, 1 µH, 14.4 A, 0.0064 Ω, SMD	6.95x2.8x6.6mm	CMLE063T-1R0MS	Cyntec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
R1	1	100 k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R2	1	86.6 k	RES, 86.6 k, 1%, 0.1 W, 0603	0603	CRCW060386K6FKEA	Vishay-Dale

Table 4-1. TPS54824EVM-779 Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R4	1	10	RES, 10, 5%, 0.1 W, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R5	1	9.53 k	RES, 9.53 k, 1%, 0.1 W, 0603	0603	CRCW06039K53FKEA	Vishay-Dale
R6	1	6.04 k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	CRCW06036K04FKEA	Vishay-Dale
R7	1	69.8 k	RES, 69.8 k, 1%, 0.1 W, 0603	0603	CRCW060369K8FKEA	Vishay-Dale
R8	1	12.1 k	RES, 12.1 k, 1%, 0.1 W, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
R9	1	30.9 k	RES, 30.9 k, 1%, 0.1 W, 0603	0603	CRCW060330K9FKEA	Vishay-Dale
SH-J1, SH-J2	2	1x2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	15		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		4.5-V to 17-V Input, 8-A Synchronous Step-Down Voltage Regulator, RNV0018B (VQFN-HR-18)	RNV0018B	TPS54824RNVR	Texas Instruments
C1, C2	0	22 µF	CAP, CERM, 22 µF, 35 V, ±20%, X5R, 1206	1206	C3216X5R1V226M160AC	TDK
C20	0	47 pF	CAP, CERM, 47 pF, 50 V, ±5%, C0G/NP0, 0603	0603	06035A470JAT2A	AVX
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R10	0	2.00 k	RES, 2.00 k, 1%, 0.1 W, 0603	0603	CRCW06032K00FKEA	Vishay-Dale

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2018) to Revision B (August 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Edited user's guide for clarity	2

Changes from Revision * (November 2016) to Revision A (November 2018)	Page
• Added Section 1.3	3
• Added Text: When modifications are made	3
• Added Section 1.4.3	4

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