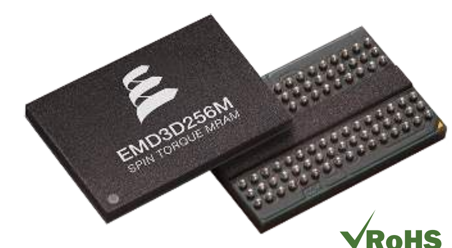
256Mb ST-DDR3 Spin-transfer Torque MRAM

FEATURES



- Non-volatile 256Mb (32Mb x 8, 16Mb x 16) DDR3
- Supports standard DDR3 SDRAM features
- V_{DD} = 1.5v +/- 0.075v
- Up to 667MHz ^{f}CK (1333MT/sec/pin)
- Page size of 512 bits (x8) or 1024 bits (x16)
- On-device termination
- On-Chip DLL aligns DQ, DQS, $\overline{DQS}$ transition with CK transition
- All addresses and control inputs are latched on rising edge of Clock
- Burst length of 8 with programmable Burst Chop length of 4
- Standard 10x13mm 78-Ball (x8) or 96-ball (x16) BGA Package

INTRODUCTION

The EMD3D256M08/16B 256Mb DDR3 Spin-transfer Torque MRAM (STT-MRAM) is a non-volatile memory that offers non-volatility and high endurance at DDR3 speeds. The device is capable of DDR3 operation at rates of up to 1333MT/Sec/Pin. It is designed to comply with all DDR3 DRAM features including on-device termination (ODT) and internal ZQ calibration but with the benefit of data persistence and extremely high write cycle endurance. With Spin-Torque MRAM technology, cell refresh is not required, which greatly simplifies system design and reduces overhead.

All control and address inputs are synchronized with a pair of externally supplied differential clocks, with input latching at clock crosspoints. I/Os are synchronized with a pair of bidirectional strobes (DQS, $\overline{DQS}$). The device uses a $\overline{RAS}$/$\overline{CAS}$ multiplexing scheme and operates at 1.5V.

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DDR3 DRAM COMPATIBILITY

Everspin DDR3 Spin-Torque MRAMs are fully compatible with DDR3 standards for DRAM operation defined in JEDEC Standard JESD79-3F, with exceptions and improvements as noted and defined in this data sheet.

- The Spin-Torque MRAM is a non-volatile memory. All data in closed/precharged banks are retained in memory whenever device power is removed for any reason.
- Command timing will be different in some cases. See "Table 11 – Timing Parameters" on page 20.
- The DDR3 standard applies to densities higher than 256Mb resulting in addressing and page size differences.
- Burst Type/Burst Order supports only the sequential burst type for CA<2:0 = 000 or 100. See "Burst Length, Type and Order" on page 30.
- This data sheet will make references to JESD79-3F when the function, timing, parameter or condition is identical between the MRAM and this standard. The JESD79-3F standard is available on the JEDEC website , registration is required.

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FUNCTIONAL DESCRIPTION

Basic Functionality

The DDR3 STT-MRAM is a high-speed Spin-Torque Magnetoresistive Random Access Memory internally configured as an eight-bank RAM. It uses an 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 MRAM consists of a single 8n-bit wide, four clock data transfer at the internal STT-MRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

READ and write operations to the DDR3 STT-MRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a "chopped" burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a READ or WRITE command. The address bits registered coincident with the Active command are used to select the bank and row to be activated ([BA0:BA2] select the bank; A0-A13 select the row); refer to "Table 1 – Addressing Scheme by I/O Width" on page 9" for specific requirements. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 STT-MRAM must be powered up and initialized in a predefined manner.

Figure 1 – Simplified State Diagram STT-MRAM

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 2 – Block Diagram (32Mb x 8) STT-MRAM

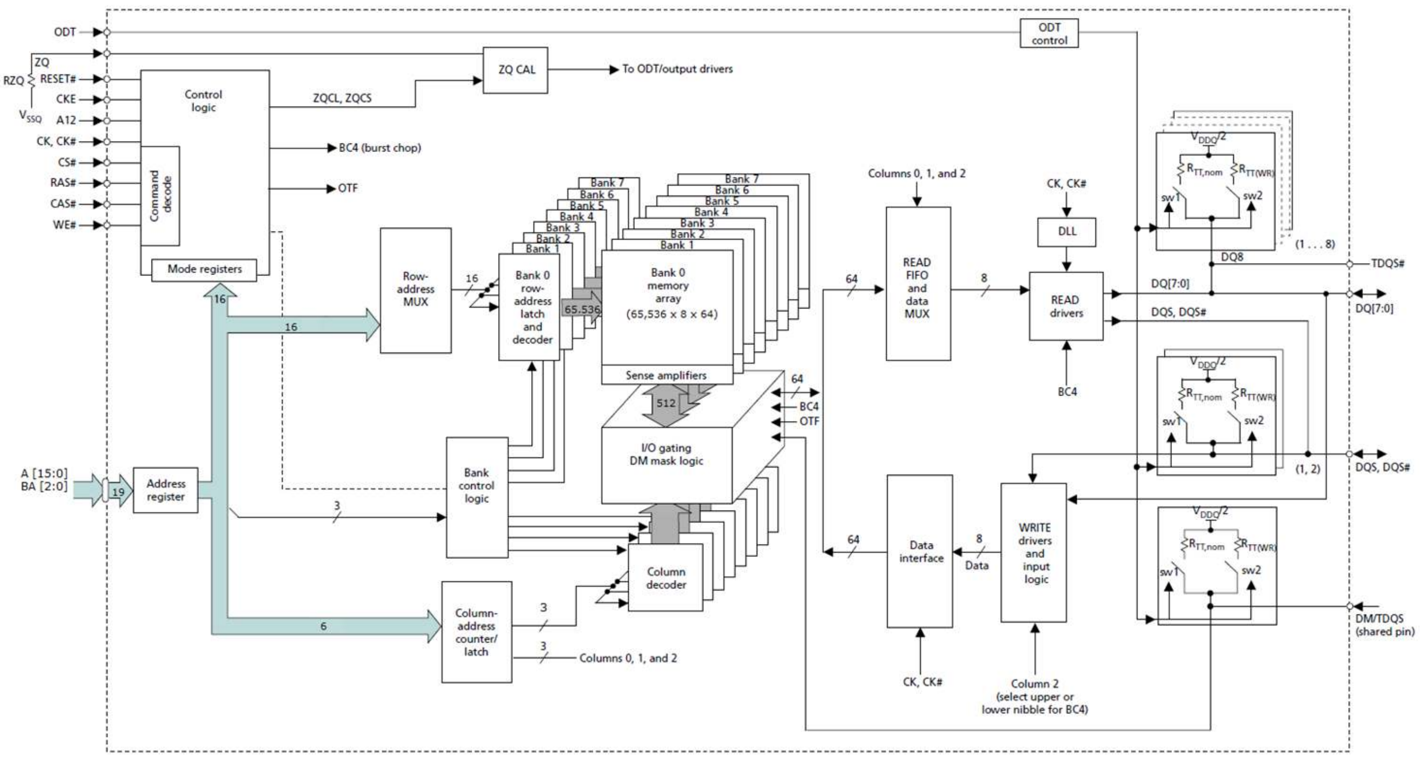

Figure 3 – Block Diagram (16Mb x 16) STT-MRAM

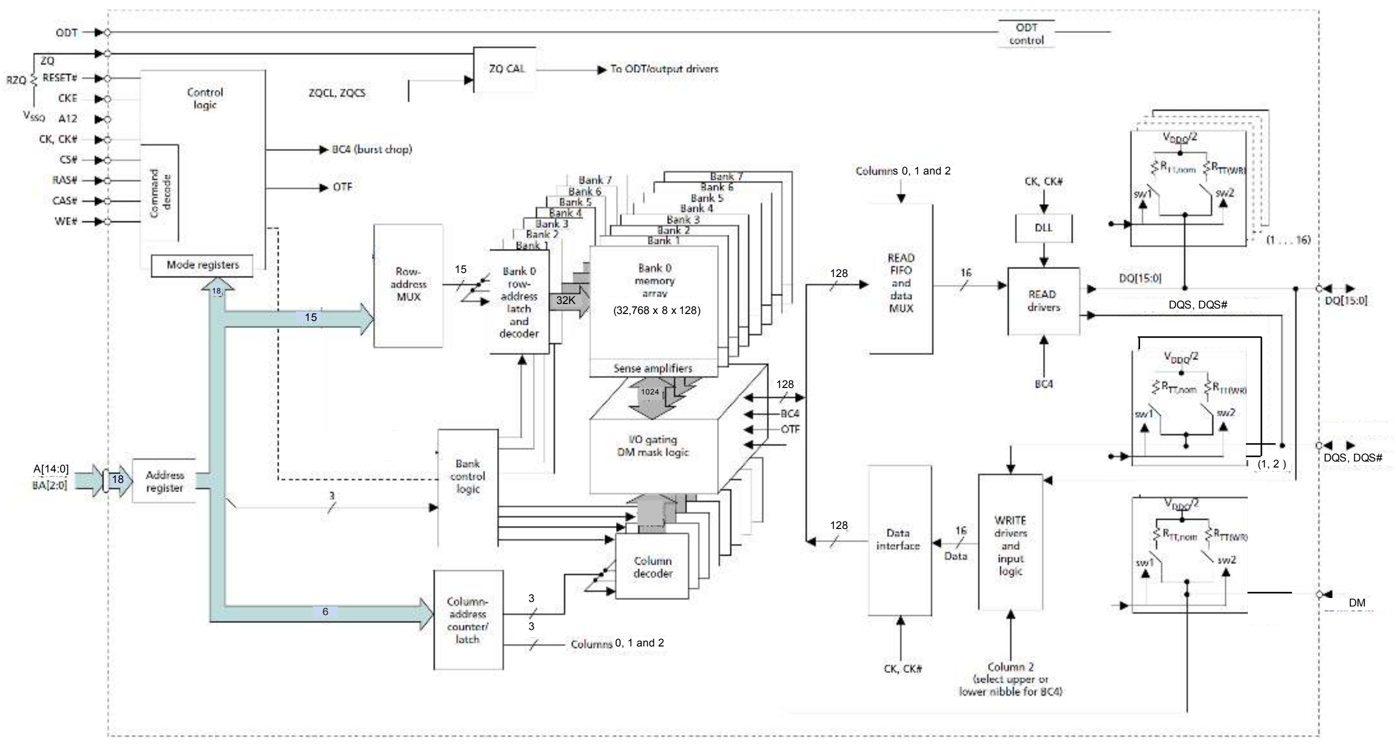

Table 1 – Addressing Scheme by I/O Width

The addressing scheme is shown in the Table 1 below. The Bank and Row Address is presented during an ACTIVE command. The Column Address is selected during a READ or WRITE command. Further explanation is given in the COMMAND section.

Configuration	32Mb x 8	16Mb x 16
# of Banks	8	8
Bank Address	BA0 - 2	BA0 - 2
Auto Precharge	A10/AP	A10/AP
BC Switch on the fly	A12/$\overline{BC}$	A12/$\overline{BC}$
# Rows	64K	32K
Row Address	A0 - A15	A0 - A14
# Columns	64	64
Column Address	A0 - A5	A0 - A5
Page Size	512 bits	1024 bits

PACKAGE BALL ASSIGNMENTS

256Mb x8 and x16 package ball assignments conform to JESD79-3F Standard DDR3 SDRAM footprints and pin assignments.

Table 2 – 32Mb x 8 in 78-Ball BGA - Top View

Row	1	2	3	4	5	6	7	8	9	Row
A	V_{SS}	V_{DD}	NC				NF/$\overline{TDQS}$	V_{SS}	V_{DD}	A
B	V_{SS}	V_{SSQ}	DQ0				DM/TDQS	V_{SSQ}	V_{DDQ}	B
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}	C
D	V_{SSQ}	DQ6	$\overline{DQS}$				V_{DD}	V_{SS}	V_{SSQ}	D
E	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}	E
F	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	F
G	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	G
H	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	H
J	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}	J
K	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	K
L	V_{SS}	A5	A2				A1	A4	V_{SS}	L
M	V_{DD}	A7	A9				A11	A6	V_{DD}	M
N	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	N
	1	2	3	4	5	6	7	8	9	

Table 3 – 16Mb x 16 in 96-Ball BGA - Top View

Row	1	2	3	4	5	6	7	8	9	Row
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{DQSU}$	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	$\overline{DQSL}$				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	J
K	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	K
L	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	L
M	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	T
	1	2	3	4	5	6	7	8	9	

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BALL FUNCTIONS AND DESCRIPTIONS

Table 4 – Ball Functions and Descriptions

Symbol	Type	Name	Description
CK, $\overline{\text{CK}}$	Input	Clock	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of $\overline{\text{CK}}$. Output data strobe (DQS, $\overline{\text{DQS}}$) is referenced to the crossings of CK and $\overline{\text{CK}}$.
CKE	Input	Clock Enable	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the STT-MRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 STT-MRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN, or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit. Input buffers (excluding CK, $\overline{\text{CK}}$, CKE, $\overline{\text{RESET}}$, and ODT) are disabled during POWER-DOWN. CKE is referenced to V_{REFCA}.
$\overline{\text{CS}}$	Input	Chip Select	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On-Die Termination	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 STT-MRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM	Input	Input Data Mask	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a WRITE access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{\text{TDQS}}$ is enabled by Mode Register A11 setting in MR1. For x16 DML is associated with DQ0-7 while DMU is associated with DQ8-15.
BA0, BA1, BA2	Input	Bank Address Inputs	Bank address inputs: BA[2:0] define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
A0-A15	Input	Address Inputs	Address Inputs: Provide the row address for Active commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{\text{BC}}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands. In using the device in x16 mode A15 needs to be pulled to logic HIGH.
Table continues on the next page.			

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Ball Functions and Descriptions (Continued)

Symbol	Type	Name	Description
A10/AP	Input	Auto Pre-charge	Auto-precharge: A10 is sampled during READ/WRITE commands to determine whether Autoprecharge should be performed to the accessed bank after the READ/ WRITE operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/$\overline{\text{BC}}$	Input	Burst Chop	Burst Chop: A12 / $\overline{\text{BC}}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
$\overline{\text{RESET}}$	Input	Acitve Low Asynchro-nous Reset	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/ Output	Data Input/ Output	Data Input/ Output: Bi-directional data bus. DQ0-7 (x8) and DQ8-15 (x16) are referenced to $V_{REFDQ\ in}$.
DQS/$\overline{\text{DQS}}$	Input/ Output	Data Strobe	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data. For x16 operation DQSL/$\overline{\text{DQSL}}$ is associated with DQ0-7 and DQSU/$\overline{\text{DQSU}}$ is associated with DQ8-15.
TDQS, $\overline{\text{TDQS}}$	Output	Termination Data Strobe	Termination data strobe: Applies to the x8 configuration only. When enabled via Mode Register A11=1 in MR1, STT-MRAM will enable the same termination resistance function on TDQS/$\overline{\text{TDQS}}$ that is applied to DQS/$\overline{\text{DQS}}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and $\overline{\text{TDQS}}$ is not used.
V_{DD}	Supply	Power Supply	Power supply: 1.5V ±0.075V.
V_{DDQ}	Supply	DQ Power Supply	DQ power supply: 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{SS}	Supply	Ground	Ground
V_{SSQ}	Supply	DQ Ground	DQ ground: Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	Reference Voltage for Control, Command and Address	Reference voltage for control, command, and address: V_{REFCA} must be maintained at all times for proper device operation.

Table continues on the next page.

Ball Functions and Descriptions (Concluded)

Symbol	Type	Name	Description
V_{REFDQ}	Supply	Reference Voltage for Data	Reference voltage for data: V_{REFDQ} must be maintained at all times for proper device operation.
ZQ	Refer-ence	External Ref-erence Ball for Output Drive Calibratoin	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	-	No Connect	No Connect: These balls should be left unconnected (the ball has no connection).
NF	-	No Function	No Function

ABSOLUTE MAXIMUM RATINGS

Table 5 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}				
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}				
T_{OPER}	Normal operating temperature	0	85	°C	2
T_{STG}	Storage temperature	-55	150	°C	-
H_{max}	Maximum magnetic field during read, write, standby or power off.	-	2,000	A/m	

Notes:

1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. The normal temperature range specifies the temperature at which all STT-MRAM specifications will be supported. During operation, the STT-MRAM case temperature must be maintained between 0°C to 85°C under all operating conditions.

THERMAL CHARACTERISTICS

Table 6 – Thermal Characteristics 78-ball BGA Package

Symbol	Parameter	Value	Unit
T_{OPER}	Maximum Operating Temperature	0 to 85	°C
Θ_{JA}	Thermal Resistance Junction to Ambient	26.4	°C/watt
Θ_{JC}	Thermal Resistance Junction to Case	2.3	°C/watt

Table 7 – Thermal Characteristics 96-ball BGA Package

Symbol	Parameter	Value	Unit
T_{OPER}	Maximum Operating Temperature	0 to 85	°C
Θ_{JA}	Thermal Resistance Junction to Ambient	25.6	°C/watt
Θ_{JC}	Thermal Resistance Junction to Case	2.3	°C/watt

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DC CHARACTERISTICS

DC Characteristics are defined under standard measurement conditions specified in JEDEC Standard JESD79-3F.

Table 8 – Power Supply and Input Leakage

All voltages referenced to V_{SS}						
Symbol	**Parameter/Condition**	**Min**	**Nom**	**Max**	**Unit**	**Notes**
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1, 2
V_{DDQ}	I/O supply voltage	1.425	1.5	1.575	V	1, 2
I_I	Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	-2	-	2	µA	3
I_{VREF}	V_{REF} supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	-1	-	1	µA	3, 4

Notes:

1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be ≤ V_{DD}. $V_{SS} = V_{SSQ}$.
2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. V_{REF} (see JESD79-3F Section 8, *AC and DC Input Measurement Levels*)
4. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.

Table 9 – Input / Output Capacitance

Note 1 applies to the entire Table.

Symbol	Parameter	DDR3-All Bins		Unit	Notes
		Min	Max		
C_{CK}	CK and $\overline{CK}$	0.8	1.6	pF	
C_{DCK}	ΔC: CK to $\overline{CK}$	0	0.15	pF	
C_{IO}	Single-end I/O: DQ, DM	1.5	3.0	pF	2
	Differential I/O: DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$	1.5	3.0	pF	3
C_{DQQS}	ΔC: DQS to $\overline{DQS}$, TDQS,$\overline{TDQS}$	0	0.2	pF	3
C_{DIO}	ΔC: DQ to DQS	-0.5	0.3	pF	4
C_{I}	Inputs (CTRL, CMD, ADDR)	0.75	1.5	pF	5
C_{DI_CTRL}	ΔC: CTRL to CK	-0.5	0.3	pF	6
$C_{DI_CMD_ADDR}$	ΔC: CMD_ADDR to CK	-0.5	0.5	pF	7
C_{ZQ}	ZQ pin capacitance	-	3.0	pF	
C_{RE}	Reset pin capacitance	-	3.0	pF	

Notes:

1. V_{DD} = 1.5V ±0.075mV, $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, $\overline{TDQS}$. C_{DDQS} is for DQS vs. $\overline{DQS}$ and TDQS vs. $\overline{TDQS}$ separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(\overline{DQS})})$.
5. Excludes CK, $\overline{CK}$; CTRL = ODT, $\overline{CS}$, and CKE; CMD = $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$; ADDR = A[n:0], BA[2:0].
6. $C_{DI_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(\overline{CK})})$.
7. $C_{DI_CMD_ADDR} = C_{I(CMD_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(\overline{CK})})$.

Table 10 – I_{DD} Maximum Limits

I_{DD} [1]	1333MT/sec/pin [2]		Units
	x8	x16	
I_{DD0}	220	220	mA
I_{DD1}	220	220	mA
I_{DD2P0} (slow)	55	55	mA
I_{DD2P1} (fast)	60	60	mA
I_{DD2Q}	90	90	mA
I_{DD2N}	90	90	mA
I_{DD2NT}	90	90	mA
I_{DD3P}	60	60	mA
I_{DD3N}	90	90	mA
I_{DD4R}	135	135	mA
I_{DD4W}	165	185	mA
I_{DD5B}	90	90	mA
I_{DD6}	45	45	mA
I_{DD7} [2]	490	667	mA
I_{DD8}	45	45	mA

Notes:

1. Refer to JESD79-3F Section 10, I_{DD} and I_{DDQ} Specification Parameters and Test Conditions, with some patterns that are STT-MRAM specific.
2. In order to limit power dissipation, I_{DD7} [2] is specified with ^{t}FAW = 190ns for the x8 and ^{t}FAW = 230ns for the x16. The ^{t}FAW can be reduced per Table 11 but I_{DD7} will increase.

TIMING PARAMETERS

Table 11 – Timing Parameters

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Internal READ to first data	^{t}AA	x8, x16	14	-	ns	
ACTIVE to internal READ or WRITE delay time	^{t}RCD	x8	95	-	ns	4
		x16	190	-	ns	4
Precharge command period	^{t}RP	x8	66	-	ns	4
		x16	134	-	ns	4
ACTIVE to ACTIVE command period	^{t}RC	x8	170	-	ns	4
		x16	332	-	ns	4
ACTIVE to Precharge command period	^{t}RAS	x8	103	-	ns	4
		x16	198	-	ns	4
ACT to ACT Command Period, different banks	^{t}RRD	x8, x16	30	-	ns	4
Four ACTIVE Window	^{t}FAW	x8	120	-	ns	4
		x16	160	-	ns	4
Output slew rate	SRQ	x8, x16	-	8.5	V/ns	4
DQS, DQS# Output high time for 1333 speed bin	^{t}QSH	x8, x16	-	.38	nCK	4
DQS, DQS# Output low time for 1333 speed bin	^{t}QSL	x8, x16	-	.38	nCK	4

Speed Bin	CL	CWL	Symbol	Min	Max	Unit	Notes
800	CL = 6	CWL = 5	^{t}CK (Avg)	2.5	3.3	ns	2
		CWL = 6,7,8,9	Reserved				3
1066 [1]	CL = 8	CWL = 6	^{t}CK (Avg)	1.875	< 2.5	ns	2
		CWL= 5,7,8,9	Reserved				3
1333 [1]	CL=10	CWL=7	^{t}CK (Avg)	1.5	<1.875	ns	2
		CWL= 5,6,8,9	Reserved				3
Supported CL settings				6,8,10		CK	
Supported CWL settings				5,6,7		CK	

1. The 1333 and 1066 speed grade ordering options are backward compatible with lower speed grade operation.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.
4. Parameter is different than Standard DDR3 due to STT-MRAM design

Note: Dynamic ODT timings are intended to follow the JEDEC specification but have not been characterized.

TRUTH TABLES

Command Truth Table

Table 12 – Command Truth Table

Notes 1-5 apply to the entire Table.

Function	Symbol	CKE Prev.	CKE Next	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA [2:0]	A13-A15	A12/ $\overline{BC}$	A10/ AP	A0-A9, A11	Notes
Mode Register Set	MRS	H	H	L	L	L	L	BA	Op. Code				
Refresh	REF	Not used for STT-MRAM											
Self Refresh Entry	SRE												
Self Refresh Exit	SRX												
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks	PREA	H	H	L	L	H	L	L	L	L	H	V	
Bank ACTIVE	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
WRITE (Fixed BL8 pr BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	V, CA	7
WRITE (BC4 on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	V, CA	7
WRITE (BL8 on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	V, CA	7
WRITE w/ Auto Precharge (Fixed BL8 or BC4)	WRAP	H	H	L	H	L	L	BA	RFU	V	H	V, CA	7
WRITE w/ Auto Precharge (BC4 On the Fly)	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	V, CA	7
WRITE w/ Auto Precharge (BL8 On the Fly)	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	V, CA	7
READ (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	V, CA	7
READ (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	V, CA	7
READ (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	V, CA	7

Table continues with notes next page.

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Command Truth Table (Continued)

Function	Symbol	CKE		CS	RAS	CAS	WE	BA [2:0]	A13-A15	A12/ BC	A10/ AP	A0-A9, A11	Notes
		Prev.	Next										
READ with Auto Precharge (Fixed BL8 or BC4)	RDAP	H	H	L	H	L	H	BA	RFU	V	H	V, CA	7
READ with Auto Precharge (BC4, on the Fly)	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	V, CA	7
READ (BL8, on the Fly)	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	V, CA	7
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	8
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	9
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	
				H	V	V	V						
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	10
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. Commands are defined by states of CS, RAS, CAS, WE, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configuration-dependent.
2. RESET is LOW enabled and used only for asynchronous reset. Thus, RESET must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.
4. Operations apply to the bank defined by the bank address, BA[2:0]. For MRS, BA selects one of four mode registers.
5. “V” means “H” or “L” (a defined logic level), and “X” means “Don’t Care.”
6. See the CKE Truth Table below for additional information on CKE transition.
7. Burst READ’s or WRITE’s cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
8. The purpose of the NOP command is to prevent the MRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
9. The DES and NOP commands perform similarly.
10. ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

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CKE Truth Table

Table 13 – CKE Truth Table

Notes 1,2 apply to the entire Table.

Current State [3]	CKE		Command [5] (RAS, CAS, WE. CS)	Action [5]
	Previous Cycle (n-1) [4]	Present Cycle (n) [4]		
Power Down	L	L	X	Maintain Power Down
	L	H	DES or NOP	Power Down Exit
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry
Reading	H	L	DES or NOP	Power Down Entry
Writing	H	L	DES or NOP	Power Down Entry
Precharging	H	L	DES or NOP	Power Down Entry
All Banks Idle [6]	H	L	X	Precharge Power Down Entry
	H	L		-

Notes:

1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. ^{t}CKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + ^{t}CKE (MIN) + ^{t}IH.
3. Current state = The state of the STT-MRAM immediately prior to clock edge n.
4. CKE (n) is the logic state of CKE at clock edge n; CKE (n - 1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 12 on page 21) Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All power-down exit parameters are also satisfied.

FUNCTIONAL PARAMETERS

Functional Parameter	Level	Description
Bit Error Rate (BER) Limit to End of Life	6.3×10^{-8}	It is expected that bit fails will be soft and distributed throughout the address space so the system ECC built into your controller should correct them. BER is after maximum page cycles, or at the end of the endurance life.
Cycle Endurance	1×10^{10}	A cycle is defined as a page access. After this number of cycles, the bit error rate may start to increase above the BER limit. System level ECC is recommended.
Data Retention	T_{OPER} = 70°C, 3 months	The data retention time starts from the last read or write cycle and does not differ between powered up and powered down conditions.

COMMAND DESCRIPTIONS

The 256Mb STT-MRAM is fully compatible with the command descriptions of JESD79-3F, section 4, with the following additional considerations:

1. Timing for Active, Precharge, Read, and Write commands are as described in JESD79-3F, with some exceptions due to the timing differences between DRAM and MRAM. These exceptions are noted in the description sections for each command.
2. To ensure the non-volatility of any data stored in the MRAM, it is necessary to close any open page by issuing a PRECHARGE command to any open banks or all banks (PRE or PREA). The PRECHARGE must be completed and ^{t}RP met with V_{DD} within the specified operating range.

ACTIVE Command

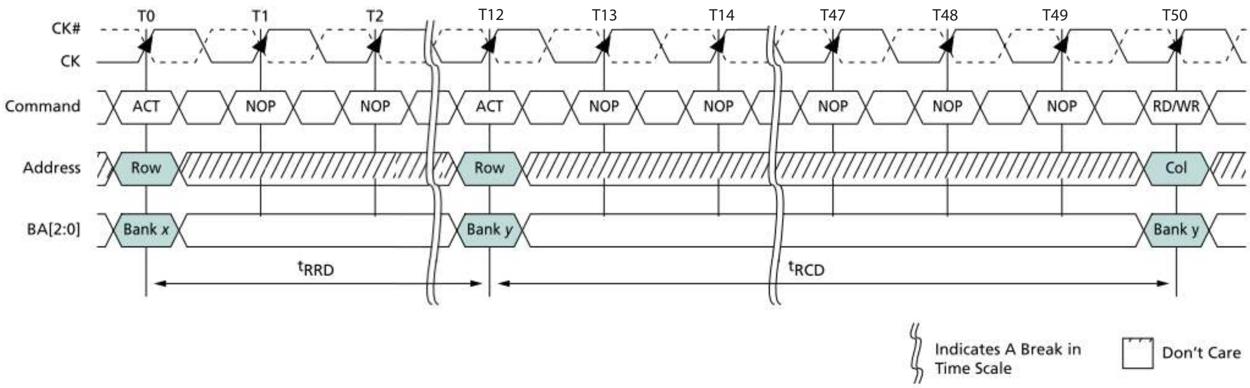
Before any READ or WRITE commands can be issued to a bank within the MRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to ^{t}RCD (MIN). In this operation, the MRAM enables a READ or WRITE command to be issued after the ACTIVE command for that bank, but prior to ^{t}RCD (MIN) with the requirement that (ACTIVE-to-READ/WRITE) + AL ≥ ^{t}RCD (MIN) (see Posted CAS Additive Latency). ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to ^{t}CCD (MIN).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD. No more than four bank ACTIVE commands may be issued in a given ^{t}FAW (MIN) period, and the ^{t}RRD (MIN) restriction still applies. The ^{t}FAW (MIN) parameter applies, regardless of the number of banks already opened or closed.

Figure 4 – ACTIVE Command Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)



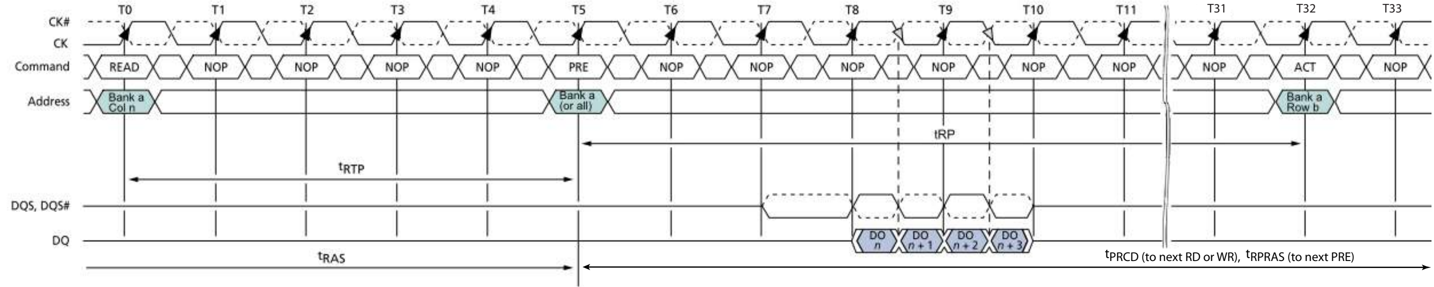
1. In this example, ^{f}CK=533MHz, 1066 MT/sec/pin, CL - ^{t}RCD - ^{t}RP = 8- 47-36, a READ or WRITE command may be issued 47 nCK (clock cycles) after the Bank is Activated.
2. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.
3. After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification.

PRECHARGE Command

Input A10 determines whether one bank or all banks are to be precharged and, in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as "Don't Care." After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

Figure 5 – PRECHARGE Command Timing



Notes:

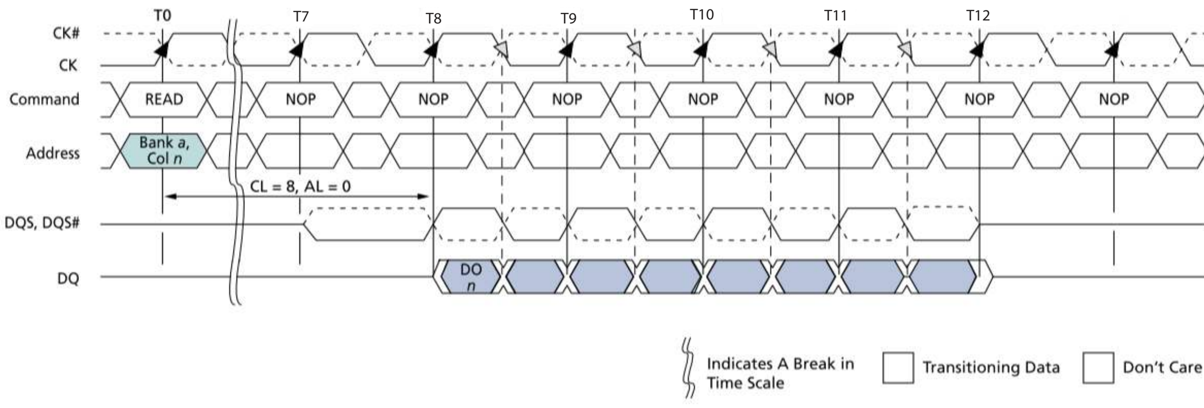
1. In this example, ^{f}CK = 533MHz, 1066 MT/sec/pin, AL=0, CL=8 with BC4 selected.
2. The minimum READ command to PRECHARGE command spacing to the same bank is equal to AL+ ^{t}RTP, with ^{t}RTP being the internal READ to PRECHARGE delay, 5 nCK (clock cycles).
3. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. This is 36 nCK (clock cycles) from the PRECHARGE command.
4. ^{t}RAS min and ^{t}RC min must be satisfied from the previous ACTIVE command.

READ Command

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of posted CAS additive latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and $\overline{CK}$.) Figure 6 below illustrates an example of RL based on a CL setting of 8 and an AL setting of 0.

Figure 6 – READ Command Timing



Notes:

1. Read Latency (RL) is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS latency (CL), (RL = AL + CL). -The value of AL and CL is programmable in the mode register via the MRS command. In this example, ^{f}CK = 533MHz, 1066 speed bin, CL=8, AL=0.
2. DO n=data-out from column n. Subsequent elements of data-out appear in the programmed order following DO n. -The burst length is selected by MR0 and A12 during the READ command.
3. Bank "a" was previously opened with an ACTIVE Command.

DQS, $\overline{DQS}$ is driven by the MRAM along with the output data. The initial LOW state on DQS and HIGH state on $\overline{DQS}$ is known as the READ preamble (^{t}RPRE). The LOW state on DQS and the HIGH state on $\overline{DQS}$, coincident with the last data-out element, is known as the READ postamble (^{t}RPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ goes High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Section 4.13.2.1 of JESD79-3F. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) is depicted in the same section.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued ^{t}CCD cycles after the first READ command. This is shown for BL8 in Standard JESD79-3F Figure 33. If BC4 is enabled, ^{t}CCD must still be met, which will cause a gap in the data output, as shown in JESD79-3F Figure 34. The DDR3 MRAM does not allow interrupting or truncating any READ burst. Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 can be found in JESD79-3F Figure 35, *READ (BL8) to WRITE (BL8)*. READ to WRITE timing for BC4 can be found in JESD79-3F Figure 36, *READ (BC4) to WRITE (BC4) OTF*. To ensure the READ data is completed before the WRITE data is on the bus, the minimum READ-to-WRITE timing is RL + ^{t}CCD - WL + 2^{t}CK.

For additional information on the READ command, please refer to JESD79-3F Section 4.13. Please note that in READ followed by a PRECHARGE, the MRAM ^{t}RP needs to be observed for a given CL.

WRITE Command

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto-precharge is selected, the row being accessed is precharged at the end of the WRITE burst. If auto-precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted.

During WRITE bursts, the first valid data-in element is registered on the first rising edge of DQS immediately following the WRITE latency (WL) clock time. Data elements will continue to be registered on successive edges of DQS.

WRITE latency (WL) is defined as the sum of posted CAS additive latency (AL) and CAS WRITE latency (CWL): WL = AL + CWL. The values of AL and CWL are programmed in the MR0 and MR2 registers respectively. Only AL=0 is supported. Prior to the first valid DQS edge, a full cycle is needed (including a dummy crossover of DQS, $\overline{DQS}$) and specified as the WRITE preamble shown in "Figure 7 – WRITE Burst Operation WL = 5 (AL = 0 CWL = 5, BL8)" on page 29. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WL clocks ±^{t}DQSS. Standard JESD79-3F Figure 43 includes ^{t}DQSS (MIN), ^{t}DQSS (NOM) and ^{t}DQSS (MAX) cases.

Data may be masked from completing a WRITE using data mask. The data mask occurs on the DM ball aligned to the WRITE data. If DM is LOW, the WRITE completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z,

and any additional input data will be ignored.

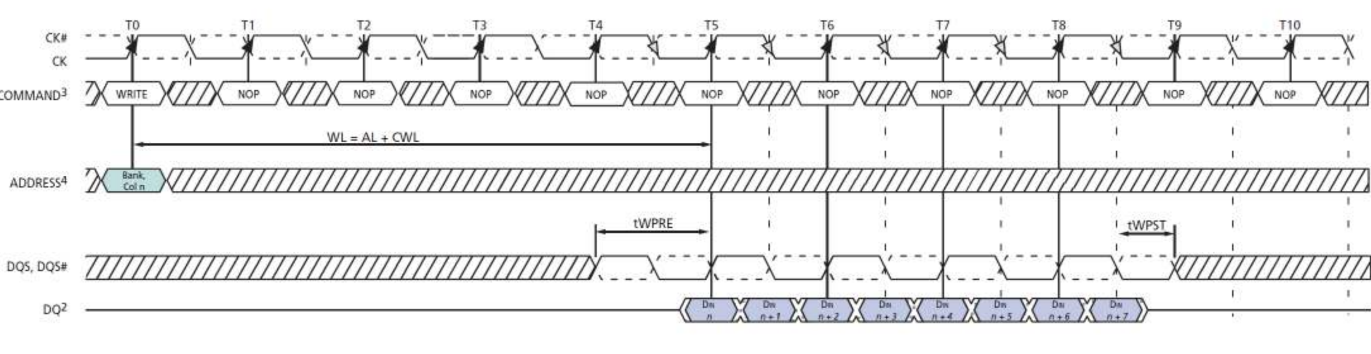
Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be ^{t}CCD clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Standard JESD79-3F Figure 51, *WRITE(BL8) to WRITE(BL8)* and Figure 52, *WRITE (BC4) to WRITE (BC4) OTF* illustrate concatenated bursts.

Data for any WRITE burst may be followed by a subsequent READ command after ^{t}WTR has been met (see Standard JESD79-3F Figure 53, *WRITE (BL8) to READ (BC4/BL8) OTF*.) Additional WRITE burst diagrams are given in Section 4.14, *WRITE Operation*.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command, providing ^{t}WR has been met, as shown in Standard JESD79-3F Figures 49 and 50. Please note that in Write followed by a PRECHARGE, the MRAM ^{t}RP needs to be observed for a given CL.

Both ^{t}WTR and ^{t}WR starting time may vary, depending on the mode register settings (fixed BC4, BL8 versus OTF).

Figure 7 – WRITE Burst Operation WL = 5 (AL = 0 CWL = 5, BL8)



TRANSITIONING DATA DON'T CARE

Notes:

1. BL8, WL= 5; AL=0, CWL=5
2. D_{IN} n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 [A1:0= 00] or MR0 [A1:0 = 01] and A12 = 1 during WRITE command at T0

Burst Length, Type and Order

Accesses within a given burst may be programmed only in a sequential order which is selected via bit A3 of Mode Register MR0=0. The ordering of accesses within a burst is determined by the burst length and the starting column address as shown in Table 14 below. The burst length is defined by bits A1:A0 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and "on the fly" which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC_n.

Table 14 – Burst Length, Type and Order

Burst Length	READ/ WRITE	Starting Column Address A[2,1,0]	Burst Type = Sequencial (Decimal)
BC4	READ	000	0, 1, 2, 3, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X
		1, V, V	4, 5, 6, 7, X, X, X, X
BL8	READ	000	0, 1, 2, 3, 4, 5, 6, 7
		100	4, 5, 6, 7, 0, 1, 2, 3
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7

Burst Type/Burst Order supports only the sequential burst type for CA<2:0 = 000 or 100

PART NUMBER DECODER

Table 15 – 256Mb x8 / x16 STT-MRAM Ordering Part Number Decoder

	Vendor	Category	Family	Voltage	Density	IO Width	Package	Timing	Temp	Rev	Class	Packing
Example Ordering Part Number	E	M	D3	D	256M	8	G1	-150	C	B	S1	R

Description	Code	
Everspin	E	
Magneto-resistive	M	
DDR3	D3	
SSTL: Vcc & Vdd = 1.5v	D	
256 Mb	256M	
x8	08	
x16	16	
10x13 BGA 78-ball	G1	
1333 MT/s	-150	
Commercial	C	0 to 85℃
Device Version	Note 1	
Device Class	Note 2	
Tray	<blank>	
Tape and Reel	R	

Note 1	
Device Version	**Definition**
A	First Version
B	Second Version

Note 2	
Device Class	**Definition**
S1	Storage DEC

ORDERING PART NUMBERS

Table 16 – Ordering Part Numbers

Org	Temp	Package	Speed Bin	Shipping Container	Part Number
32Mb x 8	0 - 85°C	10x13mm 78-ball BGA	1333	Trays	EMD3D256M08G1-150CBS1
				Tape and Reel	EMD3D256M08G1-150CBS1R
16Mb x 16	0 - 85°C	10x13mm 96-ball BGA	1333	Trays	EMD3D256M16G2-150CBS1
				Tape and Reel	EMD3D256M16G2-150CBS1R

PACKAGE OUTLINE DRAWING

Figure 8 – 78-Ball BGA Package Outline (x8)

BOTTOM VIEW

PIN A1 INDEX

9 8 7 6 5 4 3 2 1

E1

A B C D E F G H J K L M N

D1

THE WINDOW-SIDE ENCAPSULANT

78 X øb
SOLDER BALL DIAMETER REFERS
TO POST REFLOW CONDITION.

ddd(M) C A B
eee(M) C

A
A1
// bbb C
ccc C
C
SEATING PLANE

TOP VIEW

PIN A1 INDEX

E

aaa C 4x

B
A
X

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'eE' & 'eD' REPRESENT THE BASIC SOLDER BALL GRID PITCH
3. 'b' IS MEASURABLE AT THE MAXIMUN SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C. THE SOLDER BALL DIAMETER IS ø0.45mm BEFORE REFILOW.THE SOLDER BALL PAD ø0.40mm
4. PRIMARY DATUM C ARE DEFINED BY THE SPHERICAL.
5. THE OVERALL PACKAGE THICKNESS 'A' ALREADY CONSIDER COLLAPSE.
6. PACKAGE DIMENSIONS CONFORM TO JEDEC MO-207.
7. THE DISTANCE BETWEEN THE TOP SURFACE OF SMALLEST SOLDER BALL (BALL HEIGHT) AND WINDOW-SIDE ENCAPSULANT MUST > 0.10mm.
8. THE HEIGHT OF WINDOW-SIDE ENCAPSULANT 't' COULD CHANGED ASSEMBLY HOUSE'S DESIGN,BUT IT MUST SATISFY THE REQUEST OF ITEM 7.
9. 'W' DEFINES THE DISTANCE BETWEEN THE EDGE OF SOLDER BALL AND WINDOW-SIDE ENCAPSULANT.

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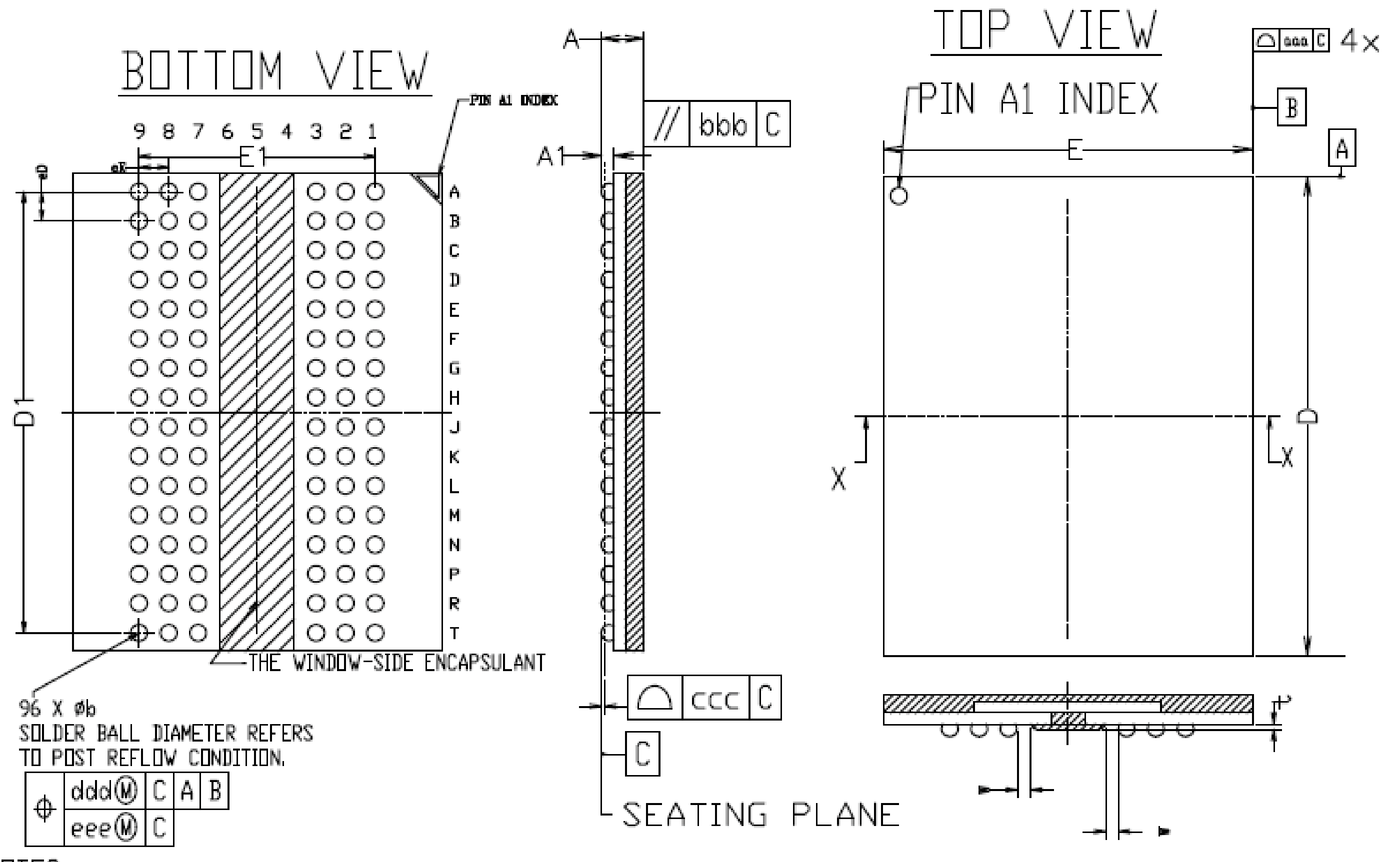
Figure 9 – 78-Ball BGA Package Outline (x8) Dimensions

DIMENSION REFERENCES Units mm

REF.	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.25	---	0.40
b	0.40	---	0.50
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1	9.60 BSC		
E1	6.40 BSC		
eE	0.80 BSC		
eD	0.80 BSC		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08
W	0.1	---	---
t	---	---	0.20

Figure 10 – 96-Ball BGA Package Outline (x16)



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'eE' & 'eD' REPRESENT THE BASIC SOLDER BALL GRID PITCH
3. 'b' IS MEASURABLE AT THE MAXIMUN SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C. THE SOLDER BALL DIAMETER IS Ø0.45mm BEFORE REFILOW.THE SOLDER BALL PAD Ø0.40mm
4. PRIMARY DATUM C ARE DEFINED BY THE SPHERICAL.
5. THE OVERALL PACKAGE THICKNESS 'A' ALREADY CONSIDER COLLAPSE.
6. PACKAGE DIMENSIONS CONFORM TO JEDEC MO-207.
7. THE DISTANCE BETWEEN THE TOP SURFACE OF SMALLEST SOLDER BALL (BALL HEIGHT) AND WINDOW-SIDE ENCAPSULANT MUST > 0.10mm.
8. THE HEIGHT OF WINDOW-SIDE ENCAPSULANT 't' COULD CHANGED ASSEMBLY HOUSE'S DESIGN,BUT IT MUST SATISFY THE REQUEST OF ITEM 7.
9. 'W' DEFINES THE DISTANCE BETWEEN THE EDGE OF SOLDER BALL AND WINDOW-SIDE ENCAPSULANT.

Figure 11 – 96-Ball BGA Package Outline (x16) Dimensions

DIMENSION REFERENCES Units mm

REF.	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.25	---	0.40
b	0.40	---	0.50
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1		9.60 BSC	
E1		6.40 BSC	
eE		0.80 BSC	
eD		0.80 BSC	
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08
W	0.1	---	---
t	---	---	0.20

Table 17 – Revision History

Revision	Date	Description of Change
1.0	February 7, 2018	Published data sheet
1.1	March 6, 2018	Updated Table 15 and 16 to remove "T" OPN designation from tray parts
1.2	March 16, 2018	Updated OPN table to change T designation for tray to blank.
1.3	October 15, 2018	Added Figure 3 and included additional details for x16 device

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