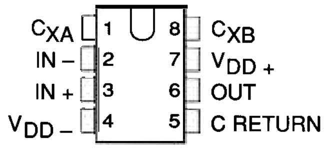
D3343, OCTOBER 1989

- Extremely Low Offset Voltage . . . 5 µV Max
- Extremely Low Change in Offset Voltage with Temperature . . . 0.003 µV/°C Typ
- Low Input Offset Current . . . 30 pA Max
- A_{VD} . . . 120 dB Min
- CMRR and k_{SVR} . . . 110 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

D, JG, OR P PACKAGE
(TOP VIEW)

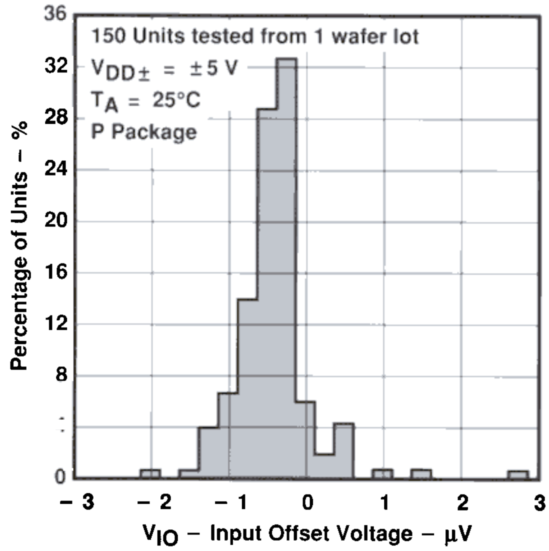


AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 µV	ICL7652D	ICL7652JG	ICL7652P

D package is available taped and reeled. Add "R" suffix to device type (i.e., ICL7652DR).

DISTRIBUTION OF ICL7652
INPUT OFFSET VOLTAGE



description

The ICL7652 is a precision chopper-stabilized operational amplifier manufactured using Texas Instruments Advanced LinCMOS™ process. This process, in conjunction with unique chopper-stabilization circuitry, produces an operational amplifier whose performance matches or exceeds that of similar devices available today.

Chopper stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even with variations in temperature, time, common-mode voltage, and supply voltage. Additionally, low-frequency noise voltage is significantly reduced. This precision, coupled with the extremely high input impedance of the CMOS input stage, makes the ICL7652 an ideal choice for low-level signal-processing applications such as strain gauges, thermocouples, and other transducer amplifiers.

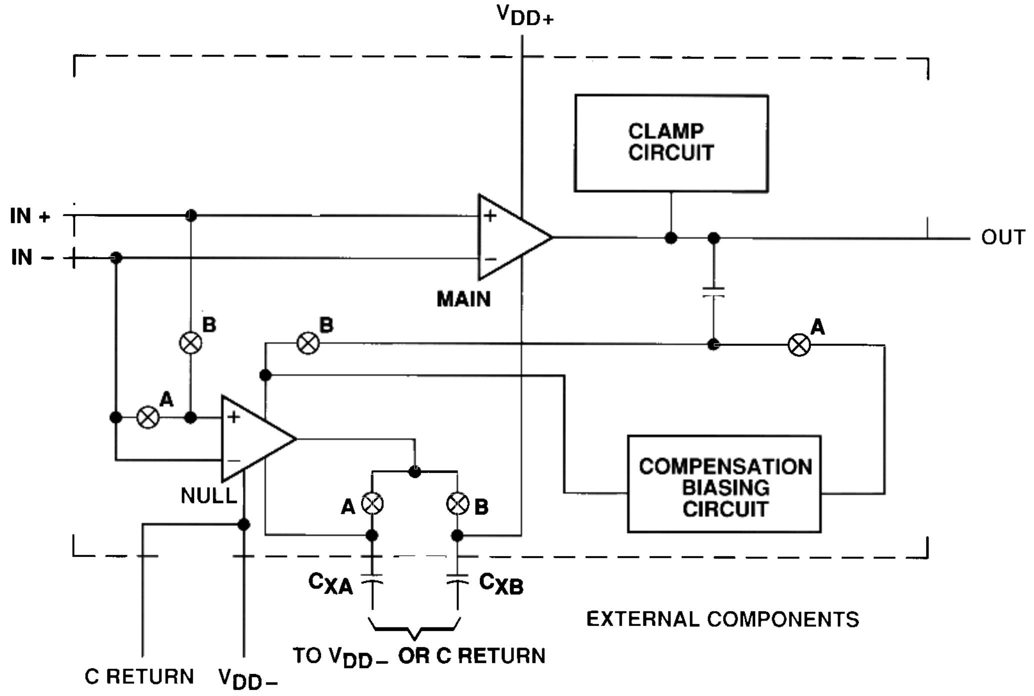
The ICL7652 input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at supply voltages as low as ±1.9 V. The ICL7652 also features fast overload recovery time. Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latchup. Additionally, the ICL7652 incorporates internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

The ICL7652 is characterized for operation from 0°C to 70°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . 8 V
Supply voltage, V_{DD-} . . . . −8 V
Differential input voltage (see Note 2) . . . . ±16 V
Input voltage range, V_I (any input) . . . . ±8 V
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	1050 mW	8.4 mW/°C	672 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	± 1.9	± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.9$	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	5	µV
			Full range			7.25	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.05	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2	30	pA
			Full range			100	
I_{IB}	Input bias current		25°C		4	30	pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ	25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	120	150		dB
			Full range	114			
f_{ch}	Internal chopping frequency		25°C		450		Hz
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	110	140		dB
			Full range	104			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ±1.9 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	110	135		dB
			Full range	104			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4	mA
			Full range			3.5	

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		V/µs
			Full range	1.5			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		V/µs
			Full range	1.8			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		94		nV/√Hz
		f = 1 kHz	25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8		µV
		f = 0 to 10 Hz	25°C		2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is 0°C to 70°C.
NOTE 5: This parameter is tested on a sample basis for the ICL7652. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
I_{IB}	Input bias current	vs Common-mode input voltage	1
		vs Temperature	2
I_{IO}	Input offset current	vs Temperature	3
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	4
V_{OM}	Maximum peak output voltage swing	vs Output current	5, 6
		vs Temperature	7, 8
A_{VD}	Differential voltage amplification	vs Frequency	9
		vs Temperature	10
I_{DD}	Supply current	vs Supply voltage	11
		vs Temperature	12
I_{OS}	Short-circuit output current	vs Supply voltage	13
		vs Temperature	14
SR	Slew rate	vs Supply voltage	15
		vs Temperature	16
	Pulse response	Small-signal	17
		Large-signal	18
	Gain-bandwidth product	vs Supply voltage	19
		vs Temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
ϕ_m	Phase margin	vs Supply voltage	22
		vs Temperature	23
		vs Load capacitance	24
	Phase shift	vs Frequency	9

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

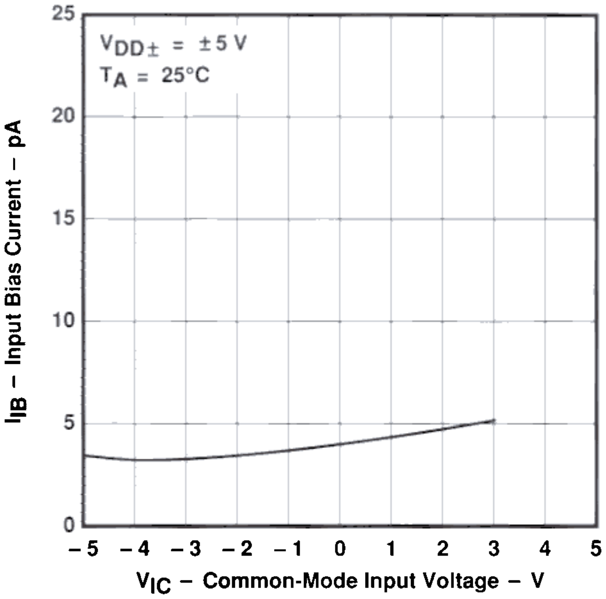


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

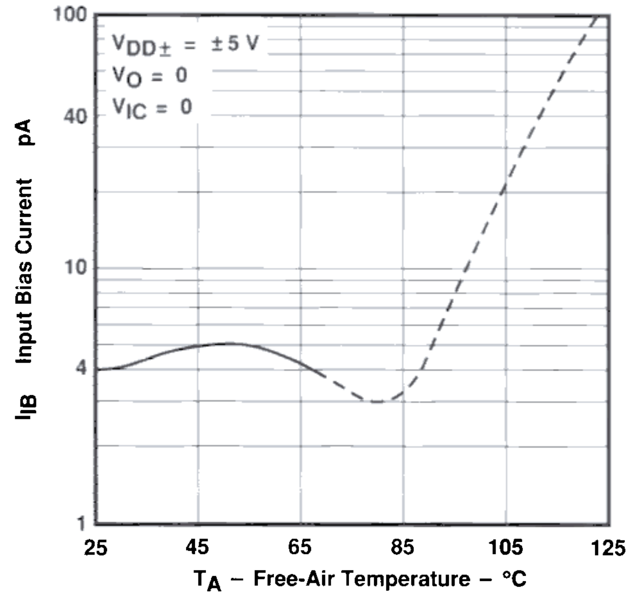


FIGURE 2

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

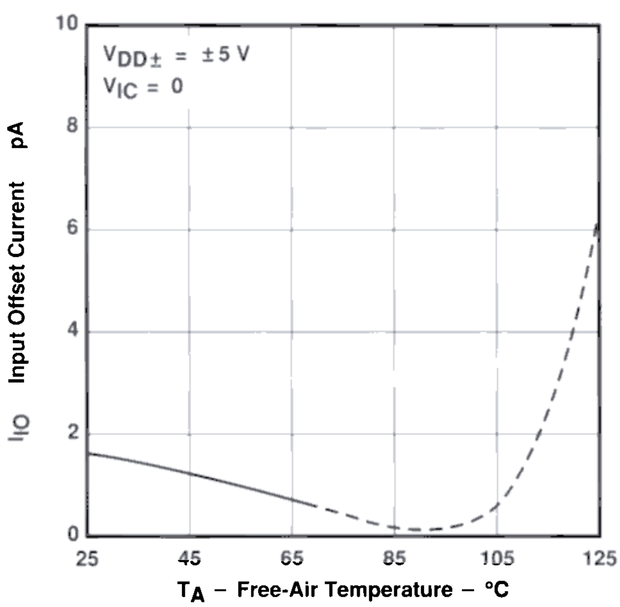


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

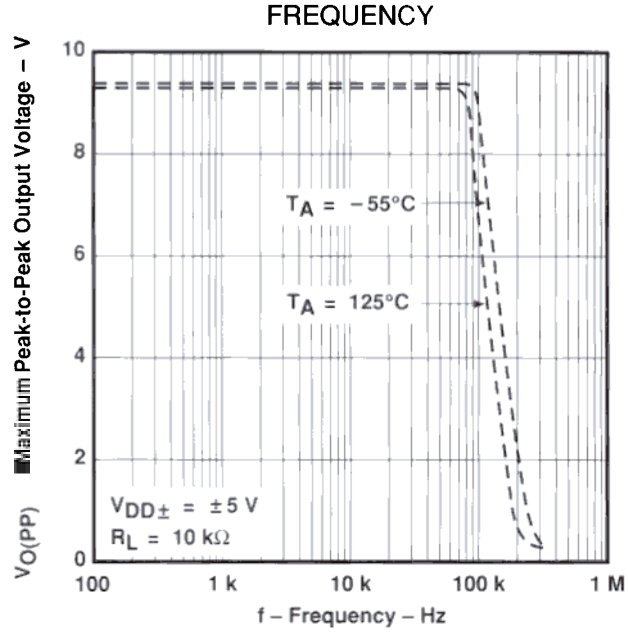


FIGURE 4

†Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from −55°C to 125°C.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

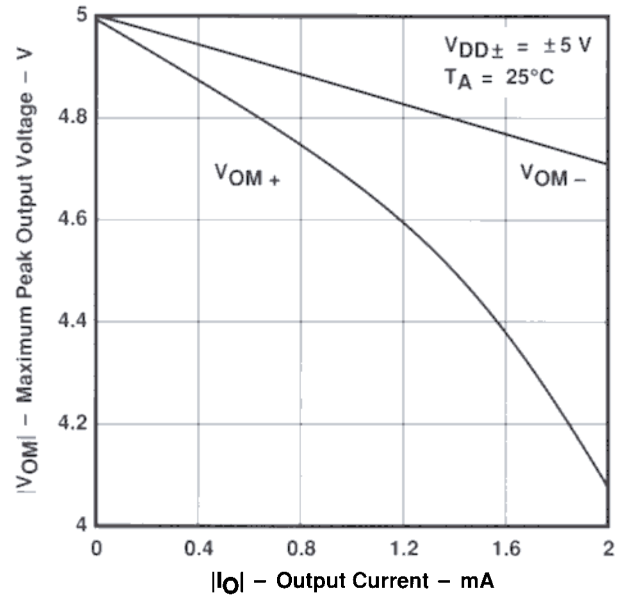

FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

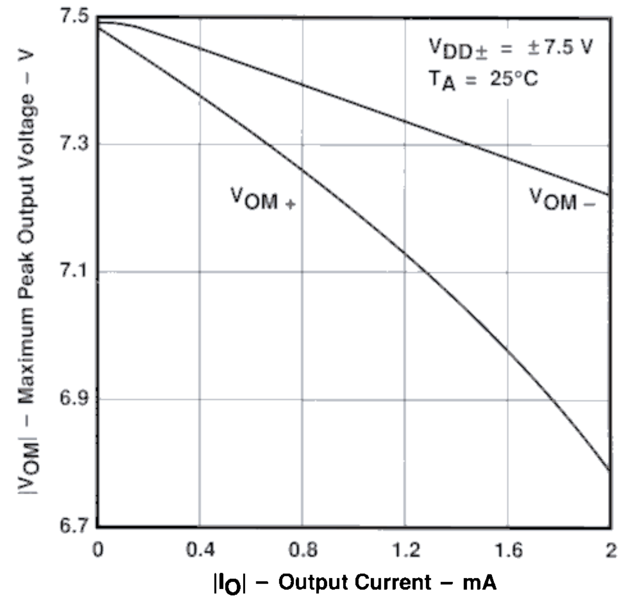

FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

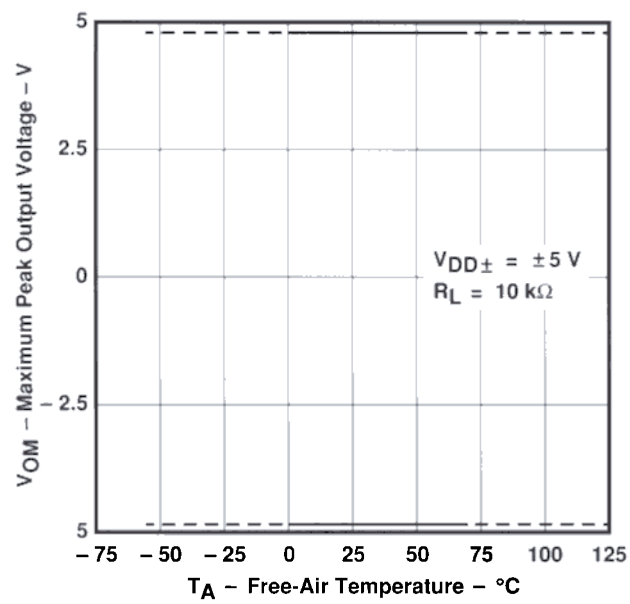

FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

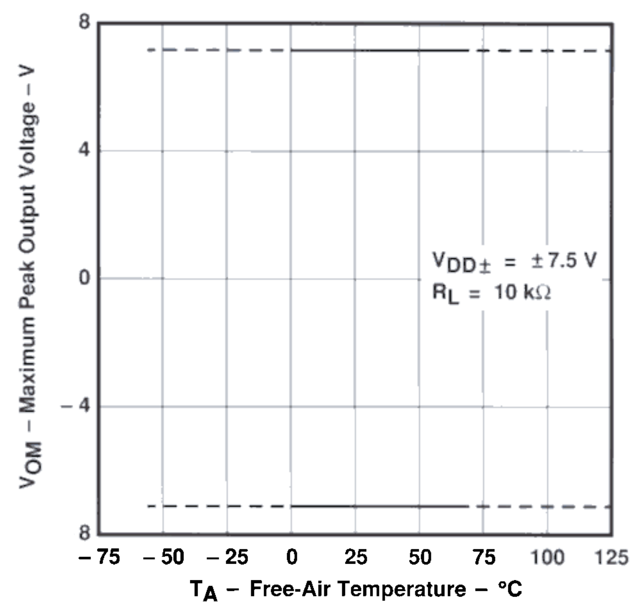

FIGURE 8

†Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from –55°C to 125°C.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

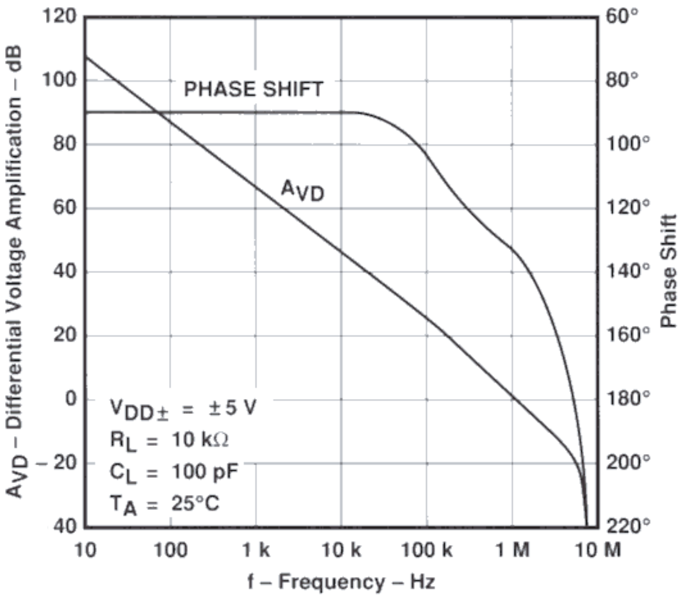

FIGURE 9

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

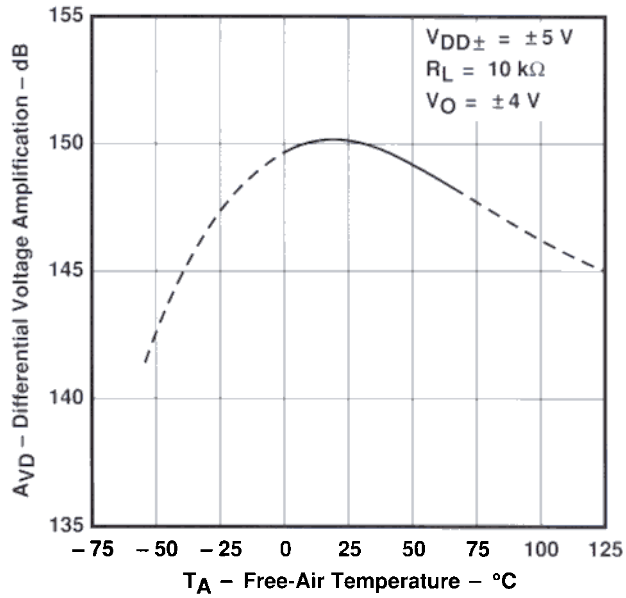

FIGURE 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

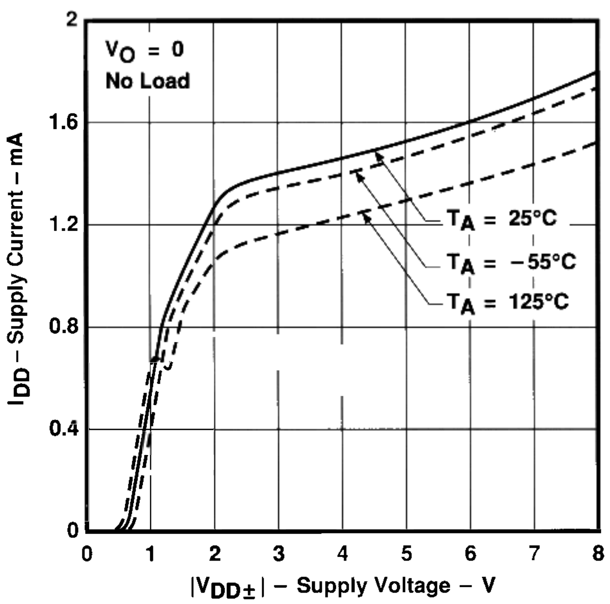

FIGURE 11

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

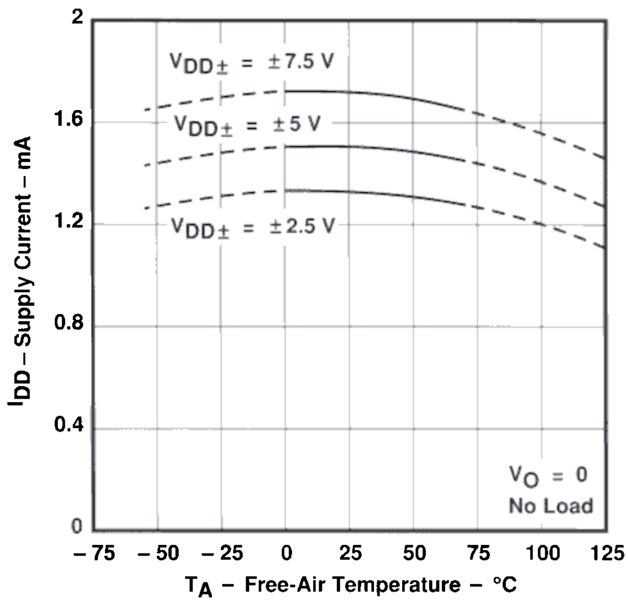

FIGURE 12

†Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from –55°C to 125°C.

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TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

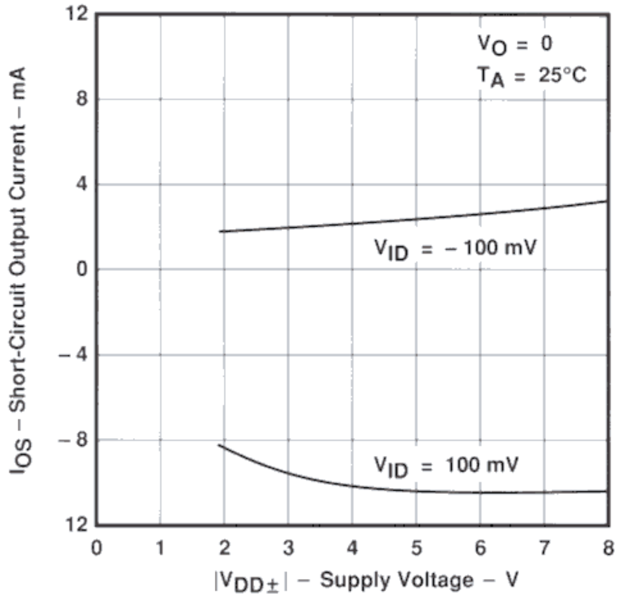

FIGURE 13

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

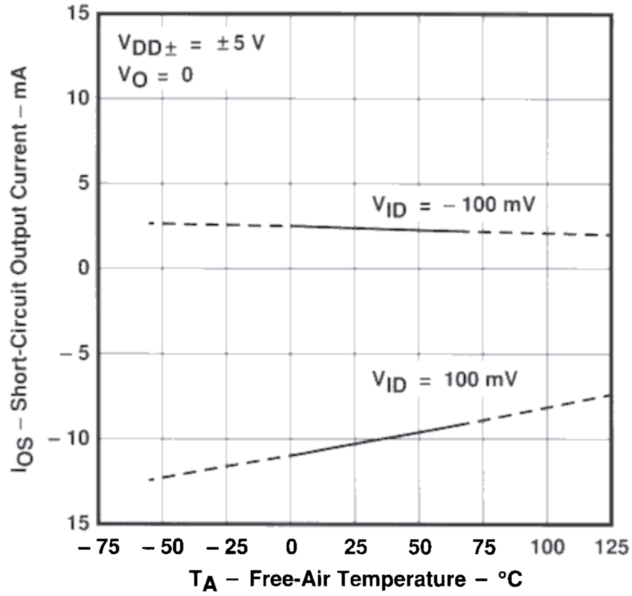

FIGURE 14

SLEW RATE
vs
SUPPLY VOLTAGE

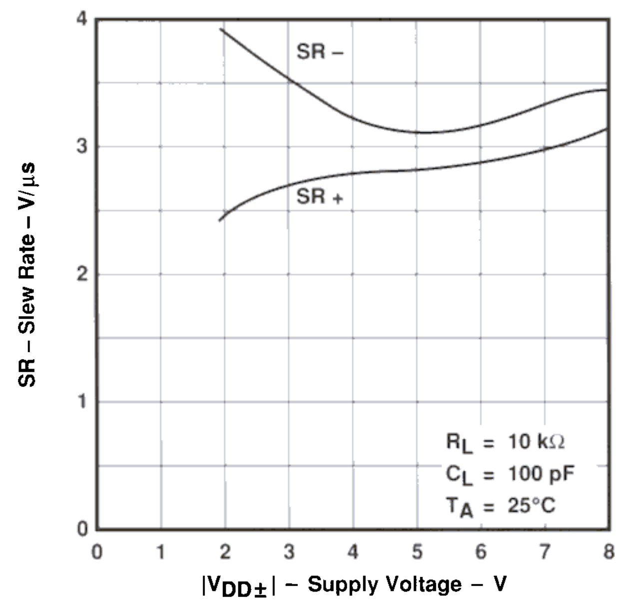

FIGURE 15

SLEW RATE
vs
FREE-AIR TEMPERATURE

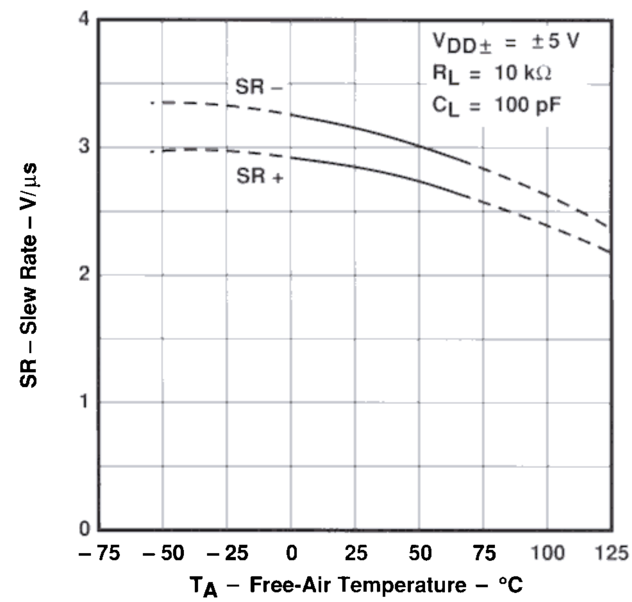

FIGURE 16

†Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from –55°C to 125°C.

TYPICAL CHARACTERISTICS†

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

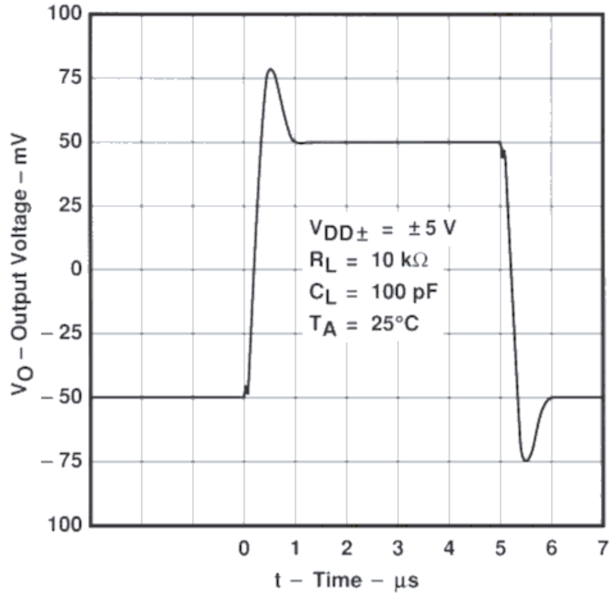

FIGURE 17

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

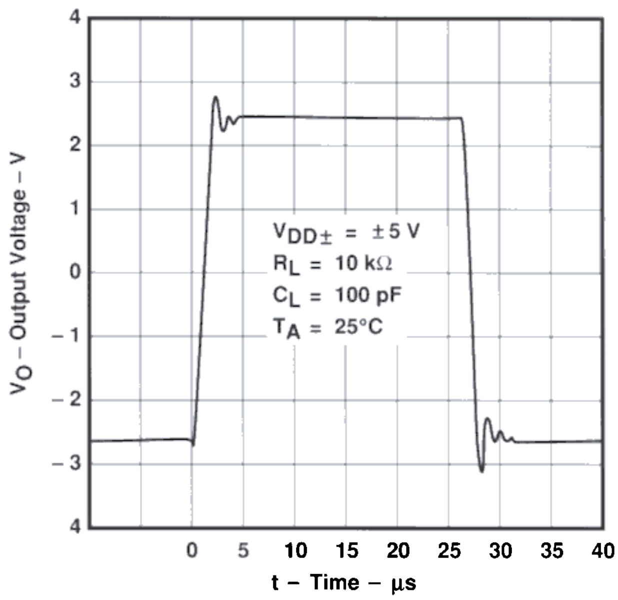

FIGURE 18

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

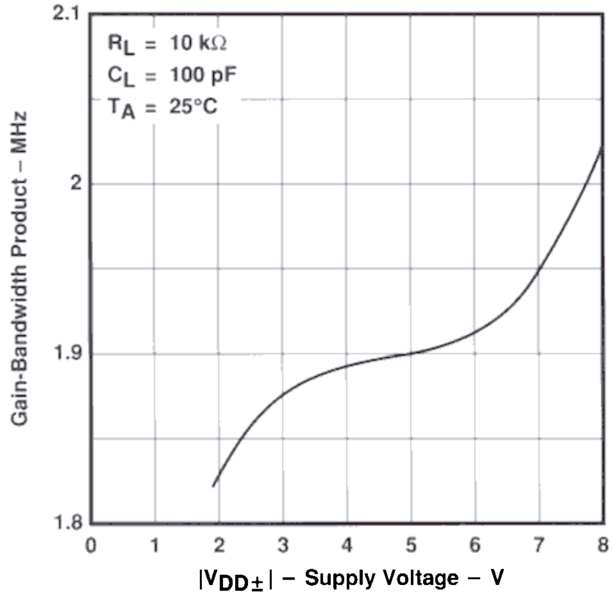

FIGURE 19

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

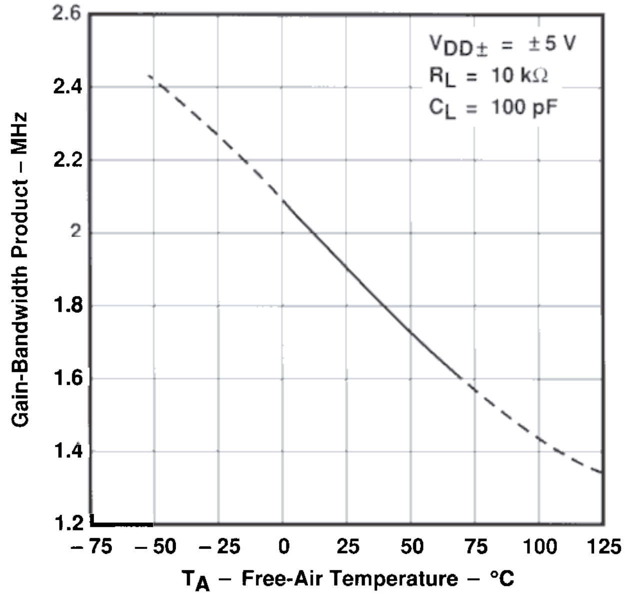

FIGURE 20

† Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from –55°C to 125°C.

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TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

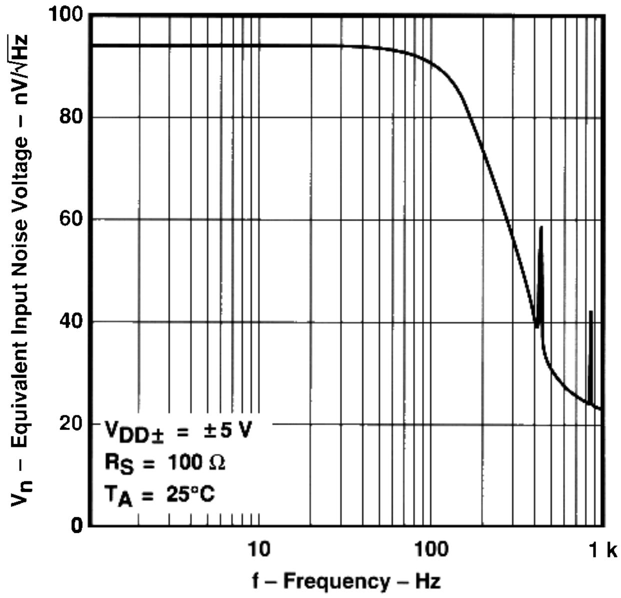

FIGURE 21

PHASE MARGIN
vs
SUPPLY VOLTAGE

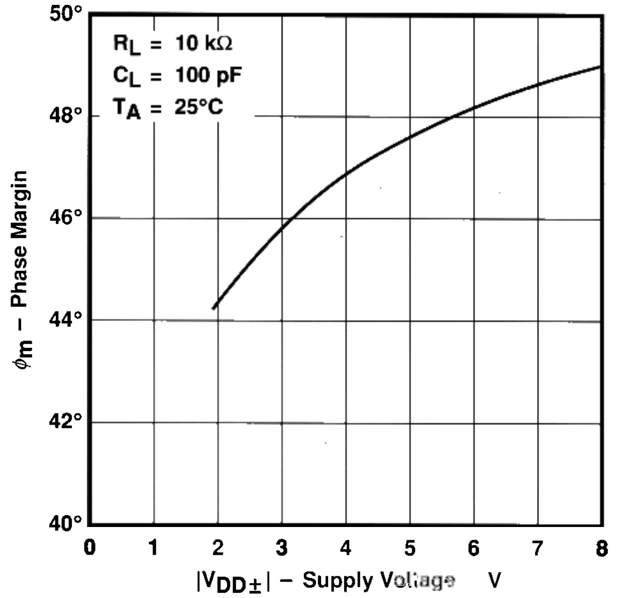

FIGURE 22

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

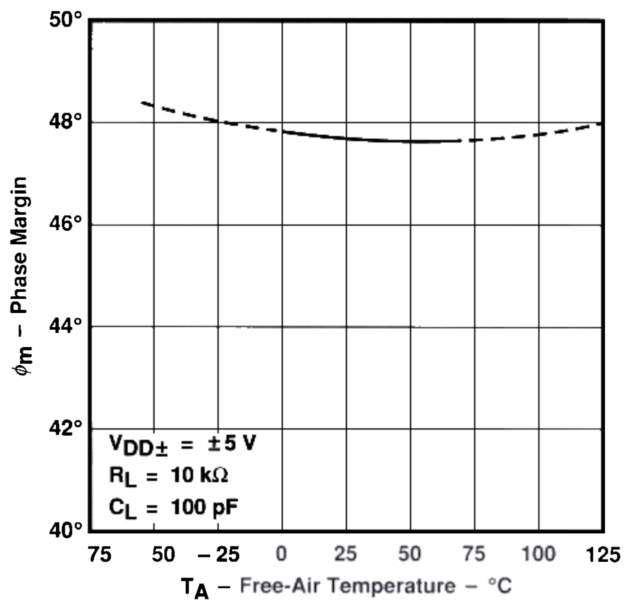

FIGURE 23

PHASE MARGIN
vs
LOAD CAPACITANCE

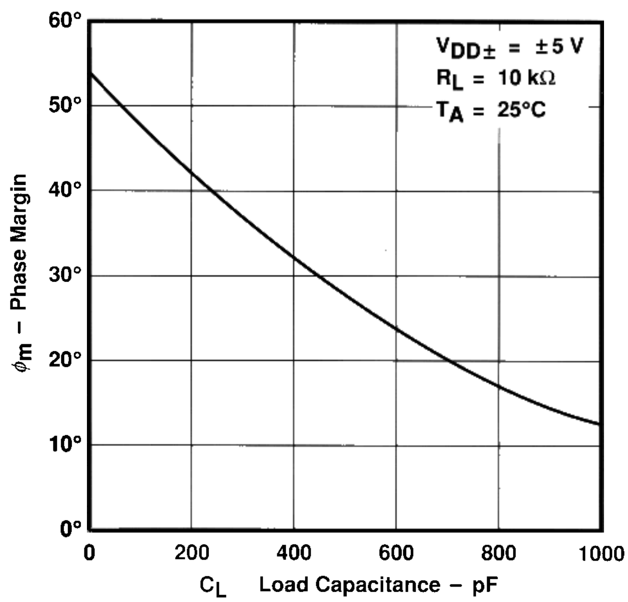

FIGURE 24

†Data at high and low temperatures are applicable to ICL7652 only within its noted operating free-air temperature range of 0°C to 70°C. The extended data have been retained to show typical performance of devices selected from the same process but characterized for operation from −55°C to 125°C.

TYPICAL APPLICATION DATA

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation that negate the performance advantages realized by using the ICL7652.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input offset voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the ICL7652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the ICL7652.

overload recovery/output clamp

When large differential input voltage conditions are applied to the ICL7652, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 25). Typical overload recovery time for the ICL7652 is significantly faster than that of competitive products.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the ICL7652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the ICL7652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

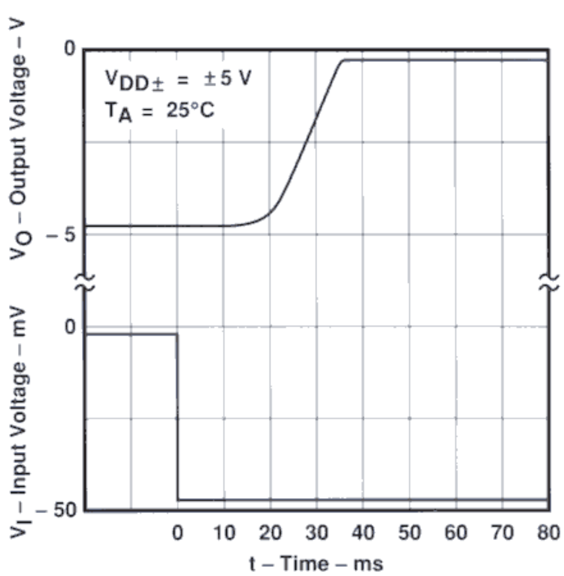

FIGURE 25. OVERLOAD RECOVERY

TYPICAL APPLICATION DATA

avoiding latchup

The ICL7652 inputs and output are designed to withstand –100-mA surge currents without sustaining latchup. However, because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by using decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The ICL7652 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the ICL7652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The ICL7652 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term “chopper-stabilized” derives from the process of switching between these two clock phases. Figure 26 shows a simplified block diagram of the ICL7652. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset-voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

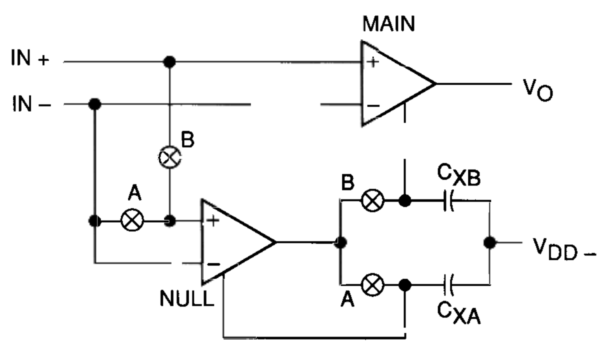

FIGURE 26. SIMPLIFIED BLOCK DIAGRAM

TYPICAL APPLICATION DATA

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS™ process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the ICL7652 by use of a patent-pending compensation circuit and the Advanced LinCMOS™ process.

The ICL7652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

temperature coefficient of input offset voltage

Figure 27 shows the effects of package-induced thermal EMF. The ICL7652 can null only the offset voltage within its nulling loop. There are metal-to-metal junctions outside the nulling loop (bonding wires, solder joints, etc.) that produce EMF. In Figure 27, an ICL7652 was placed in an oven at 25°C at t = 0, biased up, and allowed to stabilize. At t = 3 min, the oven was turned on and allowed to rise in temperature to 125°C. As evidenced by the curve, the overall change in input offset voltage with temperature is much less than the specified maximum limit of 0.05 μV/°C.

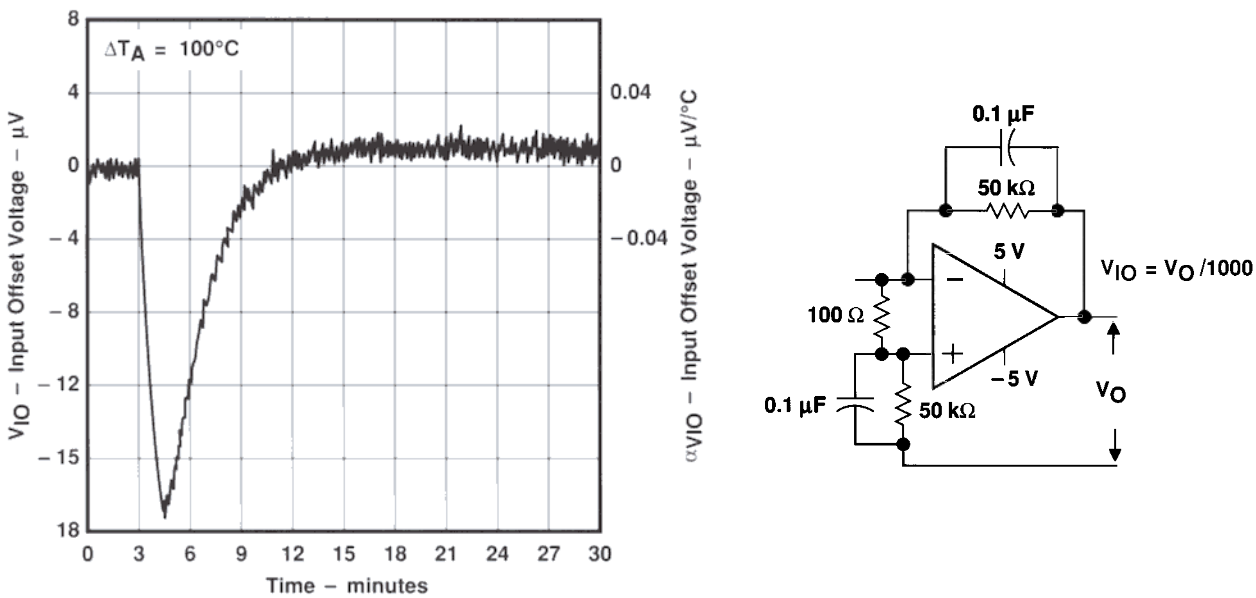

FIGURE 27. EFFECTS OF PACKAGE-INDUCED THERMAL EMF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ICL7652P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ICL7652PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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