



PJS6602

20V Complementary Enhancement Mode MOSFET

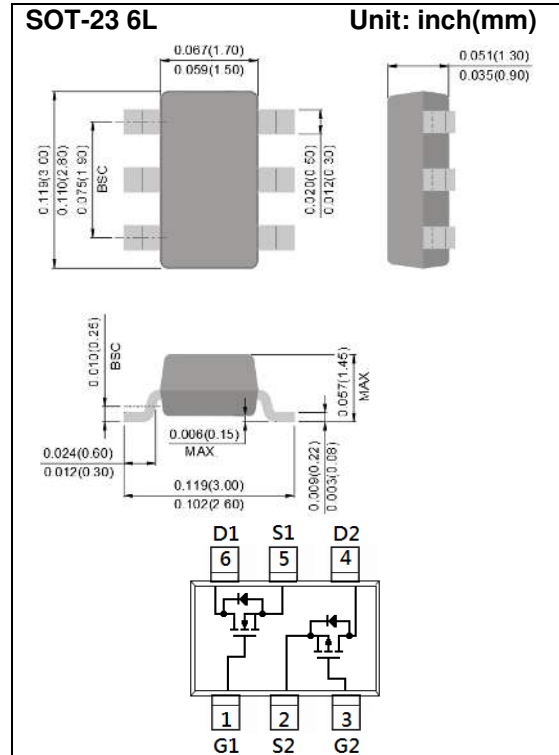
Voltage 20 / -20V **Current** 5.2 / -3.4A

Features

- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams
- Marking: SC2



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	±12	±12	V
Continuous Drain Current	I _D	5.2	-3.4	A
Pulsed Drain Current ^(Note 4)	I _{DM}	20.8	-13.6	A
Power Dissipation	P _D	1.25		W
		Derate above 25°C		10 mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150		°C
Typical Thermal Resistance	R _{θJA}	100		°C/W
- Junction to Ambient ^(Note 3)				



PJS6602

N-Channel Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.5	0.77	1.2	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =5.2A	-	29	36	mΩ
		V _{GS} =2.5V, I _D =3.2A	-	39	52	
		V _{GS} =1.8V, I _D =1.5A	-	58	92	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 5)						
Total Gate Charge	Q _g	V _{DS} =10V, I _D =5.2A, V _{GS} =4.5V ^(Note 1,2)	-	4.1	-	nC
Gate-Source Charge	Q _{gs}		-	1.1	-	
Gate-Drain Charge	Q _{gd}		-	0.7	-	
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1.0MHZ	-	396	-	pF
Output Capacitance	C _{oss}		-	54	-	
Reverse Transfer Capacitance	C _{rss}		-	40	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =10V, I _D =5.2A, V _{GS} =4.5V, R _G =6Ω ^(Note 1,2)	-	14	-	ns
Turn-On Rise Time	t _r		-	10	-	
Turn-Off Delay Time	t _{d(off)}		-	30	-	
Turn-Off Fall Time	t _f		-	7	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	1.5	A
Diode Forward Voltage	V _{SD}	I _S =1.0A, V _{GS} =0V	-	0.75	1.2	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing



PJS6602

P-Channel Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.4	-0.65	-1.2	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-3.4A	-	65	82	mΩ
		V _{GS} =-2.5V, I _D =-2.2A	-	82	110	
		V _{GS} =-1.8V, I _D =-1.2A	-	103	146	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-3.4A, V _{GS} =-4.5V (Note 1,2)	-	7	-	nC
Gate-Source Charge	Q _{gs}		-	1	-	
Gate-Drain Charge	Q _{gd}		-	1.8	-	
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1.0MHZ	-	522	-	pF
Output Capacitance	C _{oss}		-	55	-	
Reverse Transfer Capacitance	C _{rss}		-	40	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =-10V, I _D =-3.4A, V _{GS} =-4.5V, R _G =6Ω (Note 1,2)	-	10	-	ns
Turn-On Rise Time	t _r		-	4	-	
Turn-Off Delay Time	t _{d(off)}		-	34	-	
Turn-Off Fall Time	t _f		-	5	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	-1.5	A
Diode Forward Voltage	V _{SD}	I _S =-1.0A, V _{GS} =0V	-	0.77	-1.2	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
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N-Channel TYPICAL CHARACTERISTIC CURVES

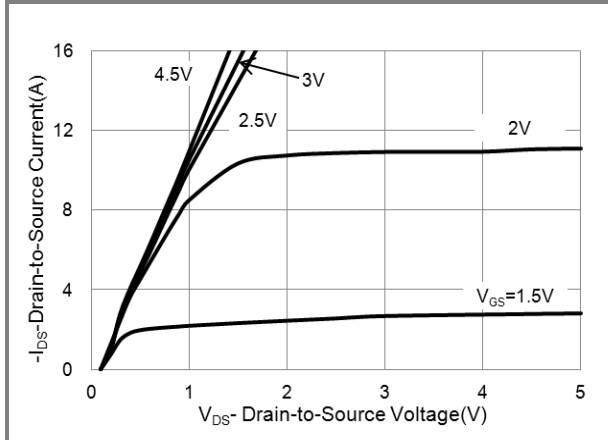


Fig.1 On-Region Characteristics

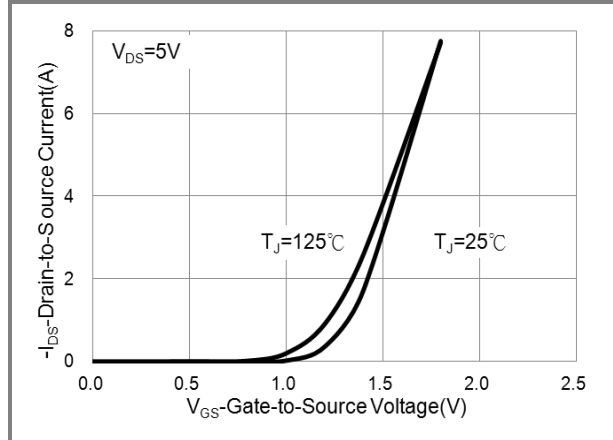


Fig.2 Transfer Characteristics

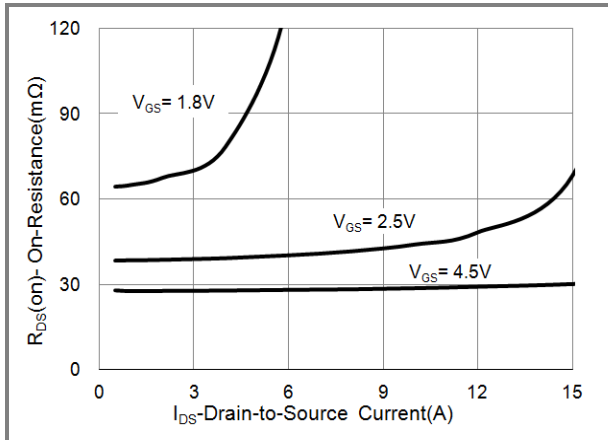


Fig.3 On-Resistance vs. Drain Current

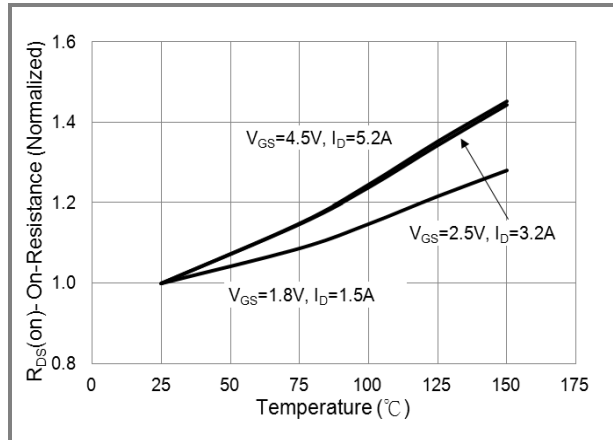


Fig.4 On-Resistance vs. Junction temperature

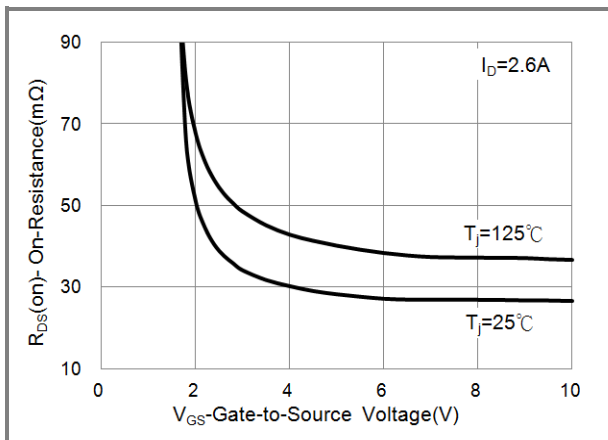


Fig.5 On-Resistance Variation with V_{G_S} .

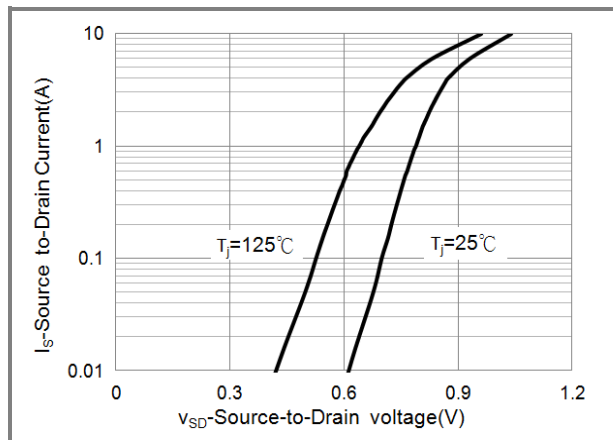


Fig.6 Body Diode Characteristics



PJS6602

N-Channel TYPICAL CHARACTERISTIC CURVES

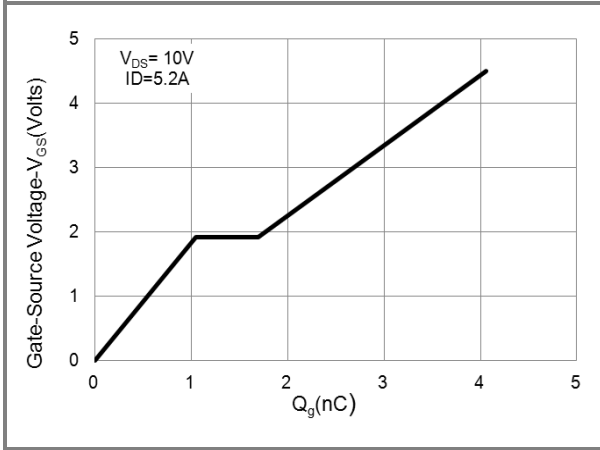


Fig.7 Gate-Charge Characteristics

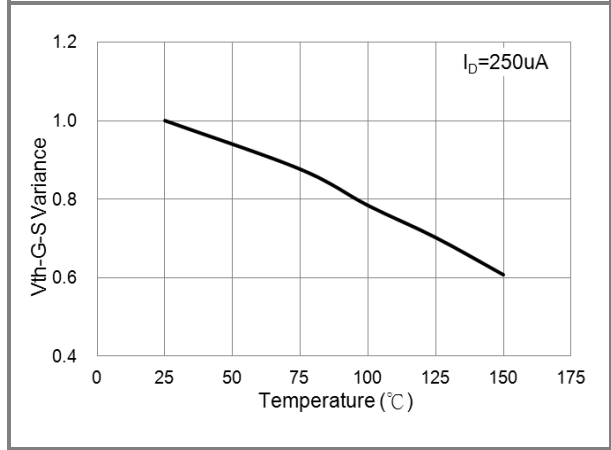


Fig.8 Threshold Voltage Variation with Temperature.

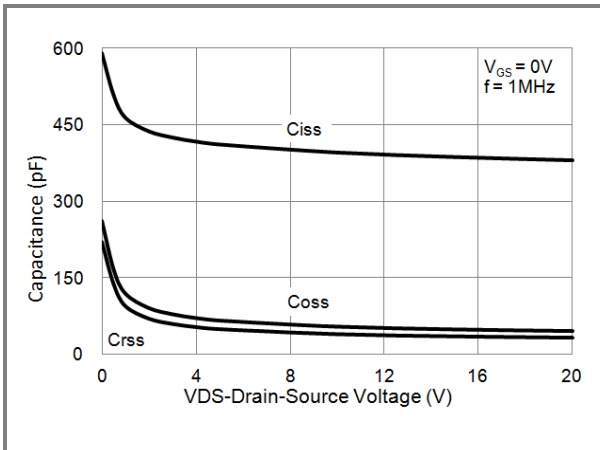


Fig.9 Capacitance vs. Drain-Source Voltage.



PJS6602

P-Channel TYPICAL CHARACTERISTIC CURVES

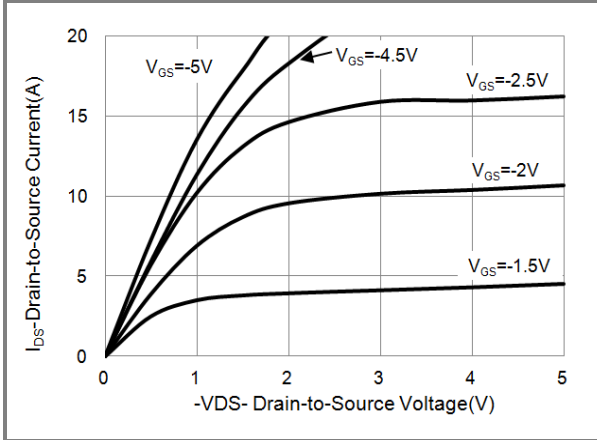


Fig.1 On-Region Characteristics

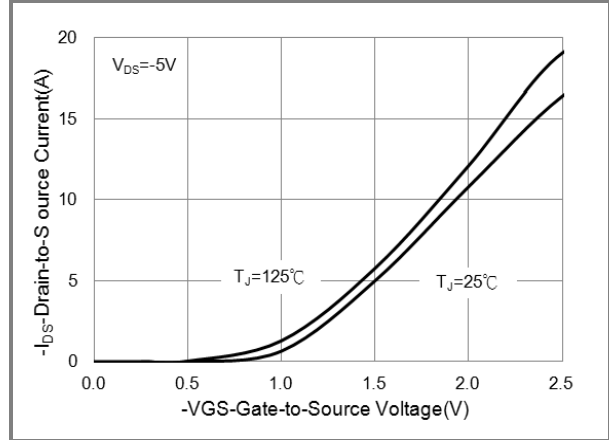


Fig.2 Transfer Characteristics

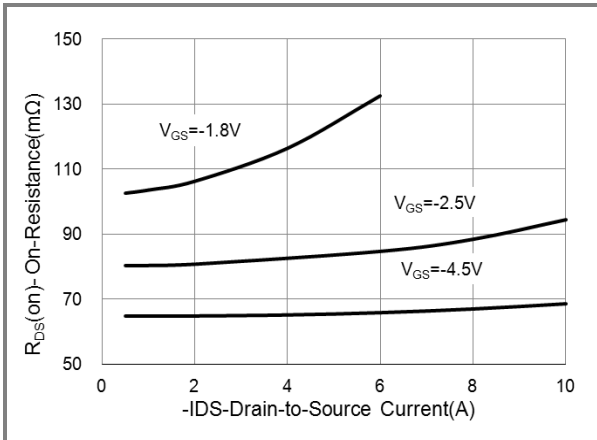


Fig.3 On-Resistance vs. Drain Current

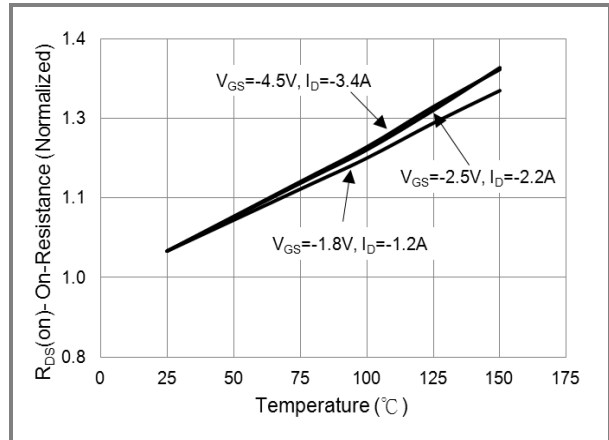


Fig.4 On-Resistance vs. Junction temperature

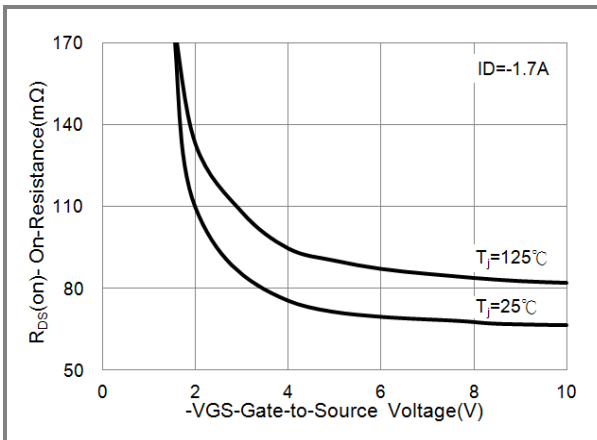


Fig.5 On-Resistance Variation with VGS.

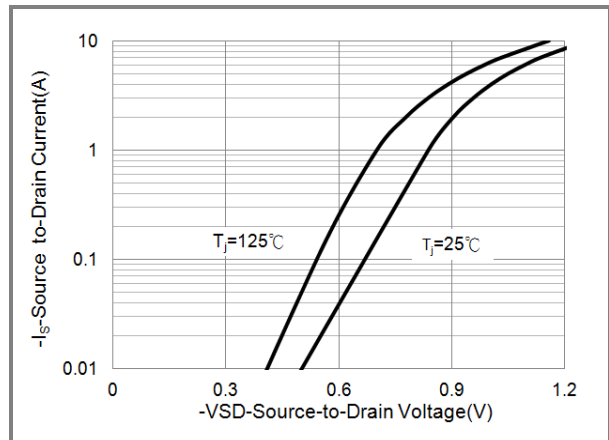


Fig.6 Body Diode Characteristics



PJS6602

P-Channel TYPICAL CHARACTERISTIC CURVES

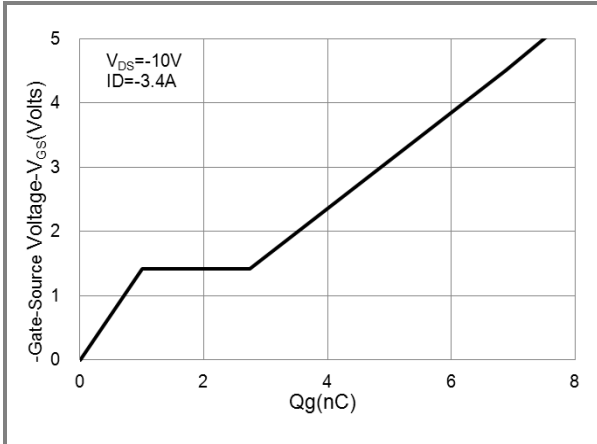


Fig.7 Gate-Charge Characteristics

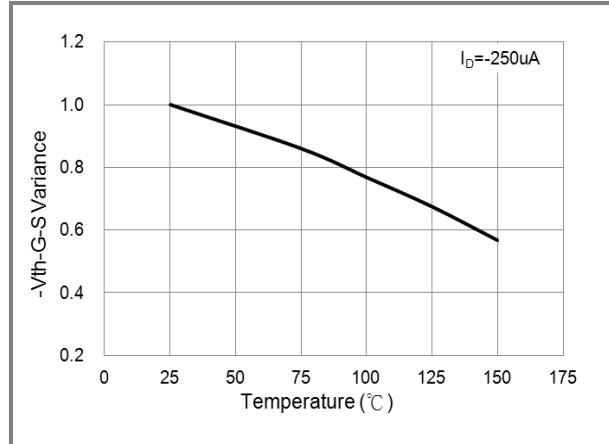


Fig.8 Threshold Voltage Variation with Temperature.

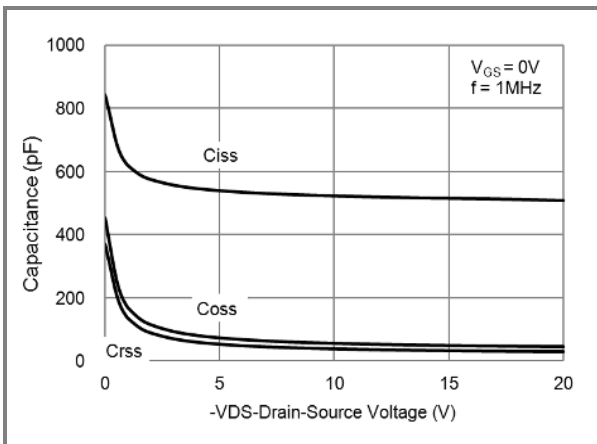


Fig.9 Threshold Voltage Variation with Temperature.

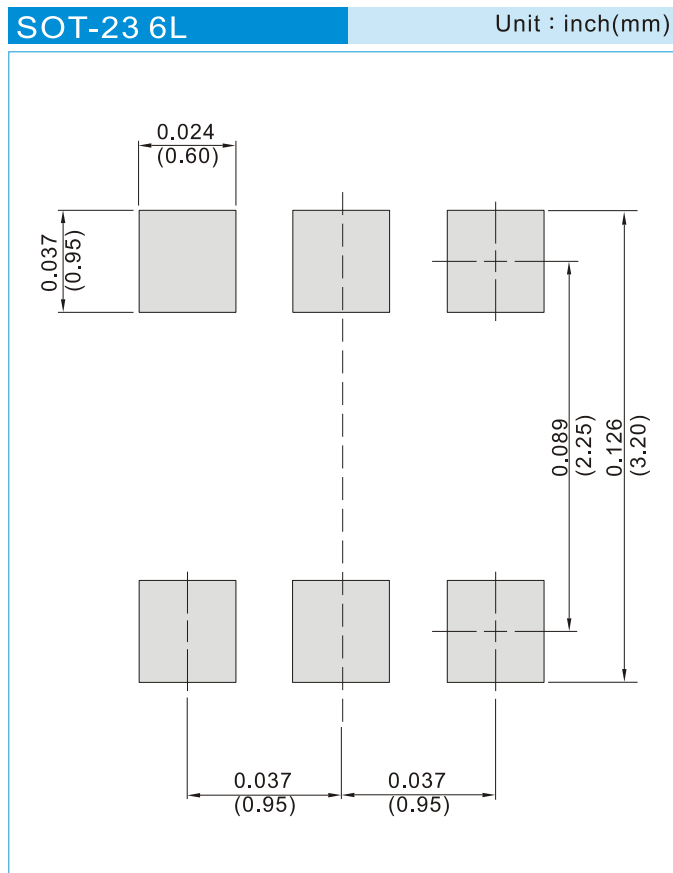


PJS6602

PART NO. PACKING CODE VERSION

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJS6602_S1_00001	SOT-23 6L	3K pcs / 7" reel	SC2	Halogen free RoHS compliant
PJS6602_S2_00001	SOT-23 6L	10K pcs / 13" reel	SC2	Halogen free RoHS compliant

MOUNTING PAD LAYOUT





PJS6602

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