# MP5090

## Low $I_Q$, Dual-Channel, 3A/2A Load Switch

The Future of Analog IC Technology

## DESCRIPTION

The MP5090 integrates dual load switches to provide load protection covering a 0.5V to 5.5V voltage range. Each channel provides up to 3A/2A of load protection covering a 0.5V to 5.5V voltage range with a 1.85V VCC power supply. With a small $R_{DS(ON)}$ in a tiny package, the MP5090 provides a highly efficient and space-saving solution for notebook, tablet, and other portable device applications.

With an internal soft-start function, the MP5090 can prevent inrush current during circuit start-up. The MP5090 also provides internal current limit, hiccup protection, and thermal shutdown features. The MP5090 also parallels both channels easily to double the current capability.

The MP5090 is available in TQFN-8 (1.5mmx2.0mm) and 8-ball CSP (1.05mmx1.60mm) packages.

## FEATURES

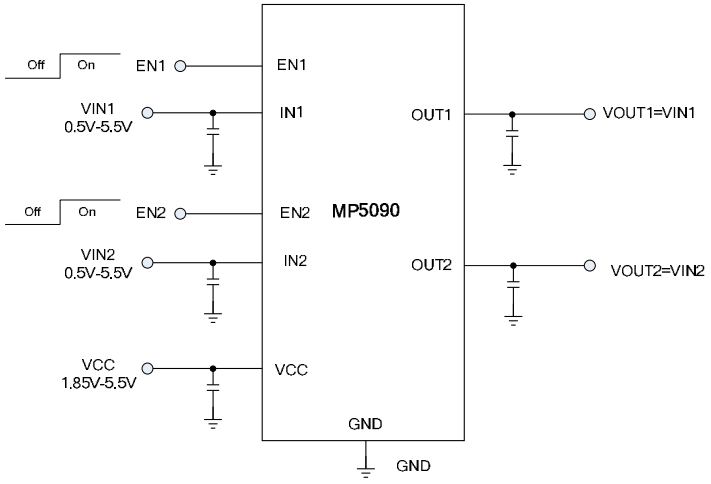
- Low Quiescent Current: 40μA
- Wide $V_{IN}$ Range from 0.5V to 5.5V
- <1μA Shutdown Current
- Output Discharge Function
- Continuous Current Capability
  - MP5090GQHT: 3A
  - MP5090GC: 2A
- Integrated Low $R_{DS(ON)}$ MOSFETs
  - MP5090GQHT: 20mΩ
  - MP5090GC: 30mΩ
- Enable Pin (EN1, EN2)
- Short-Circuitry Response Protection
- Easily Parallel-Connect Dual Channel
- Supports Reverse Block Connection
- Thermal Protection
- Available in TQFN-8 (1.5mmx2.0mm) and 8-Ball CSP (1.05mmx1.60mm) Packages

## APPLICATIONS

- Notebook and Tablet Computers
- Portable Devices
- Solid-State Drives
- Handheld Devices



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MP5090GQHT* | TQFN (1.5mmx2.0mm) | See Below |
| MP5090GC** | CSP (1.05mmx1.60mm) | See Below |

* For Tape & Reel, add suffix –Z (e.g. MP5090GQHT–Z)
** For Tape & Reel, add suffix –Z (e.g. MP5090GC–Z)

## TOP MARKING (MP5090GQHT )

EE
LL

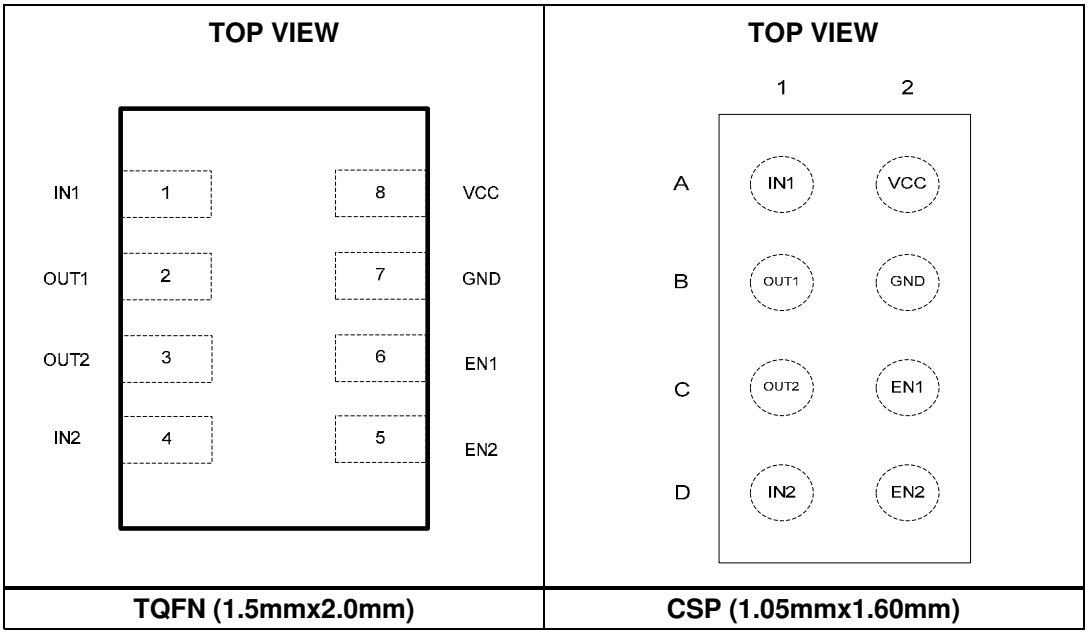
EE: Product code of MP5090GQHT
LL: Lot number

## TOP MARKING (MP5090GC)

EMY
LLL

EM: Product code of MP5090GC
Y: Year code
LLL: Lot number

## PACKAGE REFERENCE




| TQFN (1.5mmx2.0mm) | CSP (1.05mmx1.60mm) |
|---|---|

## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN1/2}$ .....-0.3V to +6V
VCC .....-0.3V to +6V
$V_{OUT1/2}$ .....-0.3V to +6V
All other pins .....-0.3V to +6V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation **(2)(4)(5)**
TQFN (1.5mmx2.0mm)..... 3.4W
CSP (1.05mmx1.60mm) ..... 1.7W

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN1/2}$).....0.5V to 5.5V
Supply voltage (VCC) .....1.85V to 5.5V
Output voltage ($V_{OUT1/2}$).....0.5V to 5.5V
Operating junction temp. ($T_J$)... -40°C to +125°C

| ***Thermal Resistance*(2)** | ***$\theta_{JA}$*** | ***$\theta_{JC}$*** | |
|---|---|---|---|
| EV5090-C-00A(4) | 69 | 28 | °C/W |
| TQFN-8 (1.5mmx2.0mm)(6) | 110 | 55 | °C/W |
| EV5090-Q-00A(5) | 35 | 6 | °C/W |
| CSP (1.05mmx1.60mm)(6) | 170 | NA | °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV5090-C-00A, 2-layer PCB.
5) Measured on EV5090-Q-00A, 2-layer PCB.
6) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 3.6V, VCC = 3.6V, $T_J$ = -40°C to +125°C, Typical value is tested at $T_J$ = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input and Supply Voltage Range** | | | | | | |
| Input voltage | $V_{IN1/2}$ | | 0.5 | | 5.5 | V |
| Supply voltage | $V_{CC}$ | | 1.85 | | 5.5 | V |
| **Supply Current (Single Channel)** | | | | | | |
| Off state leakage current | $I_{OFF}$ | $V_{IN}$ = 5V, EN = 0, $T_J$ = 25°C | | | 1 | μA |
| VCC standby current | $I_{STBY}$ | VCC = 3.6V, EN = 0, $T_J$ = 25°C | | 0.1 | 1 | μA |
| | | VCC = 3.6V, enable, no load | | 40 | | |
| **Power MOSFET** | | | | | | |
| On resistance | $R_{DSON1/2}$ | TQFN, VCC = 5.0V, single channel | | 20 | | mΩ |
| | | TQFN, VCC = 3.3V, single channel | | 24 | | |
| | $R_{DSON1/2}$ | CSP, VCC = 5.0V, single channel | | 30 | | |
| | | CSP, VCC = 3.3V, single channel | | 35 | | |
| **Thermal Shutdown and Recovery** | | | | | | |
| Shutdown temperature (5) | $T_{STD}$ | | | 155 | | °C |
| Hysteresis (5) | $T_{HYS}$ | | | 30 | | °C |
| **Under-Voltage Lockout (UVLO) Protection** | | | | | | |
| VCC under-voltage lockout threshold | $V_{CC\ UVLO}$ | UVLO rising threshold | | 1.7 | 1.85 | V |
| UVLO hysteresis | $V_{UVLOHYS}$ | | | 100 | | mV |
| **Soft Start (SS)** | | | | | | |
| Vo rise time | $T_{ss}$ | Vo = 3.6V, 10% to 90% | | 30 | | μs |
| EN turn on time | $T_{DELAY}$ | | | 30 | | μs |
| **Enable (ENx)** | | | | | | |
| EN rising threshold | $V_{ENH}$ | | | 1 | 1.2 | V |
| EN hysteresis | $V_{ENHYS}$ | | | 200 | | mV |
| EN resistance | | Between EN and GND | | 1 | | MΩ |
| **ILIM** | | | | | | |
| Current limit (5) | $I_{LIM}$ | TQFN package, VCC = 5V, $T_J$ = 25°C | 3.2 | 3.6 | | A |
| | | CSP package, VCC = 5V, $T_J$ = 25°C | 2.1 | 2.5 | | A |
| Hiccup on time | $T_{ON}$ | | | 2 | | ms |
| Hiccup off time | $T_{OFF}$ | | | 90 | | ms |
| **Discharge Resistance (Single Channel)** | | | | | | |
| Resistance | $R_{DIS}$ | | | 50 | | Ω |

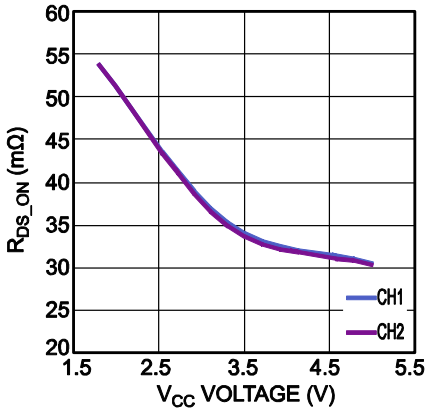
**NOTE:**

7) Guaranteed by characterization, not tested in production.

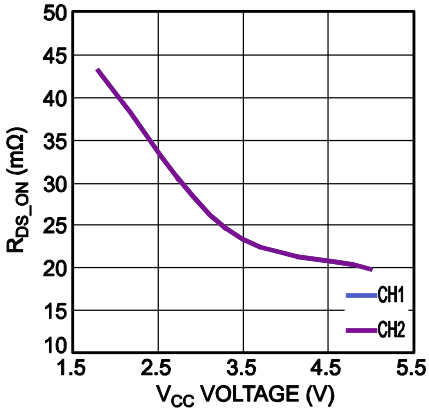
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 3.6V, VCC = 3.6V, $T_A$ = 25°C, unless otherwise noted.**

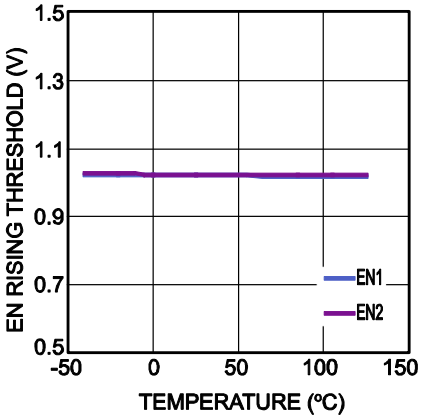
### $R_{DS(ON)}$ vs. VCC (CSP)



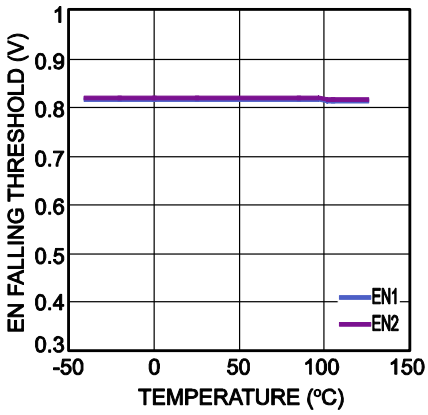

### $R_{DS(ON)}$ vs. VCC (TQFN)



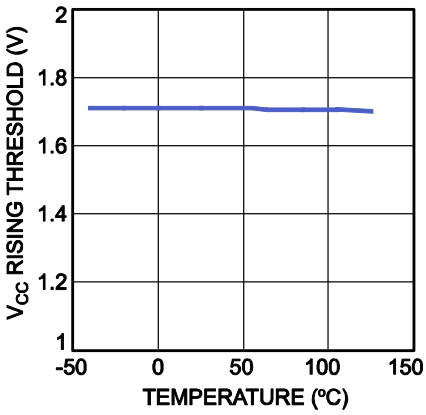

### EN Rising Threshold



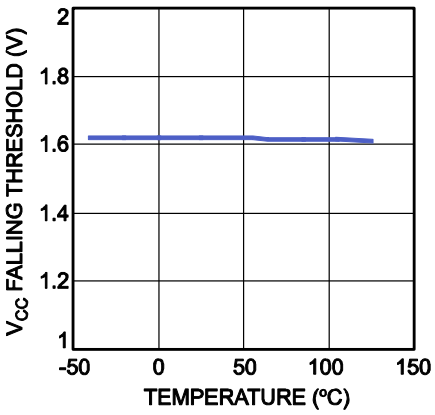

### EN Falling Threshold




### VCC Rising Threshold



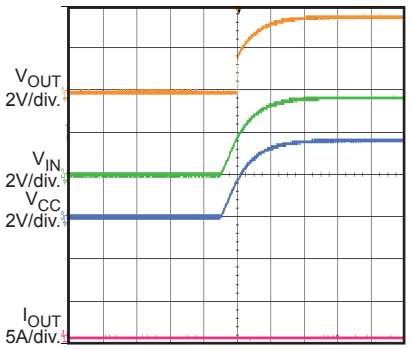

### VCC Falling Threshold



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

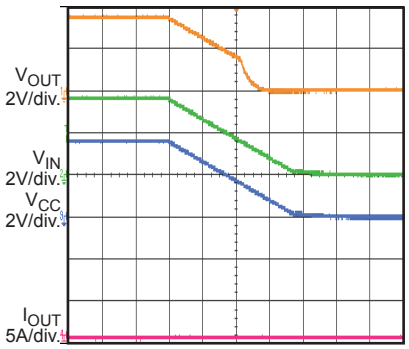
**$V_{IN}$ = 3.6V, VCC = 3.6V, $T_A$ = 25°C, for MP5090GQHT, unless otherwise noted.**

### $V_{IN}$ Start-Up
with No Load



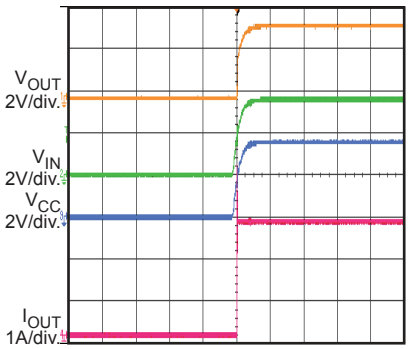

5ms/div.

### $V_{IN}$ Shutdown
with No Load



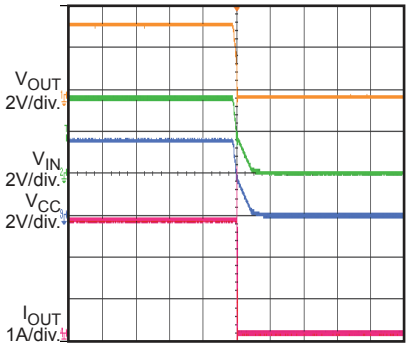

5ms/div.

### $V_{IN}$ Start-Up
with 3A Load



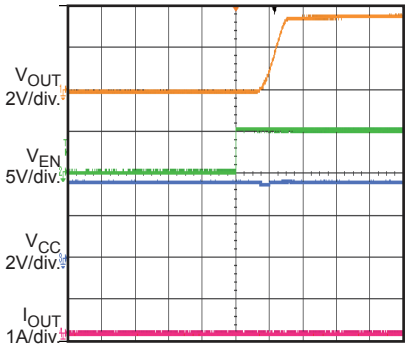

20ms/div.

### $V_{IN}$ Shutdown
with 3A Load



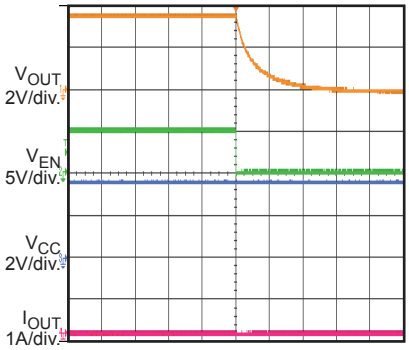

20ms/div.

### EN Start-Up
with No Load



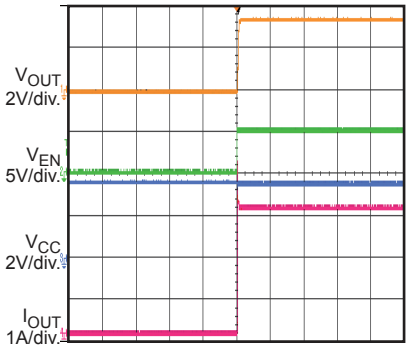

50µs/div.

### EN Shutdown
with No Load



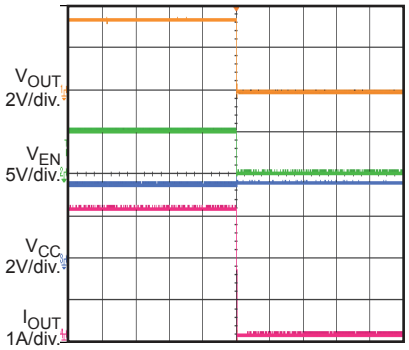

1ms/div.

### EN Start-Up
with 3A Load



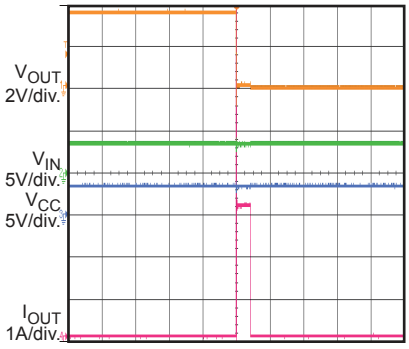

2ms/div.

### EN Shutdown
with 3A Load




2ms/div.

### Short Enter

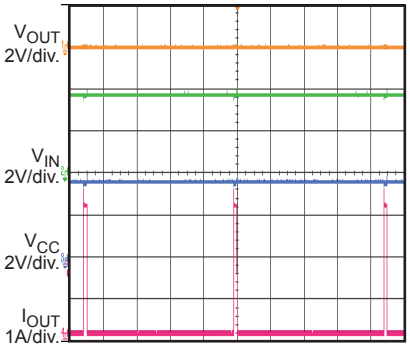



5ms/div.

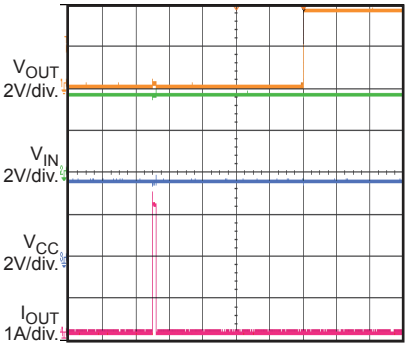
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 3.6V, VCC = 3.6V, $T_A$ = 25°C, for MP5090GQHT, unless otherwise noted.**

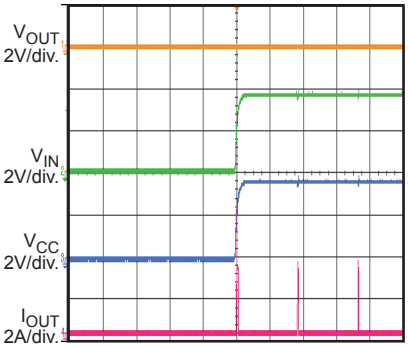
### Short Steady State



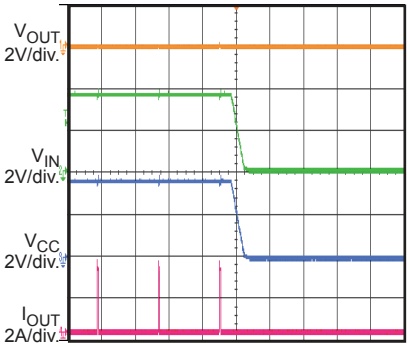

### Short Recovery



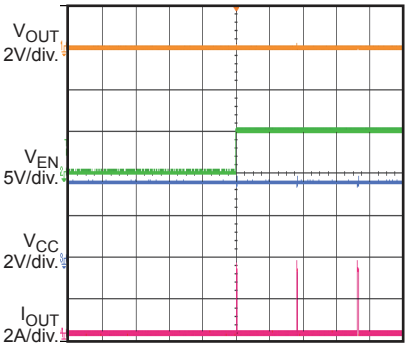

### $V_{IN}$ Start-Up with Short



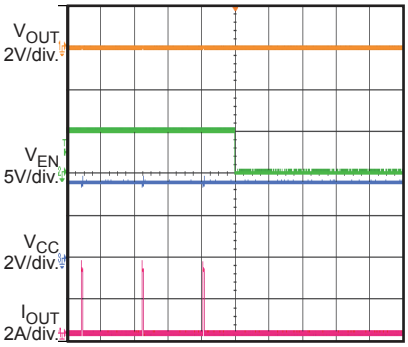

### $V_{IN}$ Shutdown with Short



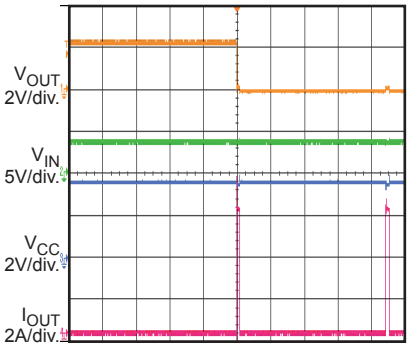

### EN Start-Up with Short



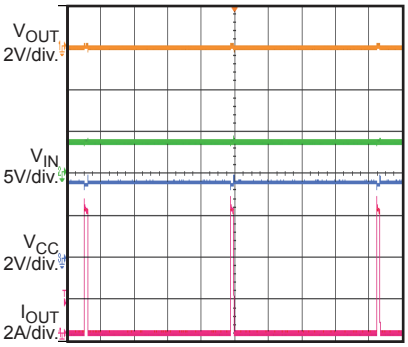

### EN Shutdown with Short



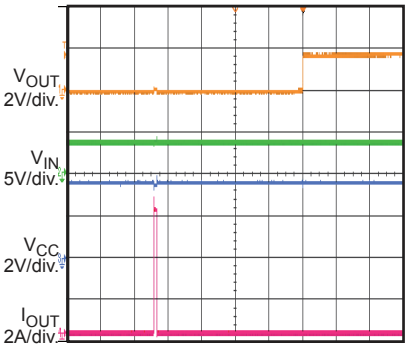

### Short Enter (Parallel)




### Short Steady (Parallel)




### Short Recovery (Parallel)



## PIN FUNCTIONS

| Package Pin # | | Name | Description |
|---|---|---|---|
| TQFN | CSP | | |
| 1 | A1 | IN1 | **Input power supply of switch 1.** |
| 2 | B1 | OUT1 | **Output to the load of switch 1.** |
| 3 | C1 | OUT2 | **Output to the load of switch 2.** |
| 4 | D1 | IN2 | **Input power supply of switch 2.** |
| 5 | D2 | EN2 | **Enable input of switch 2.** Pull EN2 below the specified threshold to shut the chip down. |
| 6 | C2 | EN1 | **Enable input of switch 1.** Pull EN1 below the specified threshold to shut the chip down. |
| 7 | B2 | GND | **Ground.** |
| 8 | A2 | VCC | **Load switch supply voltage to the control circuitry.** |

## BLOCK DIAGRAM

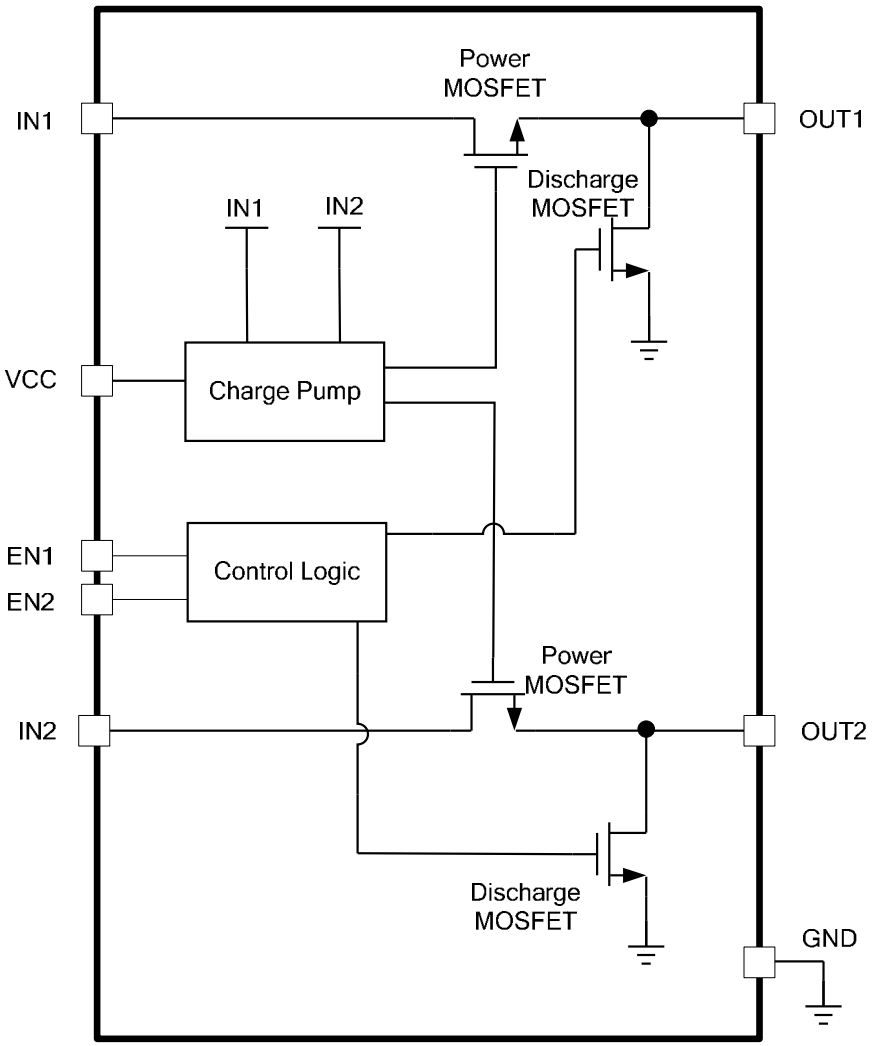



**Figure 1: Functional Block Diagram**

## OPERATION

The MP5090 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the slew rate of the voltage to the load. The MP5090 integrates dual load switches. Each channel can provide 3A of current (for the MP5090GQHT. The CSP package (MP5090GC) can provide 2A of load capability. The MP5090 can also easily parallel both channels connected together to achieve a maximum 6A load for the MP5090GQHT. The CSP package, MP5090GC, can achieve 4A if the parallel is used.

### Enable (EN1, EN2)

When the input voltage is greater than the under-voltage lockout threshold (UVLO) (typically 0.5V), and VCC is higher than 1.85V, the MP5090 can be enabled by pulling EN above 1.2V. Pull EN to ground to disable the MP5090. The recommended start-up sequence is to power up VCC and $V_{IN}$ first. After they are ready, pull the EN voltage high.

### Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current limit level (about 5A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns. Fast off keeps the power MOSFET off for about 80μs before turning it back on.

If the current limit block starts to regulate the output current, the power loss on the power MOSFET causes the IC temperature to rise. Hiccup protection limits the current for 2ms and turns it off for another 90ms for the thermal sink. If the junction temperature rises high enough during the hiccup on time, thermal shutdown is triggered. After thermal shutdown, the output is disabled until the over temperature fault is removed. The over-temperature threshold is 155°C, and the hysteresis is 30°C.

### Output Discharge

The MP5090 has an output discharge function. The output discharge resistor is active when EN or VCC is low. This function can discharge Vo by pulling down the resistance internally when the IC is disabled and the load is very light.

# APPLICATION INFORMATION

## Selecting the VCC Capacitor

VCC is an internal load switch supply voltage to the control circuitry. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 1µF capacitor is sufficient.

## Selecting the Input and Output Capacitor

The input capacitor is very important for protecting the part from input voltage spikes when a dead short or $V_{IN}$ hot-plug occurs. 0805 ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF 0805 input capacitor and a 1µF 0603 output capacitor are sufficient for each channel. For high output voltage applications, a 22µF input capacitor for each channel is recommended.

## Reverse Current Block Usage

The dual-channel load switch can be combined into a single-channel load switch with a reverse current block function (see Figure 2). IN1 is the input port, and IN2 is the output port. When EN1 = EN2 = high, the internal MOSFET is on. When EN1 = EN2 = low, the internal MOSFET is off, and the body diode blocks the reverse current.

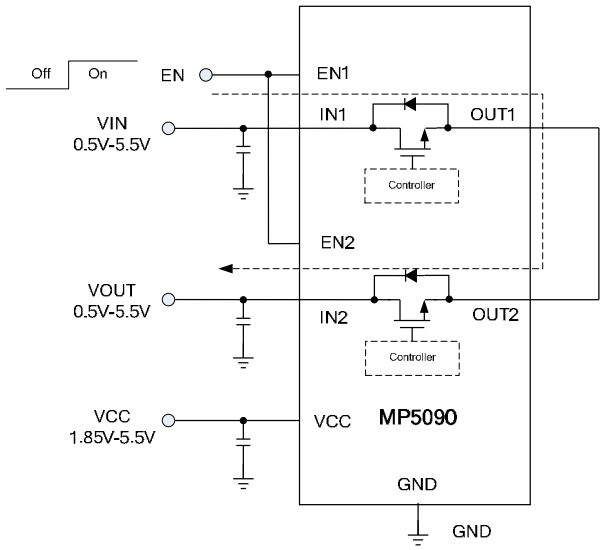



**Figure 2: Reverse Current Block Usage**

## Parallel Channel Usage

The MP5090 can be parallel-connected to achieve a 6A single-load switch for the MP5090GQHT. The CSP package, MP5090GC, can achieve 4A (see Figure 3). In this parallel connection, IN1 is connected to IN2 externally, and OUT1 is connected to OUT2 externally.

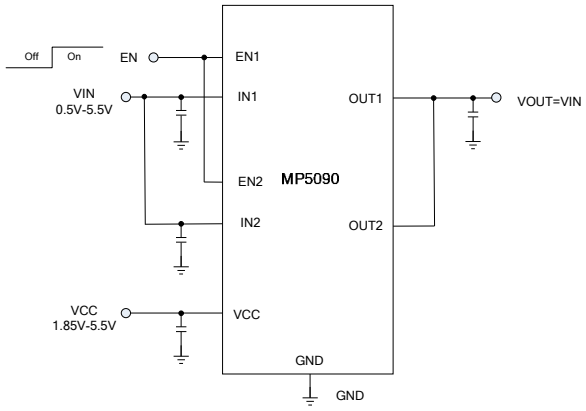
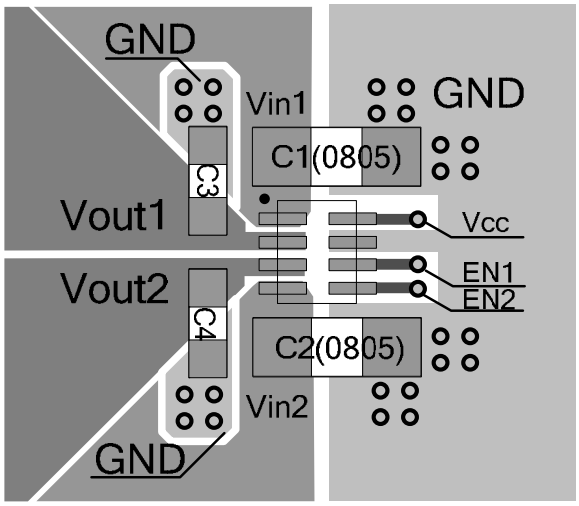



**Figure 3: Parallel Channel Usage**

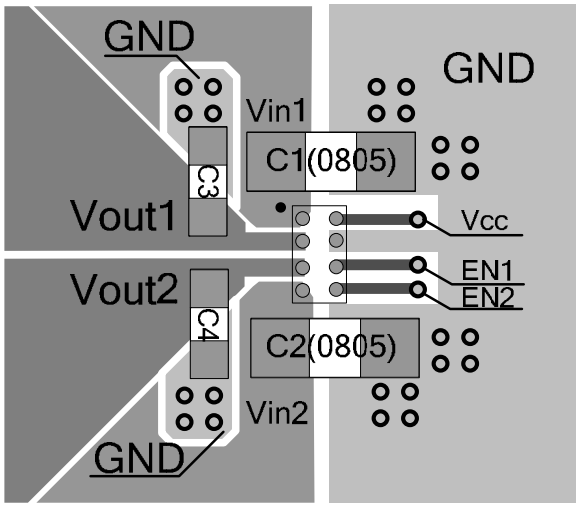
## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

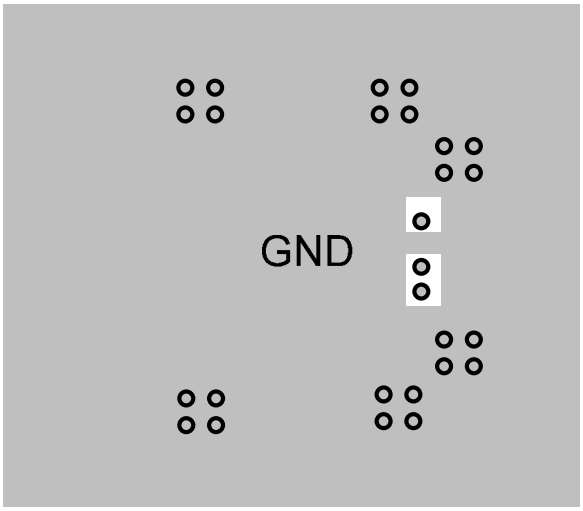
1. Place the caps close to the pins.
2. Place enough vias around the IC to achieve better thermal performance.




**Top Layer (TQFN)**




**Top Layer (CSP)**




**Bottom Layer**

**Figure 4: Recommended Layout**

## TYPICAL APPLICATION CIRCUIT

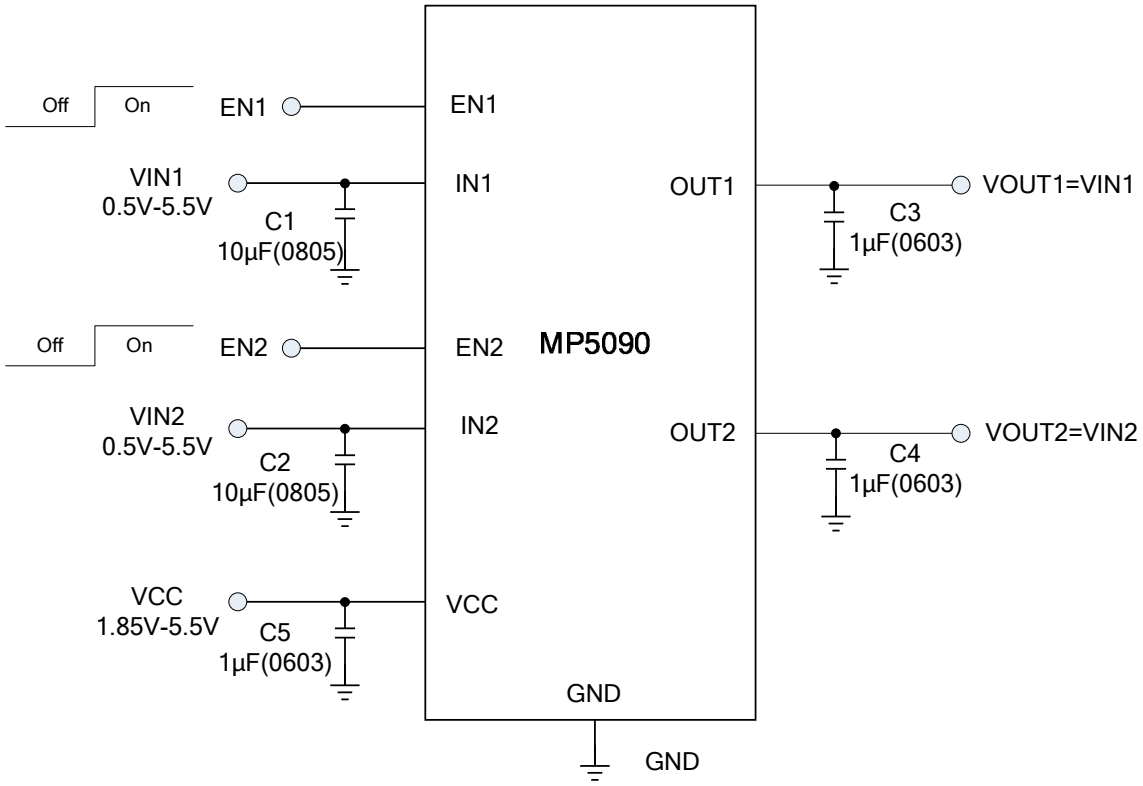
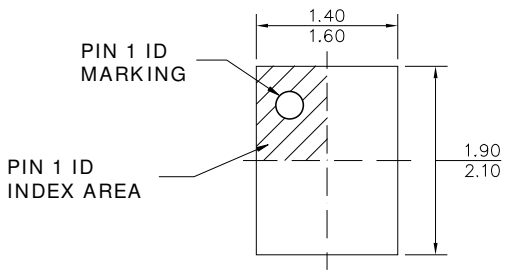


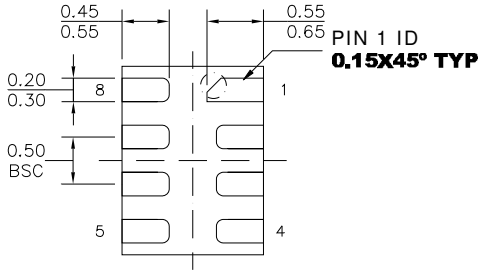

**Figure 5: Typical Application Schematic**

# PACKAGE INFORMATION

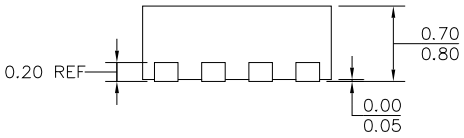
## TQFN (1.5mmx2.0mm)



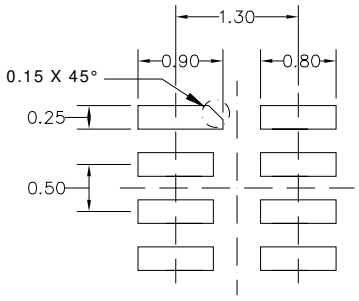

TOP VIEW




BOTTOM VIEW




SIDE VIEW



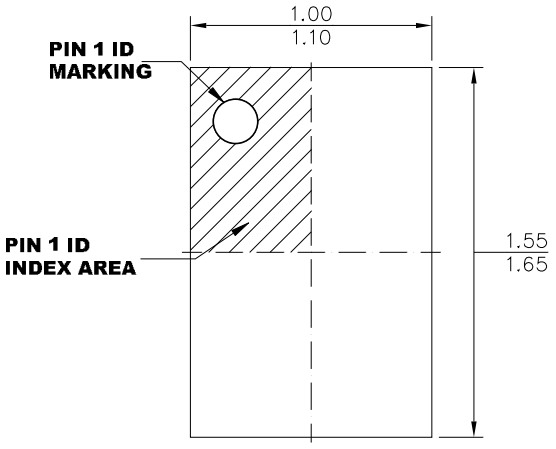

RECOMMENDED LAND PATTERN

NOTE:

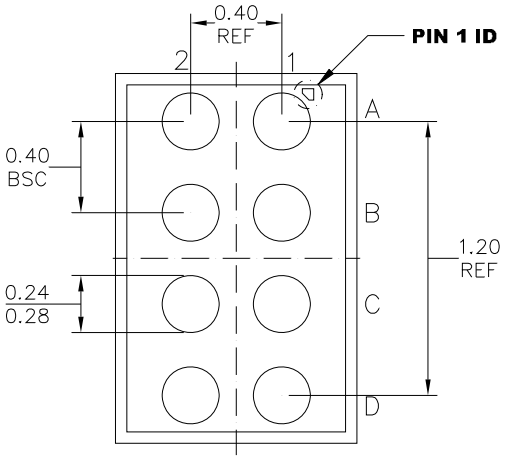
**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**3) JEDEC REFERENCE IS MO-220.**
**4) DRAWING IS NOT TO SCALE.**

## PACKAGE INFORMATION *(continued)*

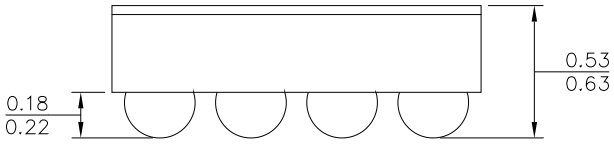
### CSP (1.05mmx1.60mm)



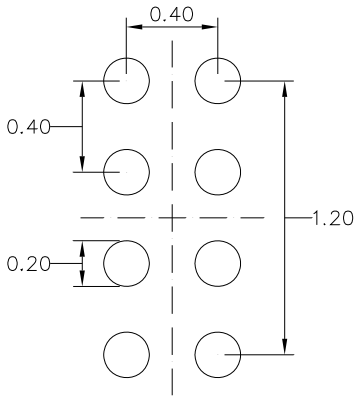

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.