Microsemi

MAX24205, MAX24210
5- or 10-Output Any-to-Any Timing ICs

General Description

The MAX24205 and MAX24210 are flexible, high-performance timing and clock synthesizer ICs that include a DPLL and two independent APLLs. When locked to one of two input clock signals, the device performs any-to-any frequency conversion. From any input clock frequency 1Hz to 750MHz the device can produce frequency-locked APLL output frequencies up to 750MHz and as many as 10 output clock signals that are integer divisors of the APLL frequencies. Input jitter can be attenuated by an internal low-bandwidth DPLL. The DPLL also provides truly hitless switching between input clocks and a high-resolution holdover capability. Input switching can be manual or automatic. Using only a low-cost crystal or oscillator, the device can also serve as a frequency synthesizer IC. Output jitter is typically 0.18 to 0.3ps RMS for an APLL-only integer multiply and 0.25 to 0.4ps RMS for APLL-only fractional multiply or DPLL+APLL operation.

For telecom systems, the device has all required features and functions to serve as a central timing function or as a line card timing IC. With a suitable oscillator the device meets the requirements of Stratum 2, 3E, 3, 4E, and 4; G.812 Types I to IV; G.813; and G.8262.

Applications

Frequency Conversion and Synthesis Applications in a Wide Variety of Equipment Types

Telecom Timing Cards or Line Cards for SONET/SDH, Synchronous Ethernet and/or OTN

Ordering Information

PART	OUTPUTS	TEMP RANGE	PIN-PACKAGE
MAX24205EXG+	5	-40 to +85	81-CSBGA
MAX24210EXG+	10	-40 to +85	81-CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

♦ **Input Clocks**

  ♦ One Crystal Input

  ♦ Two Differential or CMOS/TTL Inputs

  ♦ Differential to 750MHz, CMOS/TTL to 160MHz

  ♦ Continuous Input Clock Quality Monitoring

  ♦ Automatic or Manual Clock Selection

  ♦ Hitless Reference Switching on Loss of Input

♦ **Low-Bandwidth DPLL**

  ♦ Programmable Bandwidth, 0.5mHz to 400Hz

  ♦ Attenuates Input Jitter up to Several UI

  ♦ Free-Run or Holdover on Loss of All Inputs

  ♦ Hitless Reference Switching on Loss of Input

  ♦ Manual Phase Adjustment

♦ **Two APLLs Plus 5 or 10 Output Clocks**

  ♦ APLLs Perform High Resolution Fractional-N Clock Multiplication

  ♦ Any Output Frequency from <1Hz to 750MHz

  ♦ Each Output Has an Independent Divider

  ♦ Output Jitter Typically 0.18 to 0.3ps RMS for APLL-Only Integer Multiply and 0.25 to 0.4ps RMS for Other Modes (12kHz to 20MHz)

  ♦ Outputs are CML or 2xCMOS, Can Interface to LVDS, LVPECL, HSTL, SSTL and HCSL

  ♦ CMOS Output Voltage from 1.5V to 3.3V

♦ **General Features**

  ♦ Suitable Line Card IC or Timing Card IC for Stratum 2/3E/3/4E/4, SMC, SEC/EEC, or SSU

  ♦ Automatic Self-Configuration at Power-Up from External EEPROM Memory

  ♦ Uses External Crystal, Oscillator or Clock Signal As Master Clock

  ♦ Internal Compensation for Local Oscillator Frequency Error

  ♦ SPI Processor Interface

  ♦ 1.8V + 3.3V Operation (5V Tolerant)

  ♦ -40 to +85°C Operating Temp. Range

  ♦ 10mm x 10mm CSBGA Package

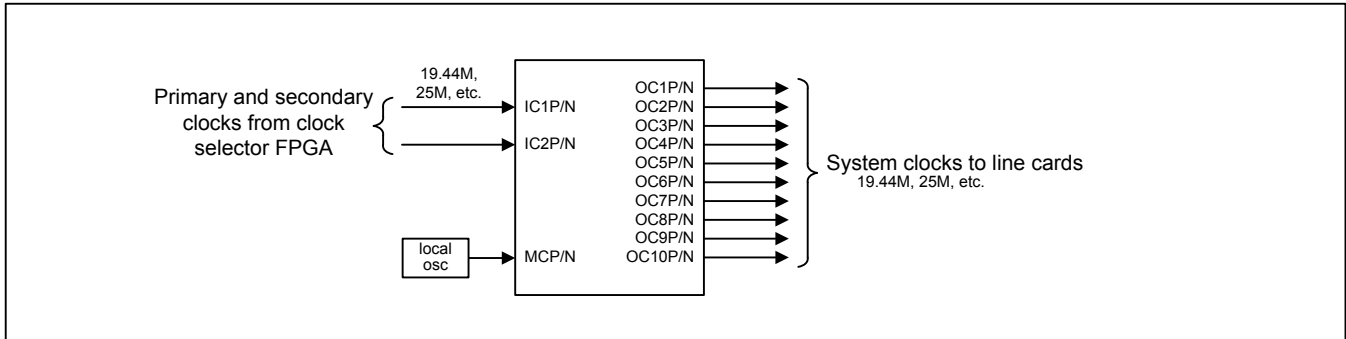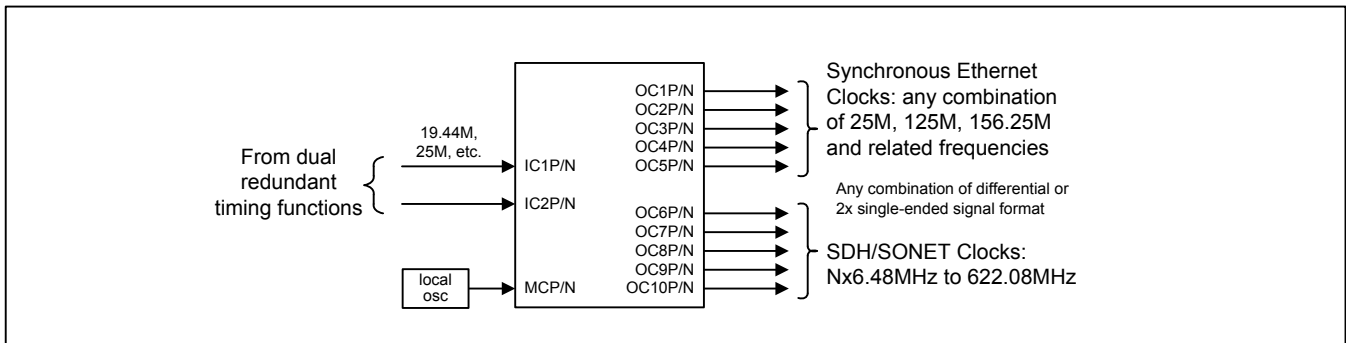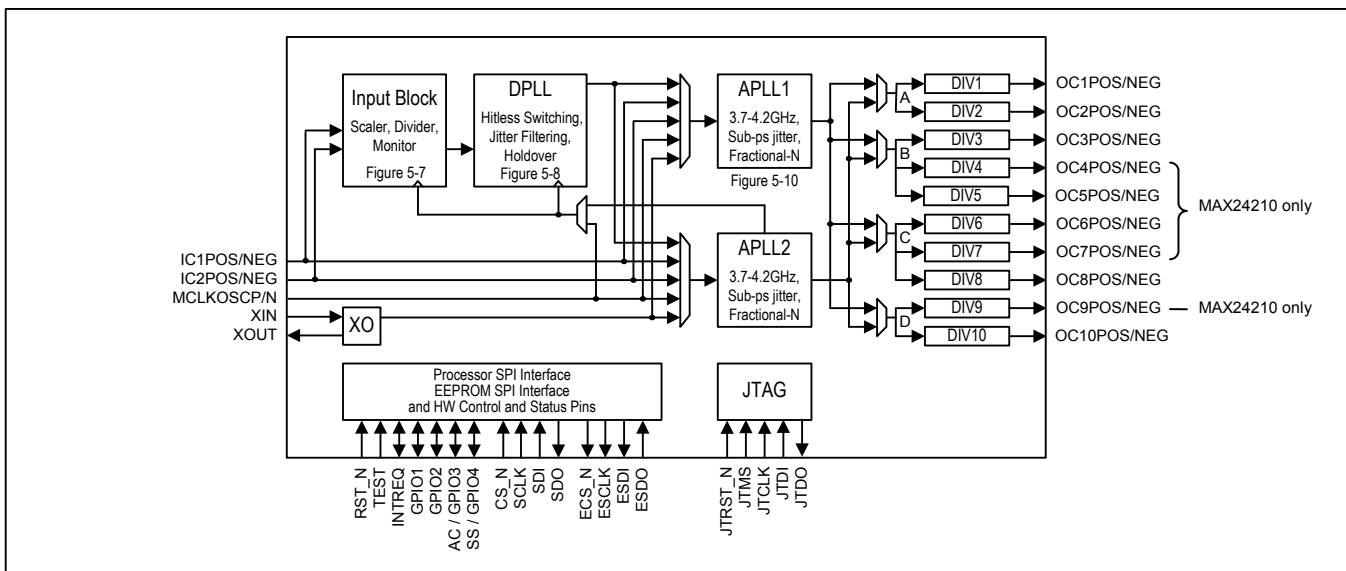# 1. Application Examples

Figure 1-1. Telecom Timing Card

Figure 1-2. Synchronous Ethernet and SDH/SONET Line Card

2. Block Diagram

Figure 2-1. Block Diagram

3. Detailed Features

3.1 Input Block Features

- Two input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 1Hz up to 750MHz
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Per-input fractional scaling (i.e. multiplying by N÷D where N is a 16-bit integer and D is a 32-bit integer and N<D) to undo 64B/66B and FEC scaling (e.g. 64/66, 238/255, 237/255, 236/255)
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement with 1.25ppm resolution
- Frequency monitor thresholds with 1.25ppm or 5ppb resolution

3.2 DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking ($\pm360°$ capture) or nearest-edge phase locking ($\pm180°$ capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching for true hitless switching
- Less than 1 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second, 5.8 minute and 93.2 minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency

3.3 APLL Features

- Two independent APLLs simultaneously product two frequency families from the same reference clock or different reference clocks
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Output jitter is typically 0.18 to 0.3ps RMS for APLL-only integer multiply and 0.25 to 0.4ps RMS for APLL-only fractional multiply or DPLL+APLL operation (12kHz to 20MHz integration band, for output frequencies >100MHz)
- Telecom output frequencies include 622.08MHz for SONET/SDH and 625MHz for Synchronous Ethernet
- Bypass mode for each APLL supports system testing and allows device to be used in fanout applications

3.4 Output Clock Features

- Ten low-jitter output clocks
- Each output can be one differential output or two CMOS/TTL outputs
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL components
- Each output can be any integer divisor of either APLL output clock
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can also produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Per-output delay adjustment, per-output enable/disable

3.5 General Features

- SPI serial microprocessor interface
- Optional automatic self-configuration at power-up from external EEPROM memory
- Four general-purpose I/O pins
- Can operate as DPLL+APLL for jitter filtering and hitless switching or as APLL only
- Local oscillator can be nearly any frequency from 10MHz to 750MHz
- Internal compensation for local oscillator frequency error
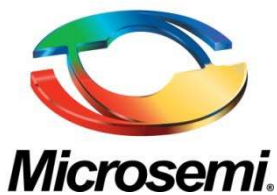
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