

FEATURES

- 133 dB SPL acoustic overload point**
- Small and thin 4 mm × 3 mm × 1 mm surface-mount package**
- Omnidirectional response**
- Very high signal-to-noise ratio (SNR): 65 dBA**
- Sensitivity of -46 dBFS**
- Extended frequency response from 45 Hz to >20 kHz**
- Low current consumption: 1.2 mA**
- Sleep mode for extended battery life: 5.5 μA consumption**
- High power supply rejection (PSR): -100 dBFS**
- Fourth-order Σ-Δ modulator**
- Digital pulse density modulation (PDM) output**
- Compatible with Sn/Pb and Pb-free solder processes**
- RoHS/WEEE compliant**

APPLICATIONS

- Smartphones and feature phones**
- Tablet computers**
- Teleconferencing systems**
- Digital still and video cameras**
- Bluetooth headsets**
- Notebook PCs**
- Security and surveillance**

GENERAL DESCRIPTION

The **ADMP621**¹ is a high sound pressure level (SPL), ultralow noise, low power, digital output, bottom ported omnidirectional MEMS microphone. This microphone clips at 133 dB SPL, which is useful for clearly capturing audio in loud environments. The **ADMP621** consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order Σ-Δ modulator. The digital interface allows the pulse density modulated (PDM) output of two microphones to be time multiplexed on a single data line using a single clock. The **ADMP621** is pin compatible with the **ADMP421** and **ADMP521** microphones, providing an easy upgrade path.

FUNCTIONAL BLOCK DIAGRAM

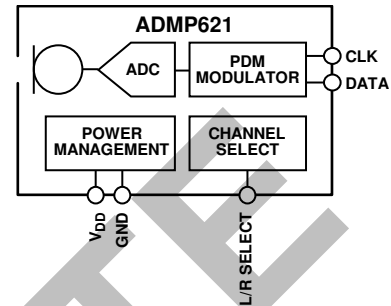
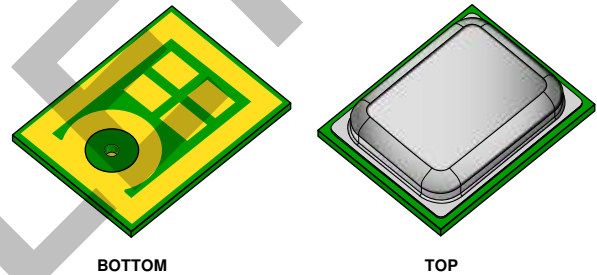


Figure 1.


 Figure 2. Isometric Views of **ADMP621** Microphone Package

The **ADMP621** has a high SNR of 65 dBA and sensitivity of -46 dBFS. The **ADMP621** has an extended wideband frequency response, resulting in natural sound with high intelligibility. Low current consumption and a sleep mode with less than 5.5 μA of current consumption enables long battery life for portable applications.

The **ADMP621** is available in a thin 4 mm × 3 mm × 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation.

¹ Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.

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REVISION HISTORY

7/13—Revision 0: Initial Revision

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$, $\text{CLK} = 3.072\text{ MHz}$, $C_{\text{LOAD}} = 30\text{ pF}$, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PERFORMANCE					
Directionality			Omni		
Output Polarity			Inverted		
Sensitivity ^{1, 2}	Input acoustic pressure vs. output data 1 kHz, 94 dB SPL	-48	-46	-44	dBFS
Signal-to-Noise Ratio (SNR)	20 Hz to 20 kHz, A-weighted		65		dB
Equivalent Input Noise (EIN)	20 Hz to 20 kHz, A-weighted		29		dB
Acoustic Dynamic Range	Derived from EIN and acoustic overload point		104		dB
Digital Dynamic Range	Derived from EIN and full-scale acoustic level		111		dB
Frequency Response ³	Low frequency -3 dB point		45		Hz
	High frequency -3 dB point		>20		kHz
Total Harmonic Distortion (THD)	105 dB SPL		0.35	1	%
Power Supply Rejection (PSR)	217 Hz, 100 mV p-p square wave superimposed on $V_{DD} = 1.8\text{ V}$, A-weighted		-100		dBFS
Power Supply Rejection—Swept Sine	1 kHz sine wave		-113		dB
Acoustic Overload Point	10% THD		133		dB SPL
Full-Scale Acoustic Level	0 dBFS output		140		dB SPL
POWER SUPPLY					
Supply Voltage (V_{DD})		1.62		3.63	V
Supply Current (I_S)					
Normal Mode	$V_{DD} = 1.8\text{ V}$		1.2	1.5	mA
	$V_{DD} = 3.3\text{ V}$		1.3	1.6	mA
Sleep Mode ⁴	$V_{DD} = 1.8\text{ V}$			5.5	μA
	$V_{DD} = 3.3\text{ V}$			8	μA
DIGITAL INPUT/OUTPUT CHARACTERISTICS					
Input Voltage High (V_{IH})		$0.65 \times V_{DD}$			V
Input Voltage Low (V_{IL})				$0.35 \times V_{DD}$	V
Output Voltage High (V_{OH})	$I_{\text{LOAD}} = 0.5\text{ mA}$	$0.7 \times V_{DD}$	V_{DD}		V
Output Voltage Low (V_{OL})	$I_{\text{LOAD}} = 0.5\text{ mA}$		0	$0.3 \times V_{DD}$	V
Output DC Offset	Percent of full scale		3		%
Latency			<30		μs
Noise Floor	20 Hz to 20 kHz, A-weighted		-111		dBFS

¹ Sensitivity is relative to the rms level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.

² The $\pm 2\text{ dB}$ sensitivity specification is valid for $\text{CLK} = 3.072\text{ MHz}$. At lower clock frequencies, the minimum and maximum specifications are -49 dBFS and -43 dBFS , respectively.

³ See Figure 6 and Figure 7.

⁴ The microphone enters sleep mode when the clock frequency is less than 1 kHz.

TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Typ	Max	Unit
SLEEP MODE					
Sleep Time	Time from CLK falling < 1 kHz		1		ms
Wake-Up Time	Time from CLK rising > 1 kHz to output within 3 dB of final sensitivity, power on		25		ms
INPUT					
t_{CLKIN}	Input clock period	270		1000	ns
Clock Frequency (CLK)		1.0	3.072 ¹	3.6	MHz
Clock Duty Ratio		40		60	%
OUTPUT					
t_{1OUTEN}	DATA1 (right) driven after falling clock edge	31			ns
$t_{1OUTDIS}$	DATA1 (right) disabled after rising clock edge	5		23	ns
t_{2OUTEN}	DATA2 (left) driven after rising clock edge	31			ns
$t_{2OUTDIS}$	DATA2 (left) disabled after falling clock edge	5		26	ns

¹ The microphone operates at any clock frequency between 1.0 MHz and 3.6 MHz. Some specifications may not be guaranteed at frequencies other than 3.072 MHz.

Timing Diagram

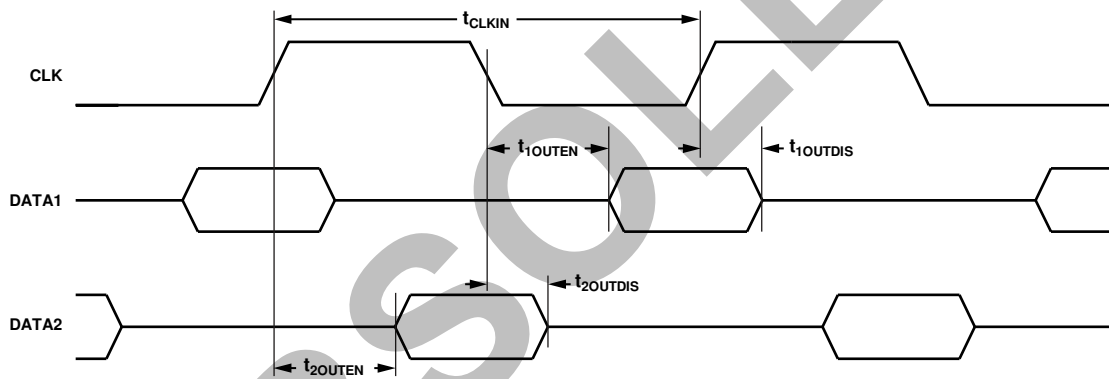


Figure 3. Pulse Density Modulated Output Timing

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	-0.3 V to +3.63 V
Digital Pin Input Voltage	-0.3 V to $V_{DD} + 0.3$ V or +3.63 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 g
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

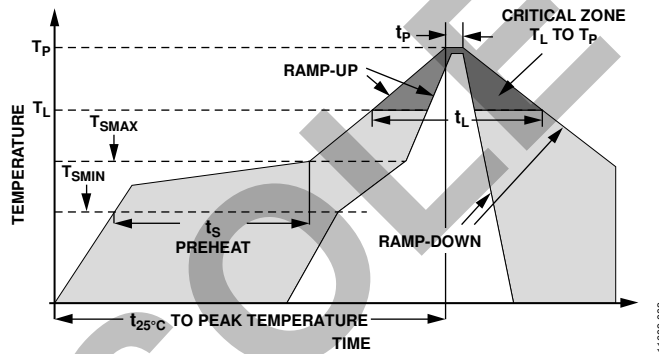


Figure 4. Recommended Soldering Profile Limits

Table 4. Recommended Soldering Profile Limits

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	1.25°C/sec maximum	1.25°C/sec maximum
Preheat		
Minimum Temperature (T_{SMIN})	100°C	100°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}), t_s	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)	1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)	45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)	183°C	217°C
Peak Temperature (T_P)	215°C +3°C/-3°C	260°C + 0°C/-5°C
Time Within 5°C of Actual Peak Temperature (t_P)	20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate	3°C/sec maximum	3°C/sec maximum
Time 25°C ($t_{25°C}$) to Peak Temperature	5 minute maximum	5 minute maximum

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

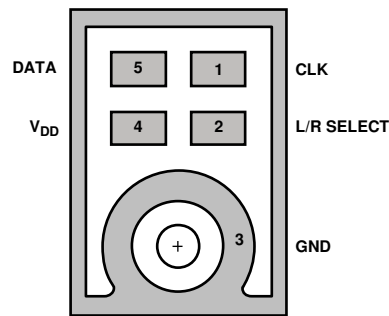


Figure 5. Pin Configuration (Bottom View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input to Microphone.
2	L/R SELECT	Left Channel or Right Channel Select. DATA1 (right): L/R SELECT tied to GND. DATA2 (left): L/R SELECT tied to V _{DD} .
3	GND	Ground.
4	V _{DD}	Power Supply. To avoid potential parasitic artifacts and for best performance, placing a 0.1 μ F (100 nF) ceramic type, X7R capacitor between Pin 4 (V _{DD}) and ground is strongly recommended. Place the capacitor as close to Pin 4 as possible.
5	DATA	Digital Output Signal (DATA1, DATA2).

TYPICAL PERFORMANCE CHARACTERISTICS

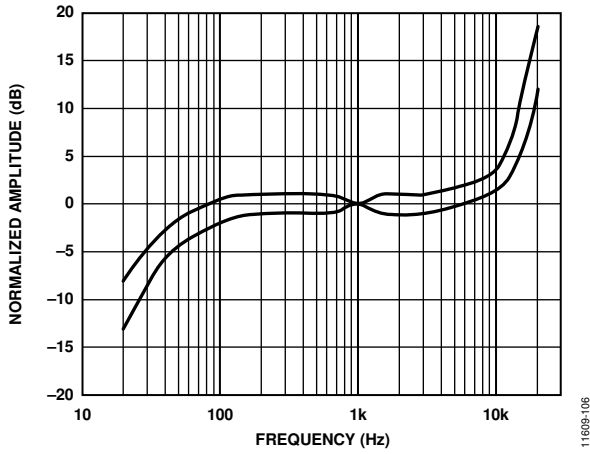


Figure 6. Frequency Response Mask

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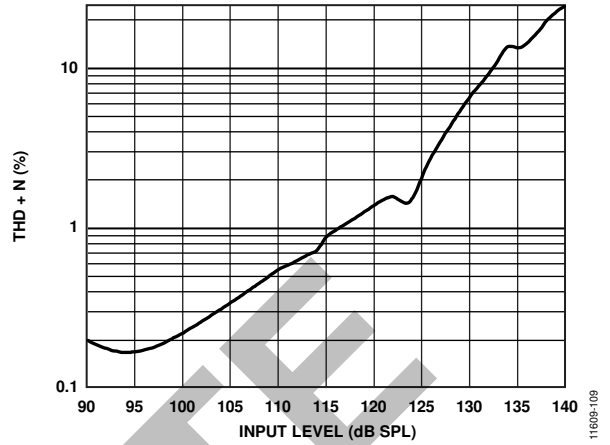


Figure 9. Total Harmonic Distortion + Noise (THD + N) vs. Input SPL

11609-109

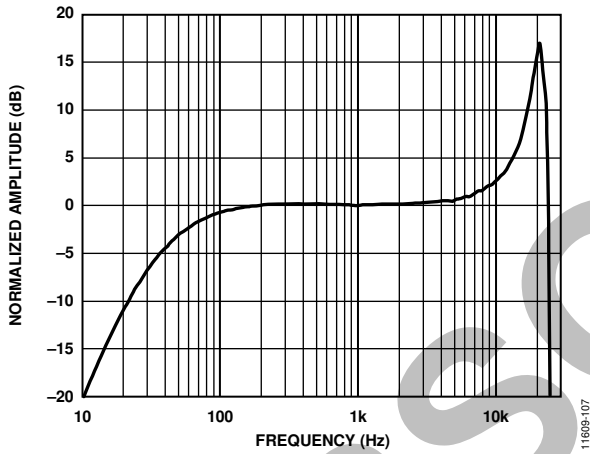


Figure 7. Typical Frequency Response (Measured)

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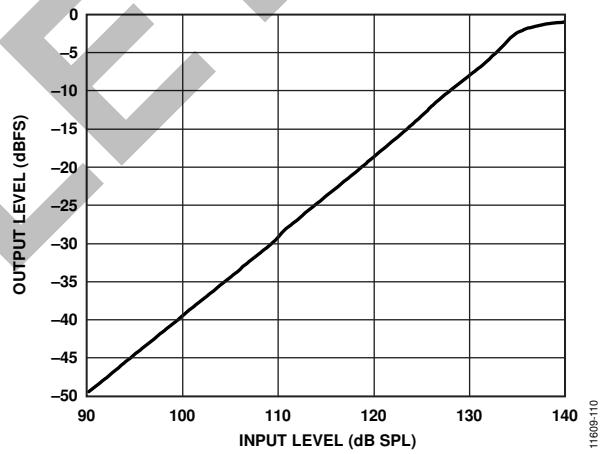


Figure 10. Linearity

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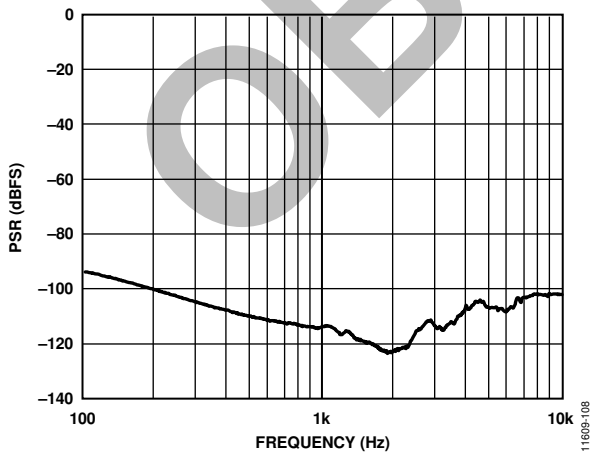


Figure 8. PSR vs. Frequency, 100 mV p-p Swept Sine Wave

11609-108

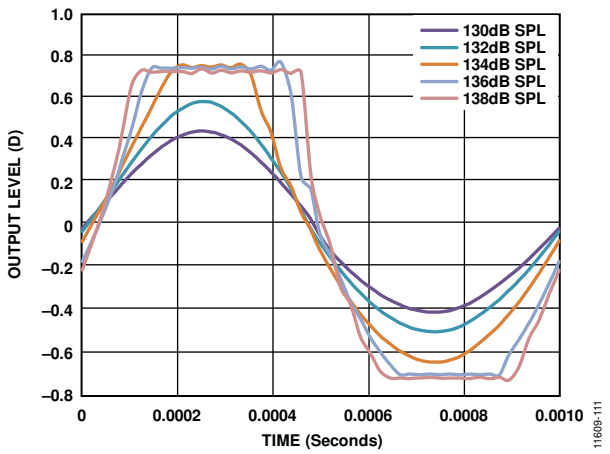


Figure 11. Clipping Characteristics

11609-111

THEORY OF OPERATION

PDM DATA FORMAT

The output from the DATA pin of the ADMP621 is in pulse density modulated (PDM) format. This data is the 1-bit output of a fourth-order Σ - Δ modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK, and the right channel is clocked on the rising edge of CLK. After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone tristates. In this way, two microphones, one set to the left channel and the other to the right, can drive a single DATA line. See Figure 3 for a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in this figure are two halves of the single physical DATA signal. Figure 12 shows a diagram of the two stereo channels sharing a common DATA line.

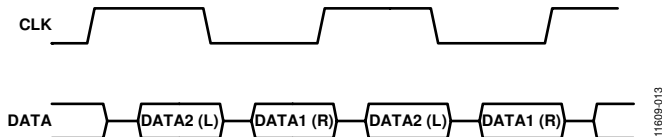


Figure 12. Stereo PDM Format

If only one microphone is connected to the DATA signal, the output is only clocked on a single edge (see Figure 13). For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition because the leakage of the DATA line is not enough to discharge the line while the driver is tristated.

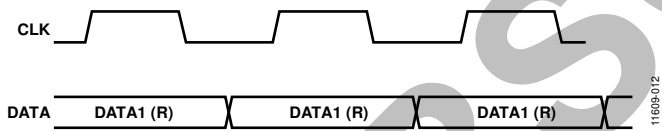


Figure 13. Mono PDM Format

See Table 6 for the channel assignments according to the logic level on the L/R SELECT pin.

Table 6. Channel Setting

L/R SELECT Setting	Channel
Low (Tie to Ground)	DATA1 (right)
High (Tie to V _{DD})	DATA2 (left)

For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale, and a high density of low pulses indicates a signal near negative full scale. A perfect zero (dc) audio signal shows an alternating pattern of high and low pulses.

The output PDM data signal has a small dc offset of about 3% of full scale. A high-pass filter in the codec that is connected to the digital microphone and does not affect the performance of the microphone typically removes this dc signal.

PDM MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified with the unit dBFS (decibels relative to digital full scale). A 0 dBFS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 14). This measurement convention also means that signals with a different crest factor may have an rms level higher than 0 dBFS. For example, a full-scale square wave has an rms level of 3 dBFS.

This definition of a 0 dBFS signal must be understood when measuring the sensitivity of the ADMP621. A 1 kHz sine wave at a 94 dB SPL acoustic input to the ADMP621 results in an output signal with a -46 dBFS level. The output digital word peaks at -46 dB below the digital full-scale level. A common misunderstanding is that the output has an rms level of -49 dBFS; however, this is not true because of the definition of the 0 dBFS sine wave.

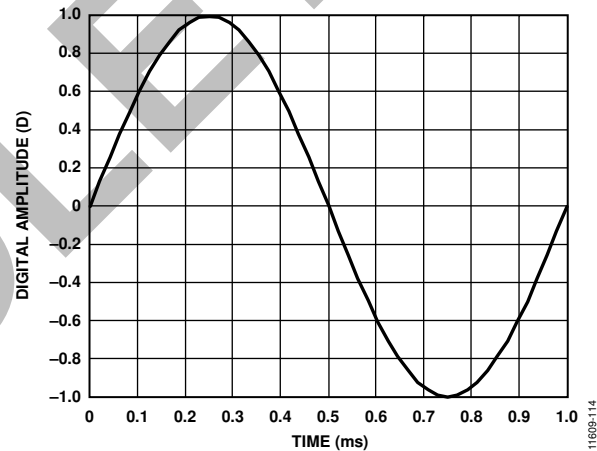


Figure 14. 1 kHz, 0 dBFS Sine Wave

There is not a commonly accepted unit of measurement to express the instantaneous level, as opposed to the rms level of the signal, of a digital signal output from the microphone. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale. In this case, a -46 dBFS sine wave has peaks at 0.005 D.

DYNAMIC RANGE CONSIDERATIONS

The full-scale digital output (0 dBFS) of the ADMP621 is mapped to an acoustic input of 140 dB SPL. The microphone clips (THD = 10%) at 133 dB SPL (see Figure 9); however, it continues to output an increasingly distorted signal above that point. The peak output level, which is controlled by the modulator, limits at about -3 dBFS (see Figure 10).

To fully use the 111 dB digital dynamic range of the output data of the ADMP621 in a design, the digital signal processor (DSP), analog-to-digital converter (ADC), or codec circuit following it must be chosen carefully. The decimation filter that inputs the PDM signal from the ADMP621 must have a dynamic range sufficiently better than the dynamic range of the microphone so that the overall noise performance of the system is not degraded. If the decimation filter has a dynamic range of 10 dB better than the microphone (121 dB), the overall system noise only degrades by 0.4 dB.

CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. This codec also generates the clock for the PDM microphones or is synchronous with the source that is generating the clock. See the Applications Information section for additional details on connecting the ADMP621 to Analog Devices, Inc., audio codecs with a PDM input. Figure 15 and Figure 16 show mono and stereo connections of the ADMP621 to a codec. The mono connection shows an ADMP621 set to output data on the right channel. To output on the left channel, tie the L/R SELECT pin to V_{DD} instead of tying it to GND.

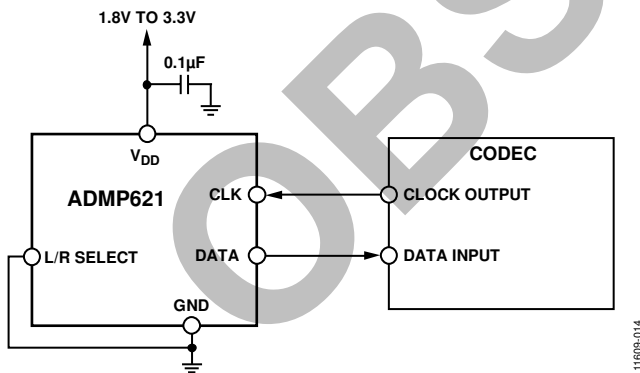


Figure 15. Mono PDM Microphone (Right Channel) Connection to Codec

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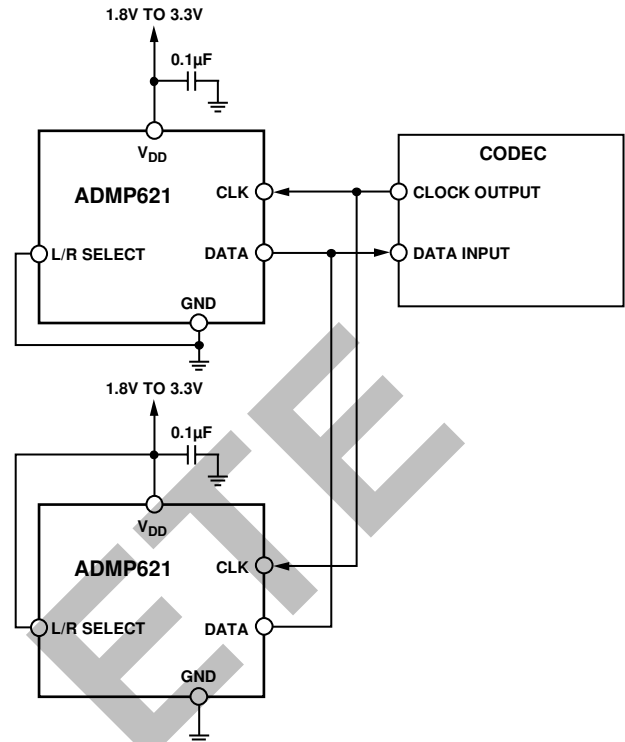


Figure 16. Stereo PDM Microphone Connection to Codec

11609-015

Decouple the V_{DD} pin of the ADMP621 to GND with a 0.1 µF capacitor. Place this capacitor as close to V_{DD} as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because it can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ADMP621 microphone(s) is placed close to the codec on the PCB. If the DATA signal must be driven over a long cable (>15 cm) or other large capacitive load, a digital buffer may be required. Only use a signal buffer on the DATA line when one microphone is in use or after the point where two microphones are connected (see Figure 17). The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select one with low propagation delay so that the timing of the data connected to the codec is not corrupted.

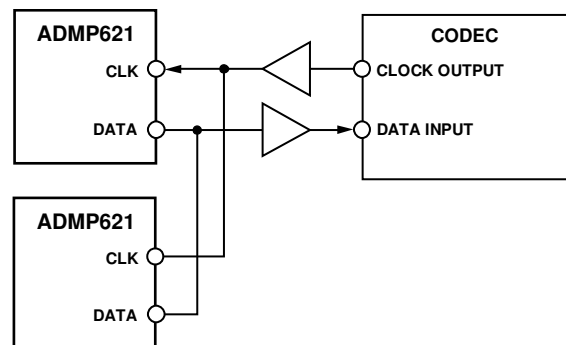


Figure 17. Buffered Connection Between Stereo ADMP621s and a Codec

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When long wires are used to connect the codec to the [ADMP621](#), a source termination resistor can be used on the clock output of the codec instead of a buffer to minimize signal overshoot or ringing. Match the value of this resistor to the characteristic impedance of the CLK trace on the PCB. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure 17.

SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 1 kHz. In this mode, the microphone data output is in a high impedance state. The current consumption in sleep mode is less than 5.5 μ A.

The [ADMP621](#) enters sleep mode within 1 ms of the clock frequency falling below 1 kHz. The microphone wakes up

from sleep mode and begins to output data 32,768 cycles after the clock becomes active. For a 3.072 MHz clock, the microphone starts to output data in 10.7 ms. For a 2.4 MHz clock, the microphone starts to output data in 13.7 ms. The wake-up time, as specified in Table 2, indicates the time from when the clock is enabled to when the [ADMP621](#) outputs data within 3 dB of its settled sensitivity.

START-UP TIME

The start-up time of the [ADMP621](#) from when the clock is active is the same as the wake-up time. The microphone starts up 32,768 cycles after the clock is active.

OBSOLETE

APPLICATIONS INFORMATION

INTERFACING WITH ANALOG DEVICES CODECS

The PDM output of the [ADMP621](#) interfaces directly with the digital microphone inputs on the Analog Devices [ADAU1361](#), [ADAU1761](#), [ADAU1781](#), and [ADAU1772](#) codecs. See the connection diagram shown in Figure 18, and refer to the [AN-1003 Application Note](#) and the respective data sheets of the codecs for more details on the digital microphone interface.

The [CN-0078 Circuit Note](#) describes the connection between these codecs and a digital microphone. All hardware configuration information is the same for the [ADMP621](#) as it is for the [ADMP421](#).

SUPPORTING DOCUMENTS

For additional information, see the following user guide, circuit note, and application notes.

Evaluation Board User Guides

[UG-326](#), *PDM Digital Output MEMS Microphone Evaluation Board*

Circuit Note

[CN-0078](#), *High Performance Digital MEMS Microphone Simple Interface to a SigmaDSP Audio Codec*

Application Notes

[AN-1003](#), *Recommendations for Mounting and Connecting Analog Devices, Inc., Bottom-Ported MEMS Microphones*

[AN-1068](#), *Reflow Soldering of the MEMS Microphone*

[AN-1112](#), *Microphone Specifications Explained*

[AN-1124](#), *Recommendations for Sealing Analog Devices, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress*

[AN-1140](#), *Microphone Array Beamforming*

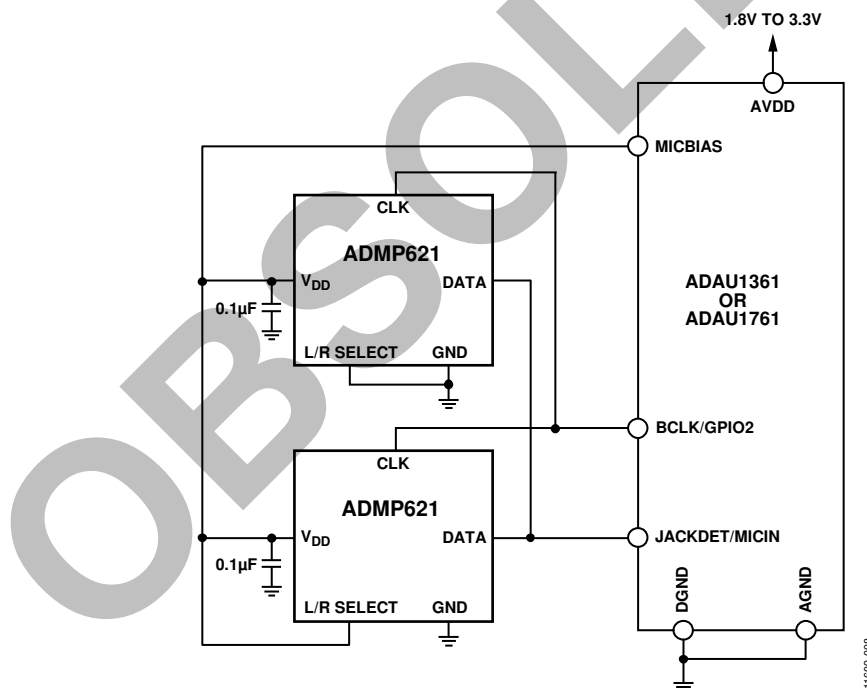


Figure 18. [ADAU1361](#) or [ADAU1761](#) Stereo Interface Block Diagram

PCB DESIGN AND LAYOUT

The recommended PCB land pattern for the ADMP621 must be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 19. Avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 20.

The response of the ADMP621 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the

microphone (0.25 mm, or 0.010 inch, in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.

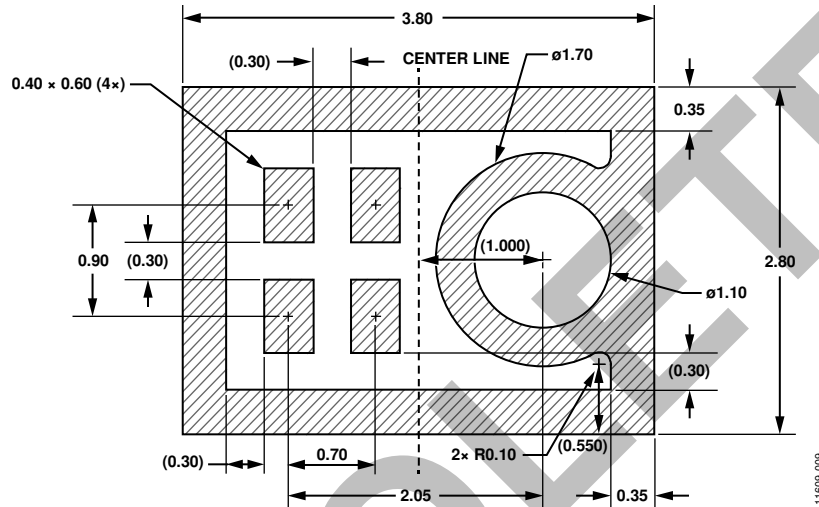


Figure 19. Recommended PCB Land Pattern Layout

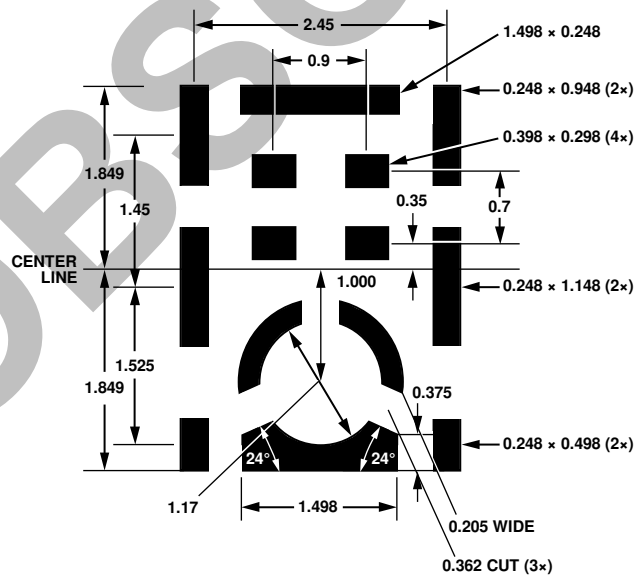


Figure 20. Suggested Solder Paste Stencil Pattern Layout

ALTERNATIVE PCB LAND PATTERNS

The standard PCB land pattern of the [ADMP621](#) has a solid ring around the edge of the footprint that can make routing the microphone signals more difficult in some board designs. This ring is used to improve the radio frequency (RF) immunity performance of the [ADMP621](#); however, it is not necessary to have this full ring connected for electrical functionality. If a design can tolerate reduced RF immunity, this ring can either be broken or removed completely from the PCB footprint. Figure 21 shows an example PCB land pattern with no enclosing ring around the edge of the part, and Figure 22 shows an example PCB land pattern with the ring broken on two sides so that the inner pads can be more easily routed on the PCB.

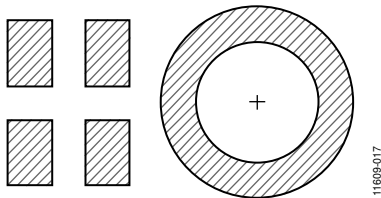


Figure 21. Example PCB Land Pattern with No Enclosing Ring

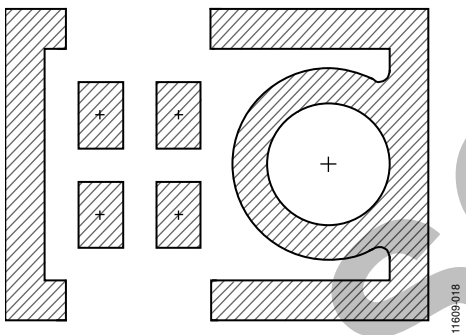


Figure 22. Example PCB Land Pattern with Broken Enclosing Ring

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground. If a pattern like one of these two examples is used on a PCB, take care that the unconnected ring on the bottom of the [ADMP621](#) is not placed directly over any exposed copper. This ring on the microphone is still at ground, and any PCB traces routed underneath it must be properly masked to avoid short circuits.

PCB MATERIAL AND THICKNESS

The performance of the [ADMP621](#) is not affected by PCB thickness and can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port, while providing the shortest acoustic path for good sound quality.

HANDLING INSTRUCTIONS

PICK-AND-PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 4 and Table 4.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow off procedures or ultrasonic cleaning.

OBSOLETE

OUTLINE DIMENSIONS

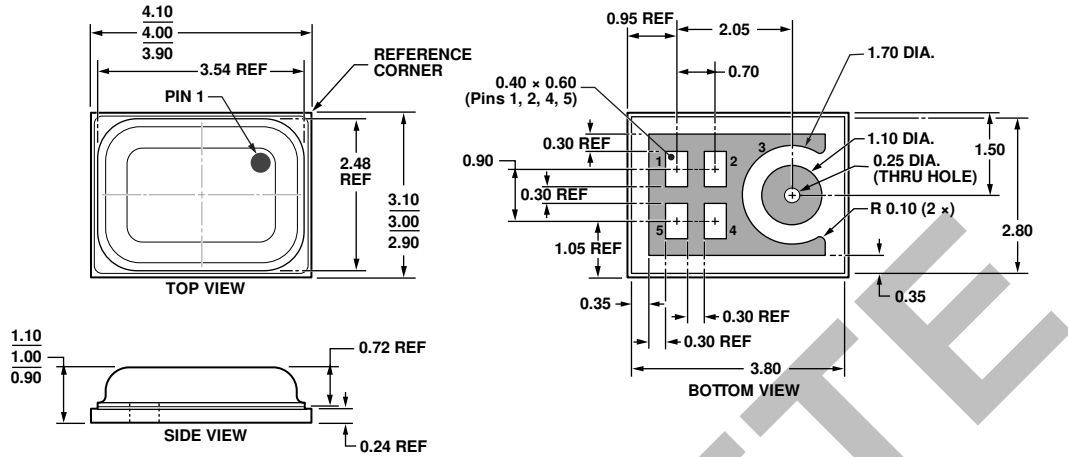


Figure 23. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
 4 mm x 3 mm Body
 (CE-5-1)
 Dimensions shown in millimeters

04-18-2012-G

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option ²	Ordering Quantity
ADMP621ACEZ-RL	-40°C to +85°C	5-Terminal LGA_CAV, 13" Tape and Reel	CE-5-1	5,000
ADMP621ACEZ-RL7	-40°C to +85°C	5-Terminal LGA_CAV, 7" Tape and Reel	CE-5-1	1,000
EVAL-ADMP621Z-FLEX		Flexible Evaluation Board		

¹ Z = RoHS Compliant Part.

² This package option is halide free.

NOTES

OBSOLETE