ISL3150E, ISL3152E, ISL3153E, ISL3155E, ISL3156E, ISL3158E

Large 3V Output Swing, 16.5kV ESD, Full Fail-Safe, 1/8 Unit Load, RS-485/RS-422 Transceivers

The ISL315xE (ISL3150E, ISL3152E, ISL3153E, ISL3155E, ISL3156E, and ISL3158E) family of 5V powered RS-485/RS-422 transceivers features high output drive and high ESD protection and high EFT immunity. The devices withstand ±16.5kV IEC61000-4-2 ESD strikes and are immune to ±4kV IEC6100-4-4 EFT transients without latch-up. The large output voltage of 3.1V typical into a 54Ω load provides high noise immunity, and enables the drive of up to 8000ft long bus segments, or eight 120Ω terminations in a star topology.

These devices possess less than 125µA bus input currents, thus constituting a true 1/8 unit load. The high output drive combined with the low bus input currents allows for connecting up to 512 transceivers on the same bus.

The receiver inputs feature a full fail-safe design that turns the receiver outputs high when the bus inputs are open or shorted.

The ISL315xE family includes half and full-duplex transceivers with active-high driver-enable pins and active-low receiver enable pins. These transceivers support data rates of 115kbps, 1Mbps, and 20Mbps. Their performance is characterized from -40°C to +85°C.

Features

- High V_{OD}: 3.1V (Typ) into R_D = 54Ω
- Low bus currents: 125µA constitutes a true 1/8 unit load
- Allows for up to 512 transceivers on the bus
- ±16.5kV ESD protection on bus I/O pins
- ±4kV EFT immunity on bus I/O pins
- High transient overvoltage tolerance of ±100V
- Full fail-safe outputs for open or shorted inputs
- Hot plug capability - driver and receiver outputs remain high-impedance during power-up and power-down
- Supported data rates: 115kbps, 1Mbps, 20Mbps
- Low supply current (driver disabled): 550µA
- Ultra-low shutdown current: 70nA

Applications

- Automated utility e-meter reading systems
- High node count systems
- PROFIBUS and Fieldbus systems in factory automation
- Security camera networks
- Lighting, elevator, and HVAC control systems in building automation
- Industrial process control networks
- Networks with star topology
- Long-haul networks in coal mines and oil rigs

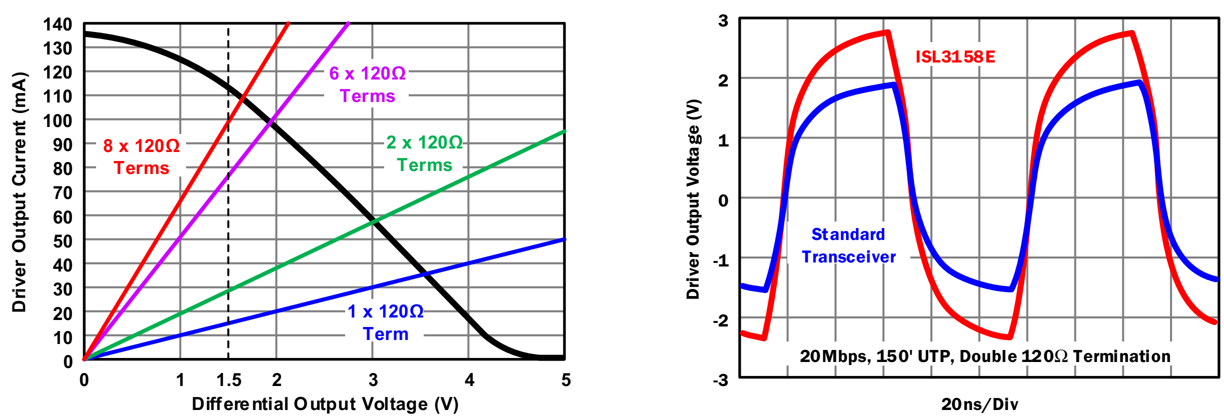


Figure 1. Typical Driver Output Performance of ISL315xE Transceivers

Contents

1. Overview

1.1 Typical Operating Circuits

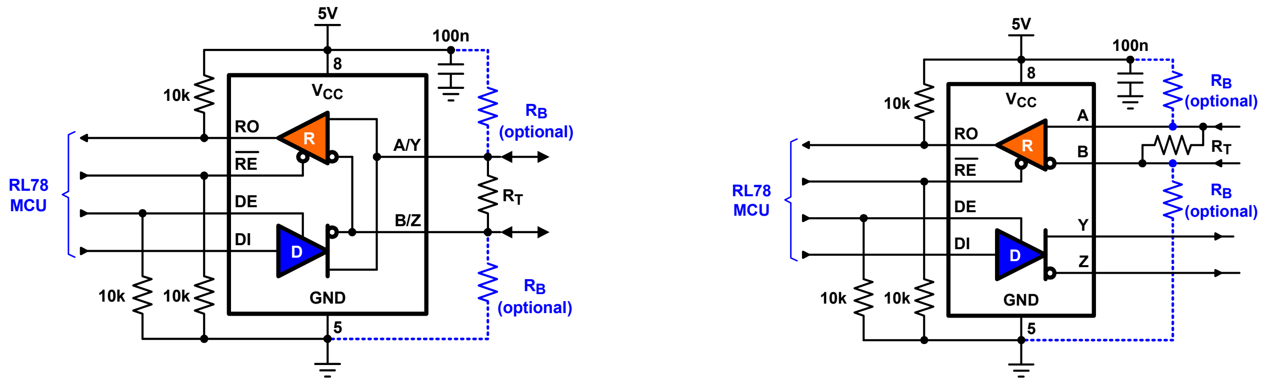


Figure 2. Typical Operating Circuits of Half-Duplex and Full-Duplex Transceivers

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range
ISL3150EIBZ	3150EIBZ	14 Ld SOIC	M14.15	Tube	-40 to +85°C
ISL3150EIBZ-T				Reel, 2.5k	
ISL3150EIBZ-T7A				Reel, 250	
ISL3150EIUZ	3150Z	10 Ld MSOP	M10.118	Tube	
ISL3150EIUZ-T				Reel, 2.5k	
ISL3150EIUZ-T7A				Reel, 250	
ISL3152EIBZ	3152EIBZ	8 Ld SOIC	M8.15	Tube	
ISL3152EIBZ-T				Reel, 2.5k	
ISL3152EIBZ-T7				Reel, 1k	
ISL3152EIBZ-T7A				Reel, 250	
ISL3152EIUZ	3152Z	8 Ld MSOP	M8.118	Tube	
ISL3152EIUZ-T				Reel, 2.5k	
ISL3152EIUZ-T7A				Reel, 250	
ISL3153EIBZ-T	3153EIBZ	14 Ld SOIC	M14.15	Reel, 2.5k	
ISL3153EIUZ	3153Z	10 Ld MSOP	M10.118	Tube	
ISL3153EIUZ-T				Reel, 2.5k	
ISL3153EIUZ-T7A				Reel, 250	
ISL3155EIBZ	3155EIBZ	8 Ld SOIC	M8.15	Tube	
ISL3155EIBZ-T				Reel, 2.5k	
ISL3155EIBZ-T7A				Reel, 250	
ISL3155EIUZ	3155Z	8 Ld MSOP	M8.118	Tube	
ISL3155EIUZ-T				Reel, 2.5k	

Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range
ISL3156EIBZ	3156EIBZ	14 Ld SOIC	M14.15	Tube	-40 to +85
ISL3156EIBZ-T				Reel, 2.5k	
ISL3156EIBZ-T7A				Reel, 250	
ISL3156EIUZ	3156Z	10 Ld MSOP	M10.118	Tube	
ISL3156EIUZ-T				Reel, 2.5k	
ISL3156EIUZ-T7A				Reel, 250	
ISL3158EIBZ	3158EIBZ	8 Ld SOIC	M8.15	Tube	
ISL3158EIBZ-T				Reel, 2.5k	
ISL3158EIBZ-T7A				Reel, 250	
ISL3158EIUZ	3158Z	8 Ld MSOP	M8.118	Tube	
ISL3158EIUZ-T				Reel, 2.5k	
ISL3158EIUZ-T7A				Reel, 250	

Notes:
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information pages for the ISL3150E, ISL3152E, ISL3153E, ISL3155E, ISL3156E, and ISL3158E. For more information about MSL, see TB363.

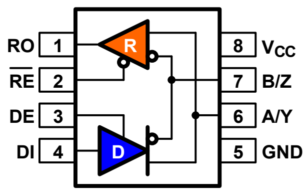
Table 1. Key Differences of Device Features

Part Number	Duplex	Data Rate (Mbps)	Rise/Fall Time (ns)	Tx/Rx Skew (ns)	Bus ESD (kV)	Pin Count
ISL3150E	Full	0.115	1100	12/4	±10	10, 14
ISL3152E	Half	0.115	1100	12/4	±16	8
ISL3153E	Full	1	150	3/4	±10	10, 14
ISL3155E	Half	1	150	3/4	±16	8
ISL3156E	Full	20	8	0.2/2.5	±10	10, 14
ISL3158E	Half	20	8	0.2/2.5	±16	8

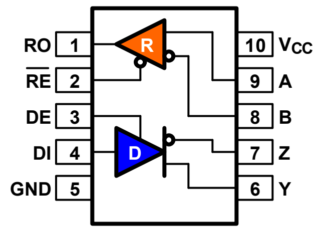
2. Pin Information

2.1 Pin Assignments

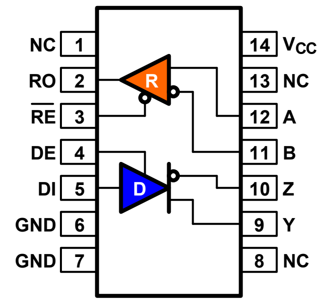
ISL3152E, ISL3155E, ISL3158E
(8 Ld MSOP, 8 Ld SOIC)
Top View



ISL3150E, ISL3153E, ISL3156E
(10 Ld MSOP)
Top View



ISL3150E, ISL3153E, ISL3156E
(14 Ld SOIC)
Top View



2.2 Pin Descriptions

8 Ld SOIC	10 Ld MSOP	14 Ld SOIC	Pin Name	Function
1	1	2	RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low. RO is Fail-safe High if A and B are unconnected (open) or shorted.
2	2	3	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	3	4	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
4	4	5	DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	5	6, 7	GND	Ground connection.
6	–	–	A/Y	Non-inverting receiver input and non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
7	–	–	B/Z	Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
–	6	9	Y	Non-inverting driver output.
–	7	10	Z	Inverting driver output.
–	8	11	B	Inverting receiver input.
–	9	12	A	Non-inverting receiver input.
8	10	–	V_{CC}	System power supply input (4.5V to 5.5V).
–	–	1, 8, 13	NC	No connection.

3. Specifications

3.1 Absolute Maximum Ratings

Parameter (Note 4)	Minimum	Maximum	Unit
V_{CC} to Ground		7	V
Input Voltages at DI, DE, $\overline{RE}$	-0.3	V_{CC} + 0.3	V
Bus I/O Voltages at A/Y, B/Z, A, B, Y, Z	-9	13	V
Transient Pulse Voltages through 100Ω at A/Y, B/Z, A, B, Y, Z (Note 5)		±100	V
RO	-0.3	V_{CC} + 0.3	V
Short Circuit Duration at Y, Z	Continuous		
ESD Rating	See "Electrical Specifications" on page 9.		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Notes:

4. Absolute Maximum ratings mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
5. Tested according to TIA/EIA-485-A, Section 4.2.6 (±100V for 15µs at a 1% duty cycle).

3.2 Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)
8 Ld SOIC	105
8 Ld MSOP	140
10 Ld MSOP	130
14 Ld SOIC	130

Note:

6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage	4.5	5.5	V
Temperature Range	-40	+85	°C
Bus Pin Common-Mode Voltage Range	-7	+12	V

3.4 Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C (Note 7). **Boldface limits apply across the operating temperature range, -40°C to +85°C**.

Parameter	Symbol	Test Conditions		Temp (°C)	Min (Note 15)	Typ	Max (Note 15)	Unit
DC Characteristics								
Driver Differential Output Voltage (No load)	V_{OD1}			Full	-	-	**V_{CC}**	V
Driver Differential Output Voltage (Loaded)	V_{OD2}	R_L = 100Ω (RS-422) (Figure 3)		Full	**2.8**	3.6	-	V
		R_L = 54Ω (RS-485) (Figure 3)		Full	**2.4**	3.1	**V_{CC}**	V
		R_L = 15Ω (Eight 120Ω terminations) (Note 16)		+25	-	1.65	-	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 4)		Full	**2.4**	3	-	V
Change in Magnitude of Driver Differential Output Voltage	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	0.01	**0.2**	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	-	**3.15**	V
Change in Magnitude of Driver Common-Mode Output Voltage	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	0.01	**0.2**	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	**2**	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	**0.8**	V
DI Input Hysteresis Voltage	V_{HYS}			+25	-	100	-	mV
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	**-2**	-	**2**	µA
Input Current (A, B, A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	70	**125**	µA
			V_{IN} = -7V	Full	**-75**	55	-	µA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{IN3}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	1	**40**	µA
			V_{IN} = -7V	Full	**-40**	-9	-	µA
Output Leakage Current (Y, Z) in Shutdown Mode (Full Duplex)	I_{IN4}	$\overline{RE}$ = V_{CC}, DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	1	**20**	µA
			V_{IN} = -7V	Full	**-20**	-9	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 9)		Full	-	-	**±250**	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	**-200**	-90	**-50**	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		+25	-	20	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -8mA, V_{ID} = -50mV		Full	**V_{CC} - 1.2**	4.3	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -8mA, V_{ID} = -200mV		Full	-	0.25	**0.4**	V
Receiver Output Low Current	I_{OL}	V_O = 1V, V_{ID} = -200mV		Full	**20**	28	-	mA
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	**-1**	0.03	**1**	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	**96**	160	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	**±7**	65	**±85**	mA

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C (Note 7). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 15)	Typ	Max (Note 15)	Unit
Supply Current							
No-Load Supply Current (Note 8)	I_{CC}	Half duplex versions, DE = V_{CC}, $\overline{RE}$ = X, DI = 0V or V_{CC}	Full	-	650	**800**	µA
		All versions, DE = 0V, $\overline{RE}$ = 0V, or full duplex versions, DE = V_{CC}, $\overline{RE}$ = X. DI = 0V or V_{CC}	Full	-	550	**700**	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}	Full	-	0.07	**3**	µA
ESD Performance							
RS-485 Pins (A, Y, B, Z, A/Y, B/Z)		IEC61000-4-2, Air-Gap Discharge Method: Half duplex	+25	-	±16.5	-	kV
		IEC61000-4-2, Air-Gap Discharge Method: Full duplex	+25	-	±10	-	kV
		IEC61000-4-2, Contact Discharge Method	+25	-	±9	-	kV
		Human Body Model, from bus pins to GND	+25	-	±16.5	-	kV
All Pins		Human Body Model, per MIL-STD-883 Method 3015	+25	-	±7	-	kV
		Machine Model	+25	-	400	-	V
Driver Switching Characteristics (115kbps Versions; ISL3150E, ISL3152E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	**500**	970	**1300**	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	-	12	**50**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	**700**	1100	**1600**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 7, Note 17)	Full	**115.2**	2000	-	kbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Note 10)	Full	-	300	**600**	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Note 10)	Full	-	130	**500**	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	50	**65**	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 6)	Full	-	35	60	ns
Time to Shutdown	t_{SHDN}	(Note 12)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Notes 12, 13)	Full	-	-	250	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Notes 12, 13)	Full	-	-	250	ns
Driver Switching Characteristics (1Mbps Versions; ISL3153E, ISL3155E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	**150**	270	**400**	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	-	3	**10**	ns

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C (Note 7). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 15)	Typ	Max (Note 15)	Unit
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	**150**	325	**450**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 7, Note 17)	Full	**1**	8	-	Mbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Note 10)	Full	-	110	**200**	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Note 10)	Full	-	60	**200**	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	50	**65**	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 6)	Full	-	35	**60**	ns
Time to Shutdown	t_{SHDN}	(Note 12)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Notes 12, 13)	Full	-	-	**250**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Notes 12, 13)	Full	-	-	**250**	ns
Driver Switching Characteristics (20Mbps Versions; ISL3156E, ISL3158E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	-	21	**30**	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	-	0.2	**3**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 5)	Full	-	12	**16**	ns
Maximum Data Rate	f_{MAX}	C_D = 470pF (Figure 7, Note 17)	Full	**20**	55	-	Mbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Note 10)	Full	-	30	**45**	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Note 10)	Full	-	28	**45**	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	50	**65**	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 6)	Full	-	38	**60**	ns
Time to Shutdown	t_{SHDN}	(Note 12)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 6, Notes 12, 13)	Full	-	-	**200**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 6, Notes 12, 13)	Full	-	-	**200**	ns
Receiver Switching Characteristics (115kbps and 1Mbps Versions; ISL3150E through ISL3155E)							
Maximum Data Rate	f_{MAX}	(Figure 8, Note 17)	Full	**1**	12	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 8)	Full	-	100	**150**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 8)	Full	-	4	**10**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9, Note 11)	Full	-	9	**20**	ns

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C (Note 7). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 15)	Typ	Max (Note 15)	Unit
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9, Note 11)	Full	-	7	**20**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9)	Full	-	8	**15**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9)	Full	-	8	**15**	ns
Time to Shutdown	t_{SHDN}	(Note 12)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9, Notes 12, 14)	Full	-	-	**200**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9, Notes 12, 14)	Full	-	-	**200**	ns
Receiver Switching Characteristics (20Mbps Versions; ISL3156E, ISL3158E)							
Maximum Data Rate	f_{MAX}	(Figure 8, Note 17)	Full	**20**	30	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 8)	Full	-	33	**45**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 8)	Full	-	2.5	**5**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9, Note 11)	Full	-	8	**15**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9, Note 11)	Full	-	7	**15**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9)	Full	-	8	**15**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9)	Full	-	8	**15**	ns
Time to Shutdown	t_{SHDN}	(Note 12)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 9), (Notes 12, 14)	Full	-	-	**200**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 9), (Notes 12, 14)	Full	-	-	**200**	ns

Notes:

7. All currents in to device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
8. Supply current specification is valid for loaded drivers when DE = 0V.
9. Applies to peak current. See "Performance Curves" beginning on page 15 for more information.
10. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
11. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
12. Transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See "Low Current Shutdown Mode" on page 21.
13. Keep $\overline{RE}$ = V_{CC}, and set the DE signal low time >600ns to ensure that the device enters SHDN.
14. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
15. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
16. See Figure 11 on page 15 for more information and for performance over temperature.
17. Limits established by characterization and are not production tested.

4. Test Circuits and Waveforms

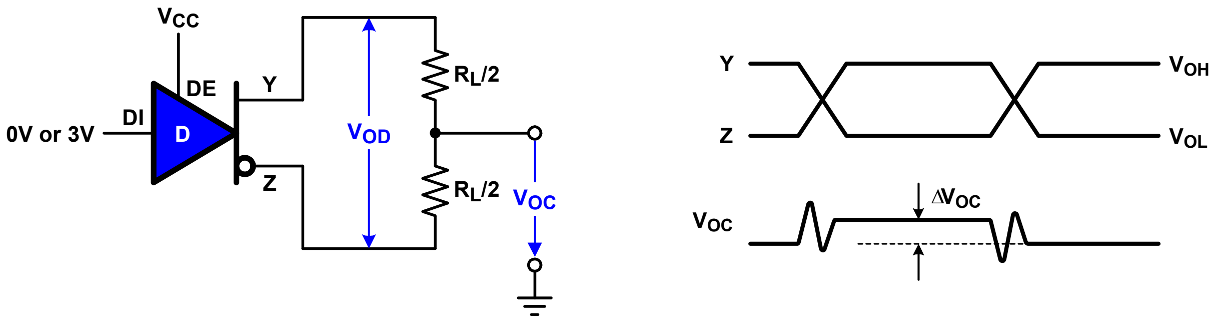


Figure 3. Measurement of Driver Differential Output Voltage with Differential Load

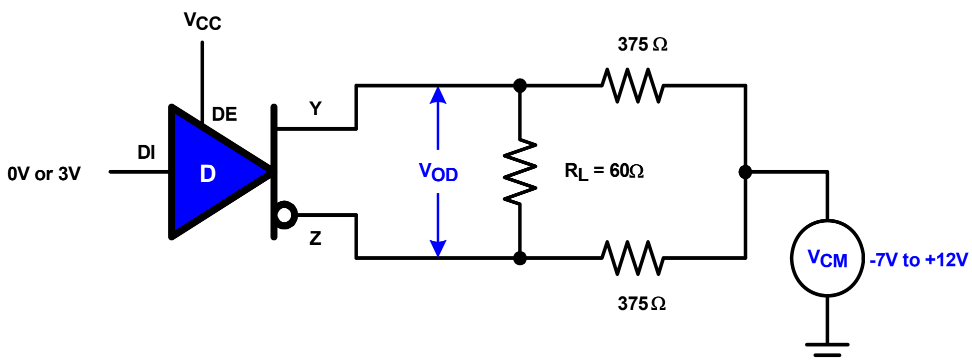


Figure 4. Measurement of Driver Differential Output Voltage with Common-Mode Load

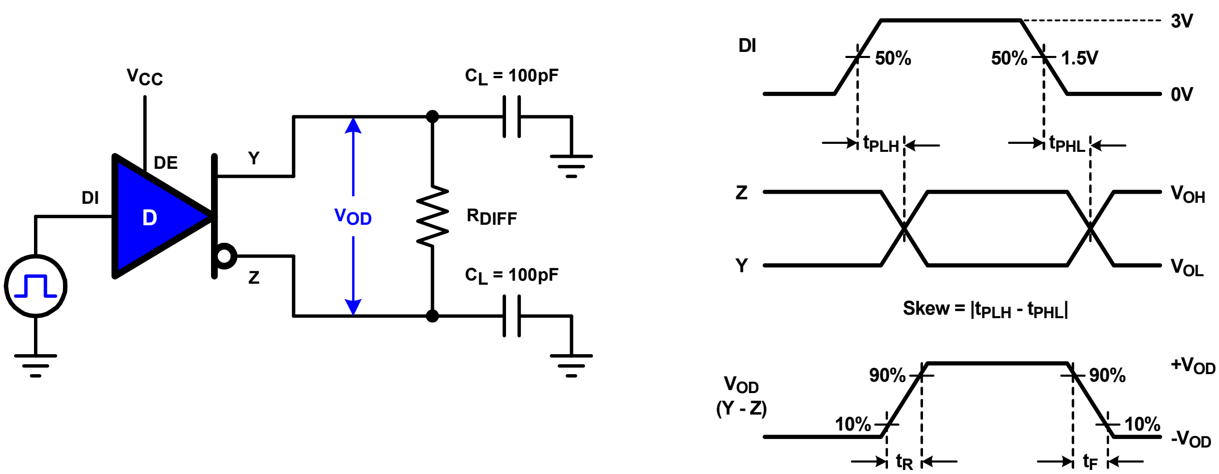
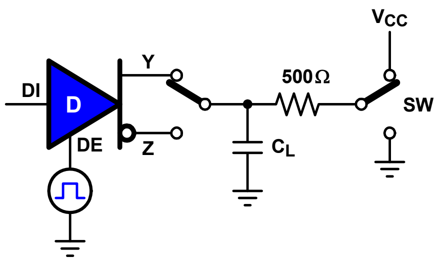


Figure 5. Measurement of Driver Propagation Delay and Differential Transition Times



Parameter	Output	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	0 (Note 10)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 10)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 13)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 13)	0/1	V_{CC}	100

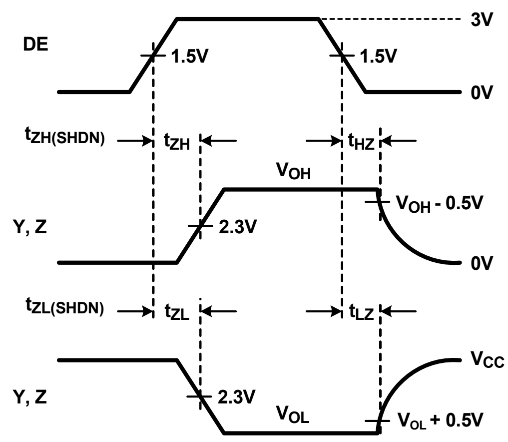


Figure 6. Measurement of Driver Enable and Disable Times

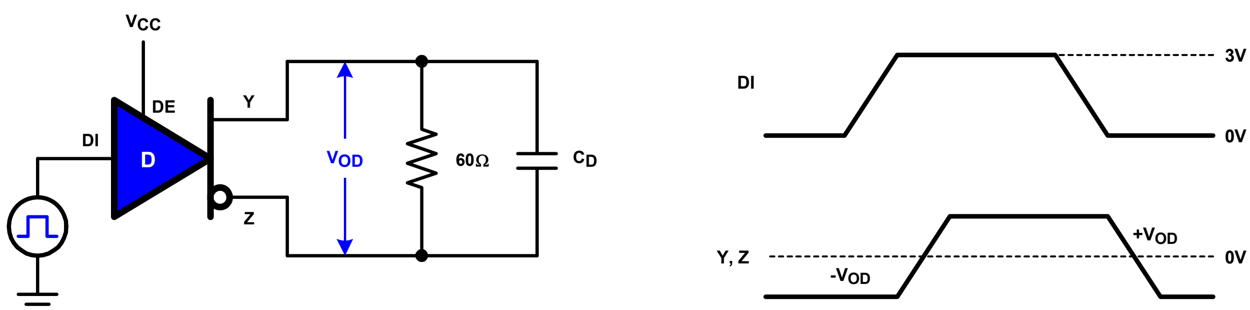


Figure 7. Measurement of Driver Data Rate

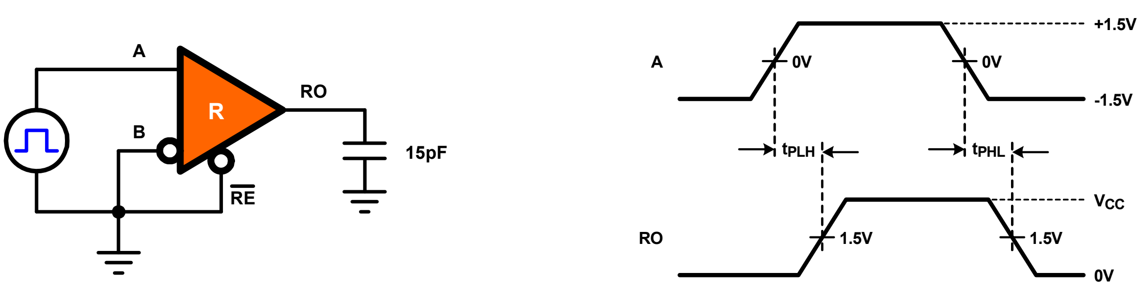
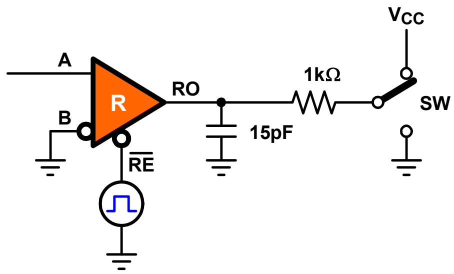


Figure 8. Measurement of Receiver Propagation Delay and Data Rate



Parameter	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 11)	0	+1.5V	GND
t_{ZL} (Note 11)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 14)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 14)	0	-1.5V	V_{CC}

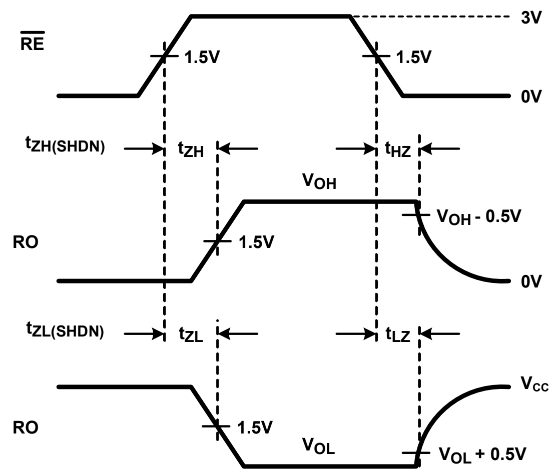


Figure 9. Measurement of Receiver Enable and Disable Times

5. Performance Curves

V_{CC} = 5V, T_A = +25°C; Unless otherwise specified

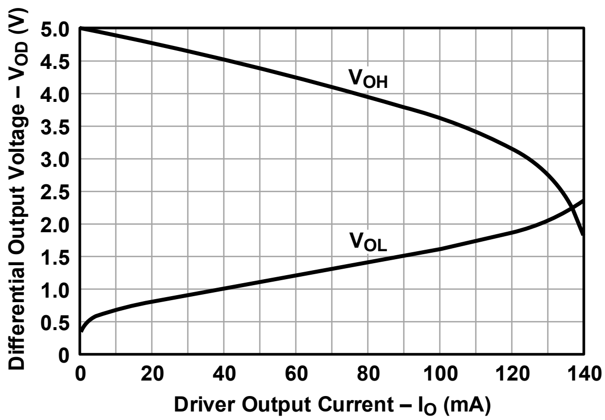


Figure 10. Driver Output High and Low Voltages vs Output Current

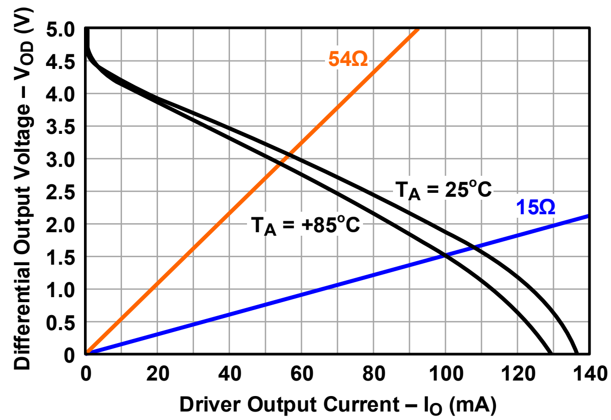


Figure 11. Driver Differential Output Voltage vs Output Current

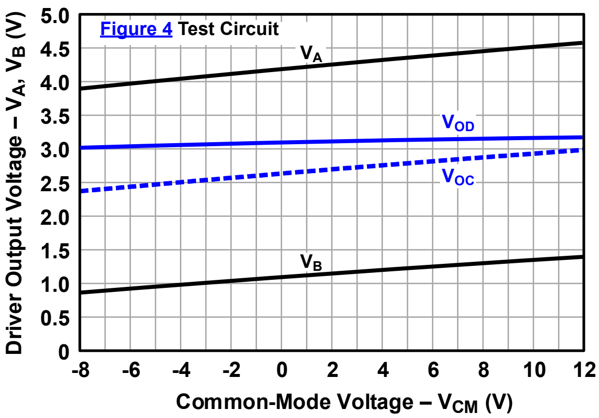


Figure 12. Driver Output Voltages vs Common-Mode Voltage

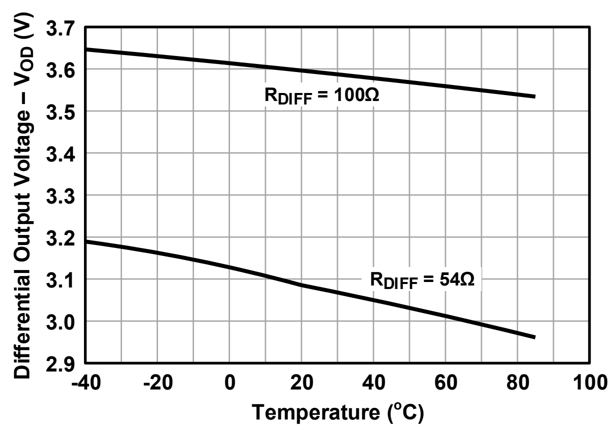


Figure 13. Driver Differential Output Voltage vs Temperature

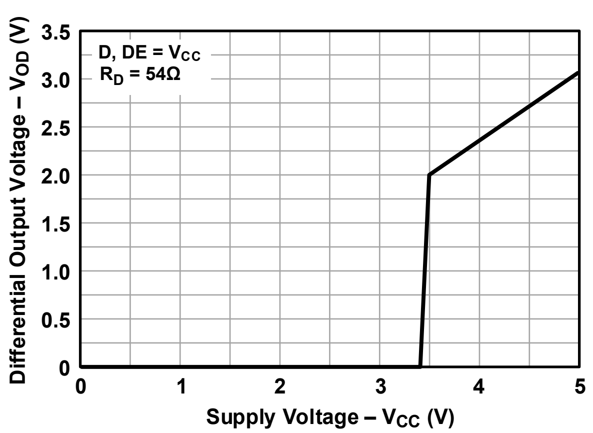


Figure 14. Driver Output Voltage vs Supply Voltage

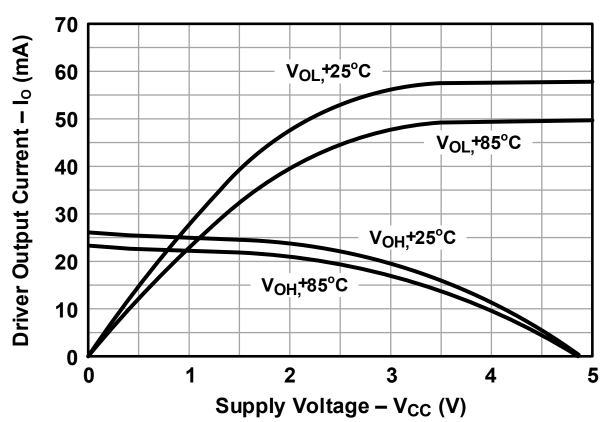


Figure 15. Receiver Output Voltage vs Output Current

V_{CC} = 5V, T_A = +25°C; Unless otherwise specified **(Continued)**

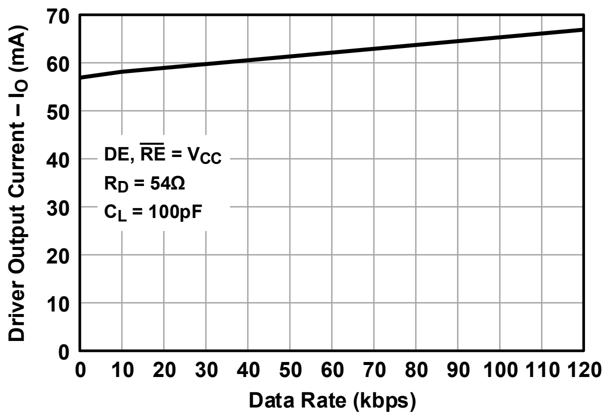


Figure 16. Supply Current vs Data Rate (ISL3150E, ISL3152E)

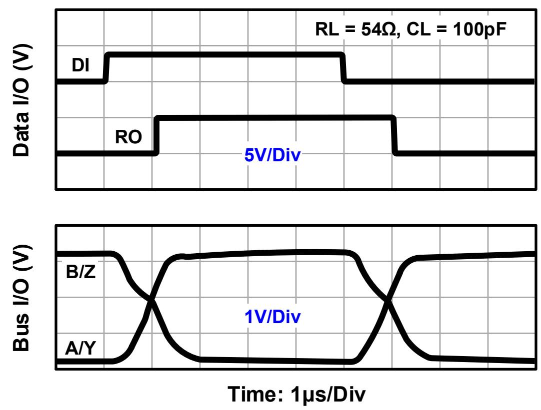


Figure 17. Waveforms (ISL3150E, ISL3152E)

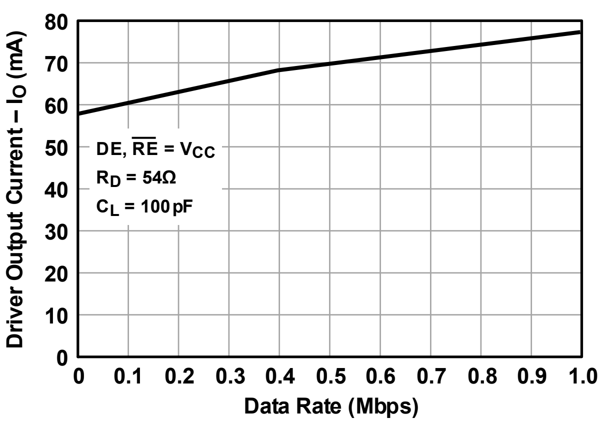


Figure 18. Supply Current vs Data Rate (ISL3153E, ISL3155E)

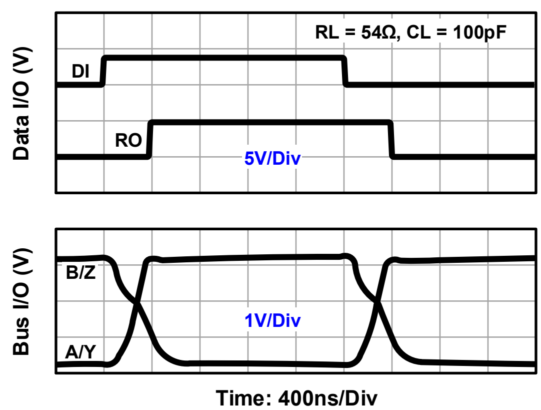


Figure 19. Waveforms (ISL3153E, ISL3155E)

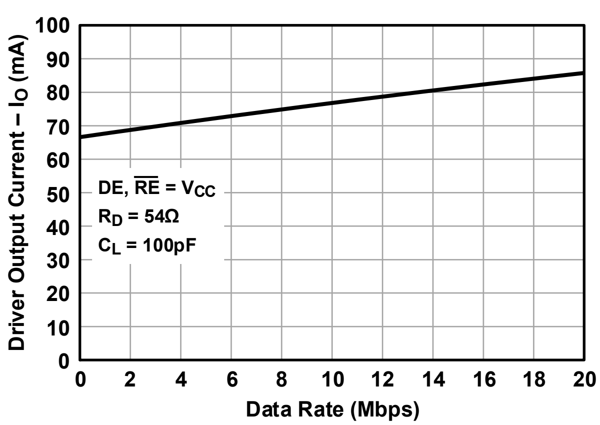


Figure 20. Supply Current vs Data Rate (ISL3156E, ISL3158E)

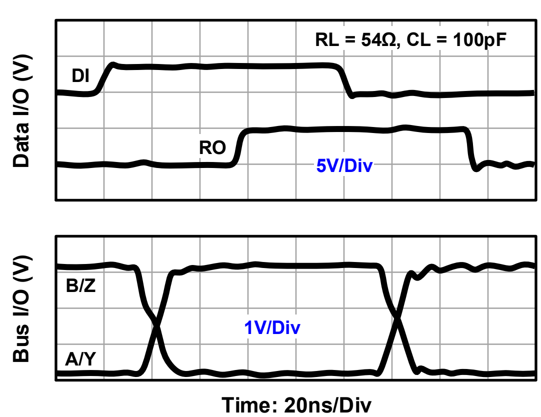


Figure 21. Waveforms (ISL3156E, ISL3158E)

V_{CC} = 5V, T_A = +25°C; Unless otherwise specified **(Continued)**

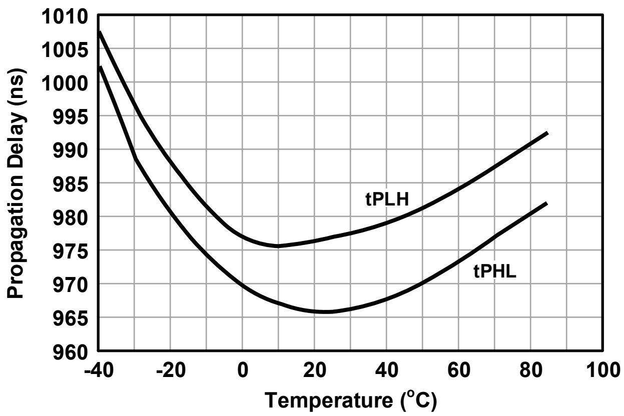


Figure 22. Differential Rise/Fall Times vs Temperature (ISL3150E, ISL3152E)

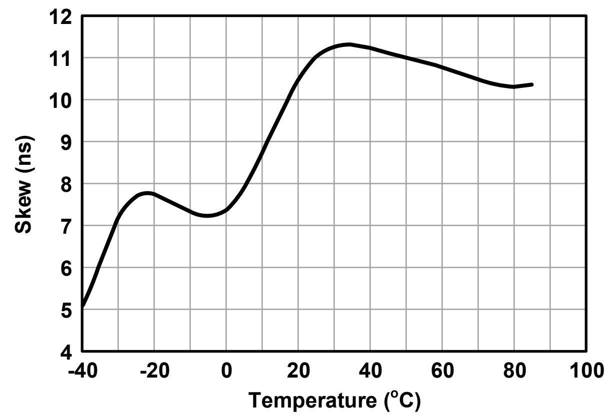


Figure 23. Differential Propagation Delay vs Temperature (ISL3150E, ISL3152E)

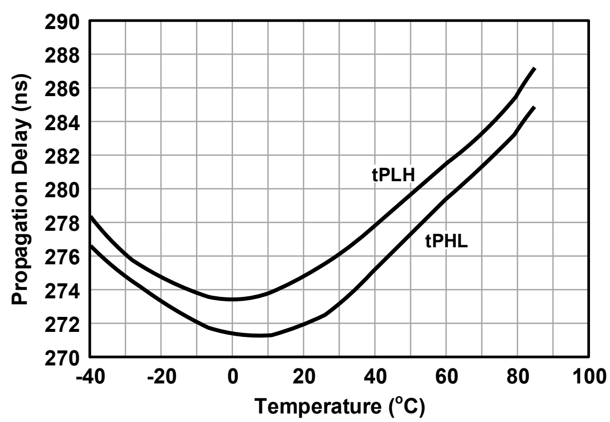


Figure 24. Differential Rise/Fall Times vs Temperature (ISL3153E, ISL3155E)

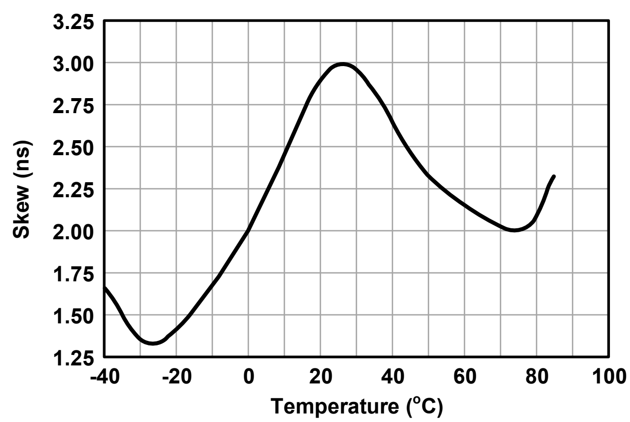


Figure 25. Differential Propagation Delay vs Temperature (ISL3153E, ISL3155E)

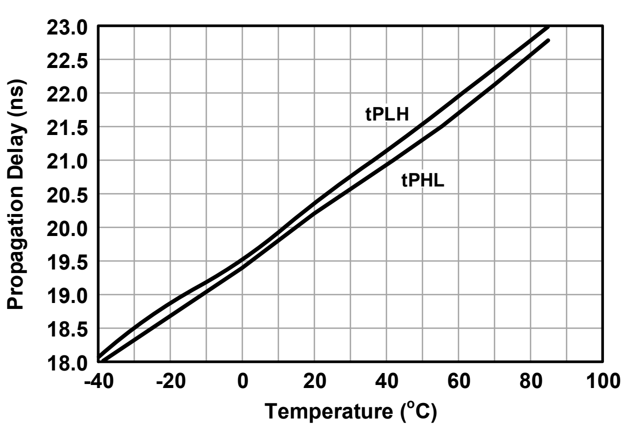


Figure 26. Differential Rise/Fall Times vs Temperature (ISL3156E, ISL3158E)

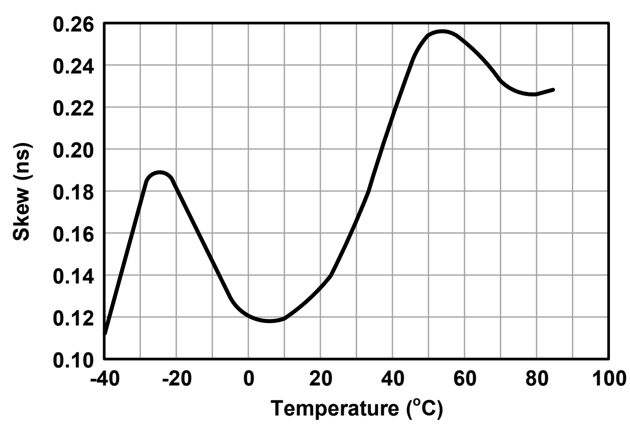


Figure 27. Differential Propagation Delay vs Temperature (ISL3156E, ISL3158E)

6. Device Description

6.1 Overview

The ISL3150E, ISL3153E, and ISL3156E are full-duplex RS-485 transceivers, and the ISL3152E, ISL3155E, and ISL3158E are half-duplex RS-485 transceivers. All transceivers feature a large output signal swing that is 60% higher than standard compliant transceivers. The devices are available in three speed grades suitable for data transmission up to 115kbps, 1Mbps, and 20Mbps.

Each transceiver has an active-high driver enable and an active-low receiver enable function. A shutdown current as low as 70nA can be accomplished by disabling both the driver and receiver for more than 600ns.

6.2 Functional Block Diagram

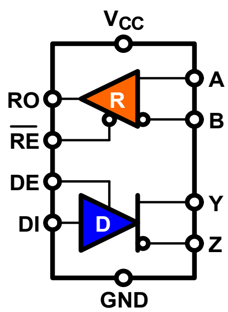


Figure 28. Block Diagram ISL3150E, ISL3153E, ISL3156E

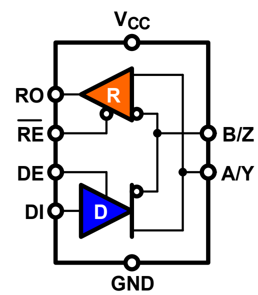


Figure 29. Block Diagram ISL3152E, ISL3155E, ISL3158E

6.3 Operating Modes

6.3.1 Driver Operation

A logic high at the driver enable pin, DE, activates the driver and causes the differential driver outputs, Y and Z, to follow the logic states at the data input, DI.

A logic high at DI causes Y to turn high and Z to turn low. In this case, the differential output voltage, defined as $V_{OD} = V_Y - V_Z$, is positive. A logic low at DI reverses the output states reverse, turning Y low and Z high, thus making V_{OD} negative.

A logic low at DE disables the driver, making Y and Z high-impedance. In this condition the logic state at DI is irrelevant. To ensure the driver remains disabled after device power-up, it is recommended to connect DE through a 1kΩ to 10kΩ pull-down resistor to ground.

Table 2. Driver Truth Table

Inputs			Outputs		Function
$\overline{RE}$	DE	DI	Y	Z	
X	H	H	H	L	Actively drives bus high
X	H	L	L	H	Actively drives bus low
L	L	X	Z	Z	Driver disabled, outputs high-impedance
H	L	X	Z*	Z*	Shutdown mode: driver and receiver disabled for more than 600ns

Note:* See Shutdown mode explanation in "Low Current Shutdown Mode" on page 21.

6.3.2 Receiver Operation

A logic low at the receiver enable pin, $\overline{RE}$, activates the receiver and causes its output, RO, to follow the bus voltage at the differential receiver inputs, A and B. Here, the bus voltage is defined as $V_{AB} = V_A - V_B$.

For $V_{AB} \geq -0.05V$, RO turns high, and for $V_{AB} \leq -0.2V$, RO turns low. For input voltages between -50mV and -200mV, the state of RO is undetermined, and thus could be high or low.

A logic high at $\overline{RE}$ disables the receiver, making RO high-impedance. In this condition the polarity and magnitude of the input voltage is irrelevant. To ensure the receiver output remains high when the receiver is disabled, it is recommended to connect RO, using a 1kΩ to 10kΩ pull-up resistor to V_{CC}.

To enable the receiver to immediately monitor the bus traffic after device power-up, connect $\overline{RE}$ through a 1kΩ to 10kΩ pull-down resistor to ground.

Table 3. Receiver Truth Table

Inputs			Outputs	Function
$\overline{RE}$	DE	A – B	RO	
L	X	$V_{AB} \geq -0.05V$	H	RO is data-driven high
L	X	$-0.05V > V_{AB} > -0.2V$	Undetermined	Actively drives bus low
L	X	$V_{AB} \leq -0.2V$	L	RO is data-driven low
L	X	Inputs Open/Shorted	H	RO is failsafe-high
H	H	X	Z	Receiver disabled, RO is high-impedance
H	L	X	Z*	Shutdown mode: driver and receiver disabled for more than 600ns

Note:* See Shutdown mode explanation in "Low Current Shutdown Mode" on page 21.

6.4 Device Features

6.4.1 Large Output Signal Swing

The ISL315xE family has a 60% larger differential output voltage swing than standard RS-485 transceivers. It delivers a minimum V_{OD} of 2.4V across a 54Ω differential load, or 1.65V across a 15Ω differential load. Figure 30 shows that the V_{OD} at 54Ω is more than 50% higher than that of a standard transceiver.

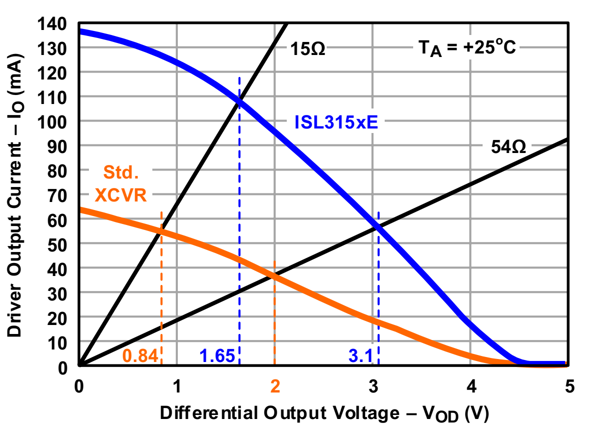
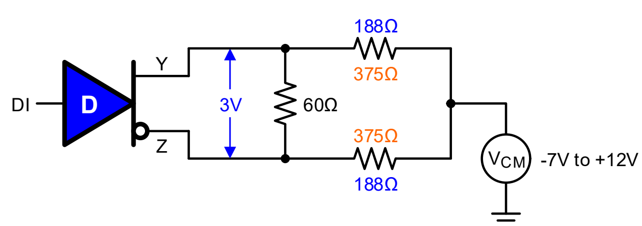


Figure 30. V-I Characteristic of ISL315xE vs Standard RS-485 Transceiver



Device	R_{CM} (Ω)	1UL (Ω)	# UL	1/8UL (Ω)	# Devices on Bus
Std. RS-485	375	12k	32	96k	256
ISL315xE	188	12k	64	96k	512

Figure 31. Unit Load and Transceiver Drive of ISL315xE vs Standard RS-485 Transceiver

Figure 31 compares the maximum number of unit loads and bus transceivers when choosing an ISL315xE over a standard transceiver. The RS-485 standard specifies a minimum total common-mode load resistance of R_{CM} = 375Ω between each signal conductor and ground. Because one unit load (1UL) is equivalent to 12kΩ, the total common-mode resistance of 375Ω yields 12kΩ/375Ω = 32 ULs.

For an ISL315xE transceiver however, R_{CM} can be as small as 188Ω, resulting in a total common-mode load of 12kΩ/188Ω = 64 ULs. This means the driver of an ISL315xE transceiver can drive up to 64 x 1UL transceivers or 512 x 1/8UL transceivers.

The advantages of such superior drive capability are:

- Up to 900mV higher noise immunity (2.4V vs 1.5V V_{OD})
- Up to twice the maximum cable length of standard transceivers (~8000ft vs 4000ft)
- The design of star configurations or other multi-terminated nonstandard network topologies

6.4.2 Driver Overload Protection

The RS-485 specification requires drivers to survive worst case bus contentions undamaged. The ISL315xE transceivers meet this requirement through driver output short circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiters that ensure that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes.

In the event of a major short-circuit conditions, the devices also include a thermal shutdown feature that disables the drivers whenever the temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. The receivers stay operational during thermal shutdown.

6.4.3 Full-Failsafe Receiver

The differential receivers of the ISL315xE family are full-failsafe, meaning their outputs turn logic high when:

- The receiver inputs are open (floating) due to a faulty bus node connector
- The receiver inputs are shorted due to an insulation break of the bus cable
- The receiver input voltage is close to 0V due to a terminated bus not being actively driven

Full-failsafe switching is accomplished by offsetting the maximum receiver input threshold to -50mV. Figure 32 shows that, in addition to the threshold offset, the receiver also has an input hysteresis, ΔV_{TH}, of 20mV. The combination of offset and hysteresis allows the receiver to maintain its output high, even in the presence of 140mV_{P-P} differential noise, without the need for external failsafe biasing resistors.

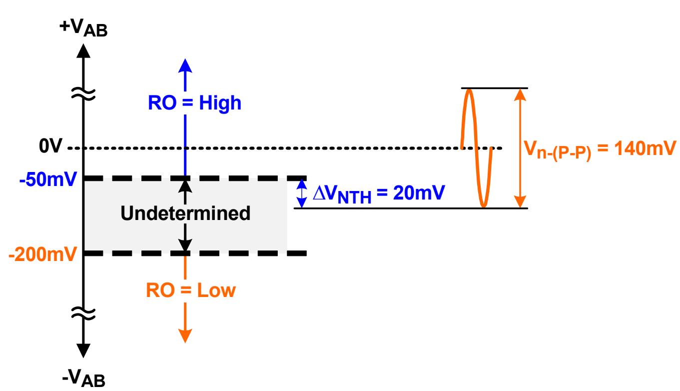


Figure 32. Full-Failsafe Performance with High Noise Immunity

6.4.4 Low Current Shutdown Mode

The ISL315xE transceivers use a fraction of the power required by their bipolar counterparts, but also include a shutdown feature that reduces the already low quiescent I_{CC} to a 70nA trickle. These devices enter shutdown whenever the receiver and the driver are simultaneously disabled ($\overline{RE} = V_{CC}$ and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that driver and receiver enable times increase when the transceiver enables from shutdown. Refer to Notes 9 to 13 at the end of "Electrical Specifications" on page 11.

6.4.5 Hot Plug Function

When the equipment powers up, there is a period of time where the controller driving the RS-485 enable lines is unable to ensure that the driver and receiver outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL315xE devices incorporate a Hot Plug function. During power-up and power-down, the Hot Plug function disables the driver and receiver outputs regardless of the states of DE and $\overline{RE}$. When V_{CC} reaches ~3.4V, the enable pins are released. This gives the controller the chance to stabilize and drive the RS-485 enable lines to the proper states.

6.4.6 High ESD Protection

The bus pins of the ISL315xE transceivers have on-chip ESD protection against ±16.5kV HBM, and ±9kV contact and ±16.5kV air-discharge according to IEC61000-4-2. The difference between the HBM and IEC ESD ratings lies in the test severity, as both standards aim for different application environments.

HBM ESD ratings are component level ratings, used in semiconductor manufacturing in which component handling can cause ESD damage to a single device. Because component handling is performed in a controlled ESD environment, the ESD stress upon a component is drastically reduced. These factors make the HBM test the less severe ESD test.

IEC ESD ratings are system level ratings. These are required in the uncontrolled field environment, where for example, a charged end user can subject handheld equipment to ESD levels of more than 40kV by touching connector pins when plugging or unplugging cables.

The main differences between the HBM and the IEC 61000-4-2 standards are the number of strikes applied during testing and the generator models (Figure 33), which create differences in the waveforms' rise times and peak currents (Figure 34).

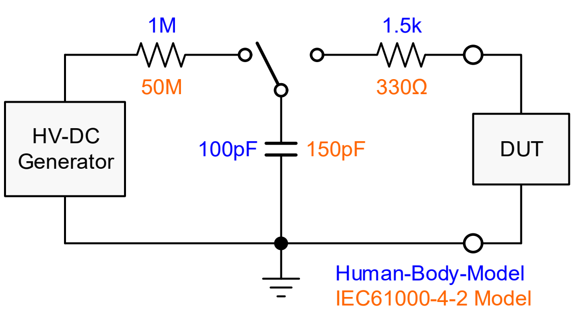


Figure 33. Generator Models for HBM and IEC ESD Tests

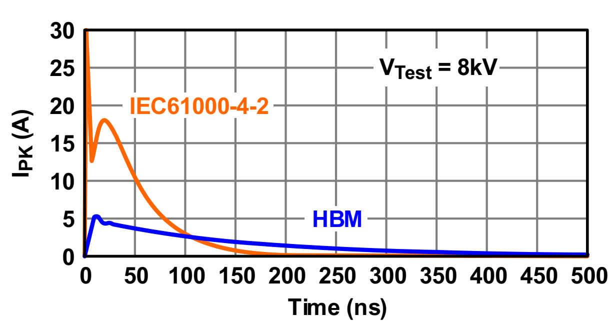


Figure 34. Difference in Rise-time and Charge Currents between HBM and IEC ESD Transients

The IEC model has 50% higher charge capacitance (C_S) and 78% lower discharge resistance (R_D) than the HBM model, thus producing shorter transient rise times and higher discharge currents. The ESD ratings of the ISL315xE transceivers exceed test level 4 of the IEC61000-4-2 standard, which significantly increases equipment robustness.

6.4.7 High EFT Immunity

The bus pins of the ISL315xE transceivers withstand ±4kV Electrical Fast Transient (EFT) immunity per IEC61000-4-4. During the EFT test, the EFT generator produces a burst of 75 fast transients capacitively coupled onto RS-485 data lines using a capacitive clamp (Figure 35).

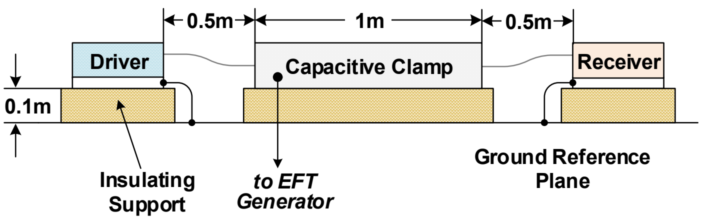


Figure 35. Test Setup with Capacitive Clamp

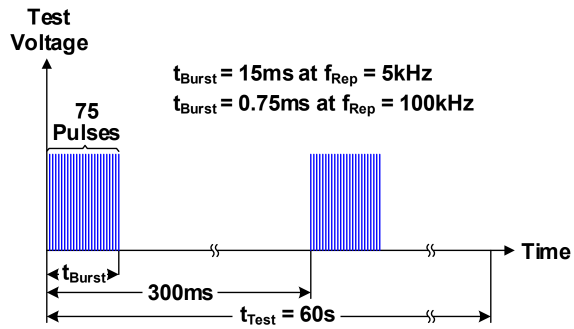


Figure 36. EFT Test Timing

A burst period is 300ms and begins with 75 EFT pulses (t_{Burst}) followed by a break interval (Figure 36). Across a test time of 60 seconds minimum, multiple bursts are applied at a predefined repetition frequency of either 5kHz or 100kHz, unleashing a minimum of 15000 EFT pulses onto the data link. The ISL315xE transceivers have been tested with both repetition frequencies (5kHz and 100kHz).

In the test setup, a complete RS-485 data link (driver, receiver, and unshielded twisted pair cable) was tested during data transmission. Afterward, the devices were tested on an automatic test system (ATE) for parametric performance. The ATE pass criterion requires that a device show no parametric shift.

All ISL315xE transceivers passed the EFT tests with ±4kV test voltage, which places this transceiver family into the highest special test level category of the IEC61000-4-4 standard (Table 4, Test Level X).

Table 4. EFT Test Level Category for ISL315xE Transceivers

Test Level	Test Voltage (V)	Repetition Frequency (kHz)	Components Passing
1	0.25	5 and 100	ISL3150E, ISL3152E, ISL3153E, ISL3155E, ISL3156E, ISL3158E
2	0.5	5 and 100	
3	1	5 and 100	
4	2	5 and 100	
X	4	5 and 100	

7. Application Information

7.1 Network Design

Designing a reliable RS-485 network requires the consideration of a variety of factors that ultimately determine the network performance. These include network topology, cable type, data rate and/or cable length, stub length, distance between network nodes, and line termination.

The main difference between network designs is dictated by their modes of data exchange between bus nodes, which can be half-duplex or full-duplex (Figures 37 and 38).

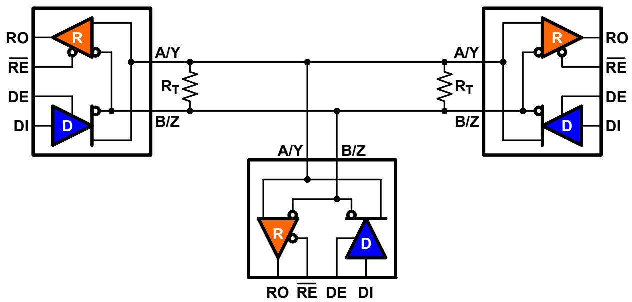


Figure 37. Half-Duplex Bus

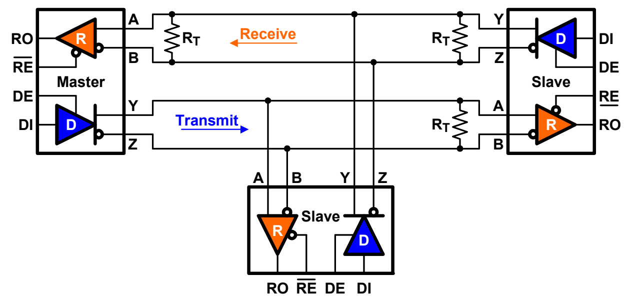


Figure 38. Full-Duplex Bus

Half-duplex networks use only a single signal-pair of cables between one master node and multiple slave nodes, which allows the nodes to either transmit or receive data, but never both at the same time. Its reduced cabling effort makes these networks well suited for covering long distances of up to several thousands of feet. To maintain high signal integrity, the applied data rates range from as low as 9.6kbps up to 115kbps. This requires transceivers with long driver output transition times, typically in the range of microseconds, to ensure low EMI in the presence of large cable inductances.

To prevent signal reflections of the bus lines, each cable end must be terminated with a resistor, R_T, whose value should match the characteristic cable impedance, Z_0.

Full-duplex networks, on the other hand, aim for high data throughput. These networks use two signal-pairs to support the simultaneous transmitting and receiving of data. The signal pair denoted as the transmit path connects the driver output of the master node to the receiver inputs of multiple slave nodes. The other pair connects the driver outputs of the slave nodes with the receiver input of the master node.

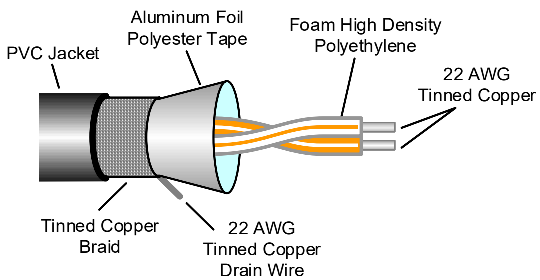
Because the data flow in the transmit path is unidirectional, the transmit path requires only one termination at the remote cable end, opposite the master node. Data flow in the receive path, however, is bidirectional, thus requiring line termination at both cable ends. Commonly, high data throughput also calls for higher data rates in the 1Mbps to 10Mbps range. As cable losses increase with frequency, most full-duplex networks are limited to shorter bus cable lengths of a few hundred feet to maintain signal integrity.

The following sections discuss the aforementioned parameters that impact network performance. This discussion applies to both half-and full-duplex network designs.

7.1.1 Cable Type

RS-485 networks use differential signaling over Unshielded Twisted Pair (UTP) cable. The conductors of a twisted pair are equally exposed to external noise. They pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers.

For best performance use industrial RS-485 cables, which are of the sheathed, shielded, twisted pair type, (STP), with a characteristic impedance of 120Ω and conductor sizes of 22 to 24 AWG (equivalent to diameters of 0.65mm and 0.51mm, respectively). They are available in single, two, and four signal-pair versions to accommodate the design of half- and full-duplex systems. Figure 39 shows the cross section and cable parameters of a typical UTP cable.



Cable:	Belden 3105A
Type:	1-pair, 22AWG PLCT/CM
Impedance:	120Ω
DC Resistance:	14.7mΩ/ft
Capacitance:	11pF/ft
Velocity:	78% (1.3ns/ft)

Figure 39. Single Pair STP Cable for RS-485 Applications

7.1.2 Cable Length vs Data Rate

RS-485 and RS-422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 20Mbps are limited to lengths less than 100ft, while the 115kbps versions can operate at full data rates with lengths of several 1000ft. Note that ISL315xE transceivers can cover almost twice the distance of standard compliant RS-485 transceivers.

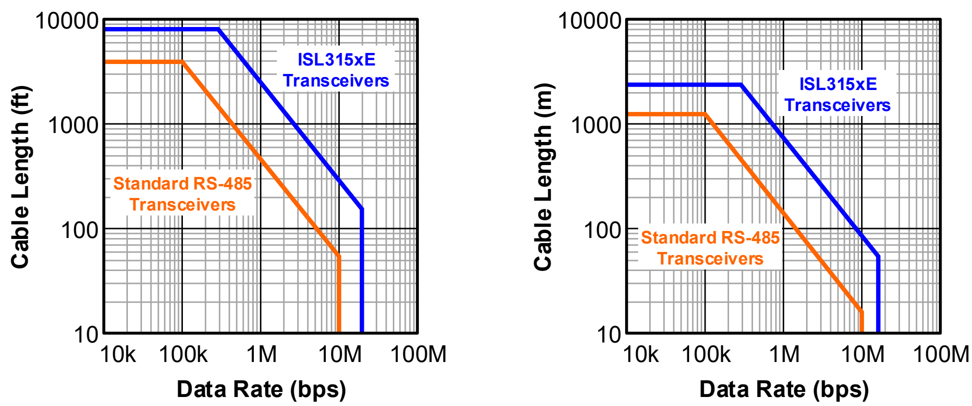


Figure 40. Data Rate vs Cable Length Guidelines in Feet and Meters

7.1.3 Topologies and Stub Lengths

RS-485 recommends its nodes to be networked in daisy-chain or backbone topology. In these topologies the participating drivers, receivers, and transceivers connect to a main cable trunk through "short" stubs. A stub being the actual electrical link between transceiver and cable trunk.

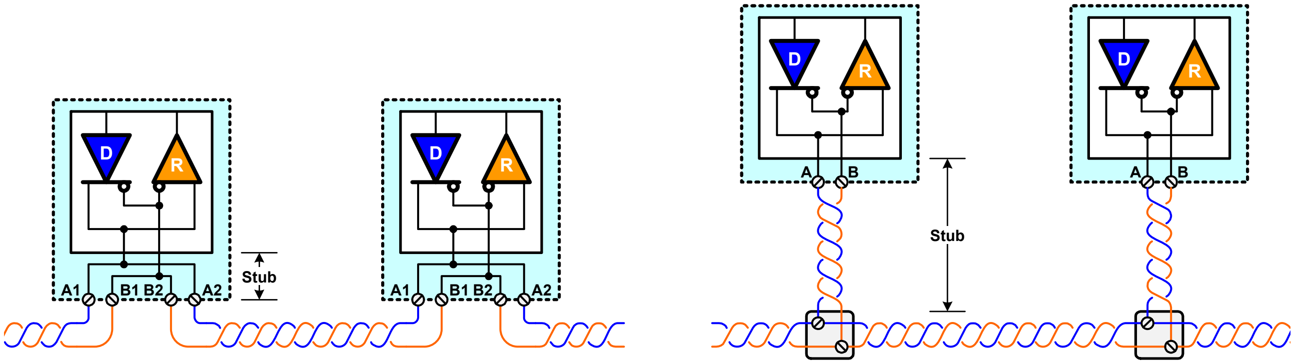


Figure 41. Stub Lengths in Daisy Chain (left) and Backbone (right) Topologies

Because daisy chaining brings the cable trunk much closer to the transceiver bus terminals than a backbone design, the stub lengths between the two topologies can differ significantly. To prevent the bus from being overloaded by line terminations, stubs are never terminated. A stub therefore, represents a piece of unterminated transmission line. To eliminate signal reflections on the stub line, a rule of thumb is to keep its propagation delay below 1/5 of the driver output rise time, which leads to the maximum stub length of:

(EQ. 1) $$L_{Stub} = v \cdot c \cdot \frac{t_r}{5}$$

where

• c is the speed of light (m/s)

• v is the signal velocity in the cable, expressed as a factor of c

• t_r is the rise time of the driver output (ns)

Applying Equation 1 to the ISL315xE transceivers assuming a velocity of 78%, results in the maximum stub lengths associated with the corresponding transceivers, as shown in Table 5.

Table 5. Stub Length as Function of Driver Rise Time

Device	Data Rate (Mbps)	Rise Time (ns)	Maximum Stub Length
ISL3150E, ISL3152E	0.115	1100	168ft (51m)
ISL3153E, ISL3155E	1	150	23ft (7m)
ISL3156E, ISL3158E	20	8	1.2ft (0.36m)

Table 5 proves that transceivers with long driver rise times are well suited for applications requiring long stub lengths and low radiated emission in the presence of increased stub inductance.

7.1.4 Minimum Distance between Nodes

The electrical characteristics of the RS-485 bus are primarily defined by the distributed inductance and capacitance along the bus cable and printed circuit board traces. Adding capacitance to the bus in the form of transceivers and connectors lowers the line impedance and causes impedance mismatches at the loaded bus section.

Input signals arriving at these mismatches are partially reflected back to the signal source, distorting the driver output signal. Ensuring a valid receiver input voltage during the first signal transition from a driver output anywhere on the bus, requires the bus impedance at the mismatches to be $Z_{load} \geq 0.4 Z_{nom}$ or 0.4 x 120Ω = 48Ω. This can be achieved by maintaining a minimum distance between bus nodes of:

(EQ. 2) $$D_{min} \geq \frac{C_L}{5.25 \cdot C_C}$$

where

- C_L is the lumped load capacitance
- C_C is the distributed cable or PCB trace capacitance per unit length.

Figure 42 shows the relationship for the minimum node spacing as a function of C_C and C_L graphically. Load capacitance includes contributions from the line circuit bus pins, connector contacts, printed circuit board traces, protection devices, and any other physical connections to the trunk line as long as the distance from the bus to the transceiver, known as the stub, is electrically short.

Putting some values to the individual capacitance contributions: 5V transceivers typically possess a capacitance of 7pF, while 3V transceivers have about twice that capacitance at 16pF. Board traces add about 1.3 to 2pF/in depending upon their construction.

Connector and suppression device capacitance can vary widely. Media distributed capacitance ranges from 11pF/ft for low capacitance, unshielded, twisted-pair cable up to 22pF/ft for backplanes.

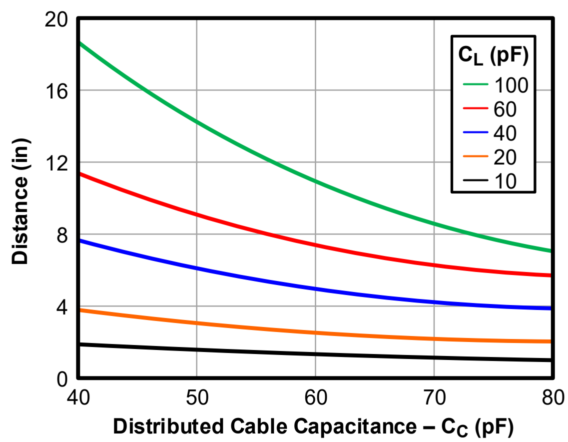


Figure 42. Minimum Distance between Bus Nodes as Function of Cable and Load Capacitance

7.1.5 Failsafe Biasing Termination

As mentioned in "Full-Failsafe Receiver" on page 20, the ISL315xE transceivers are full-failsafe and capable of tolerating up to 140mV$_{P-P}$ of differential noise on a passive bus without needing external failsafe biasing.

However, in harsh industrial environments, such as the factor floors in industrial automation, the differential noise can reach levels of more than 1V$_{P-P}$. In this case external failsafe biasing at the network's line terminations is strongly recommended. Here the termination resistors R_T connect through the biasing resistors R_B to the supply rails V_{CC} and GND.

Short data links (<100m) only require a single failsafe termination at one cable end, while the other end is terminated with the cable characteristic impedance Z_0 (Figure 43, left circuit).

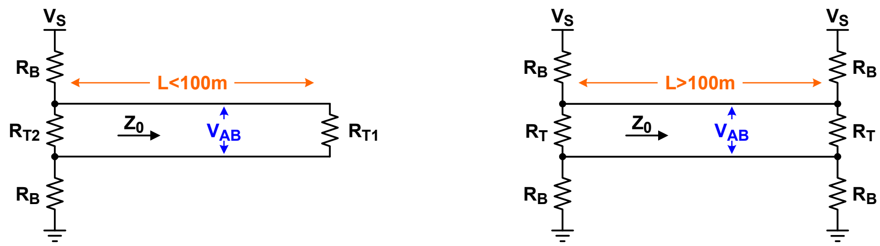


Figure 43. Failsafe Biasing of Short (<100m) and Long (>100m) Data Links

The corresponding resistor values are calculated with Equations 3 to 5.

(EQ. 3) $$R_B = \frac{V_S/V_{AB}+1}{0.036}$$

(EQ. 4) $$R_{T2} = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

(EQ. 5) $$R_{T1} = 120\Omega$$

Longer data links (>100m) require two identical failsafe basing networks, one at each cable end, to minimize the differential voltage drop along the bus (Figure 43, right circuit). Their resistor values are calculated using Equations 6 and 7:

(EQ. 6) $$R_B = \frac{2V_S/V_{AB}+1}{0.036}$$

(EQ. 7) $$R_T = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

Note that Equations 3 to 7 apply to the multi-driver applications of half- and full-duplex networks. For single driver applications, the values of R_B and R_T are calculated using Equations 8 and 9.

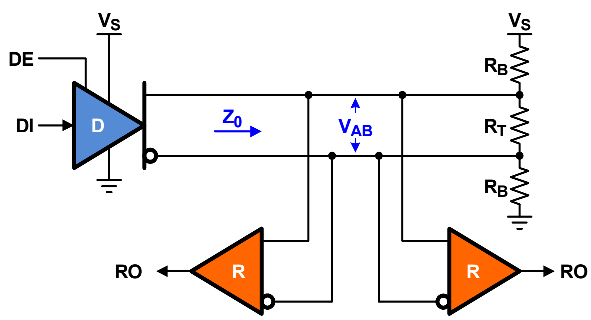


Figure 44. Failsafe Biasing of a Single-Driver Network

(EQ. 8) $$R_B = 60\Omega \cdot \frac{V_S}{V_{AB}}$$

(EQ. 9) $$R_T = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

For more details on failsafe biasing refer to TB509.

7.2 Transient Protection

Although the ISL315xE transceivers have on-chip transient protection circuitry against Electrostatic Discharge (ESD), they are vulnerable to bursts of Electrical Fast Transients (EFT) and surge transients. Surge transients can be caused by lightning strikes or the switching of power systems including load changes and short circuits. Their energy content is up to 8 million times higher than that of ESD transients and thus, requires the addition of external transient protection.

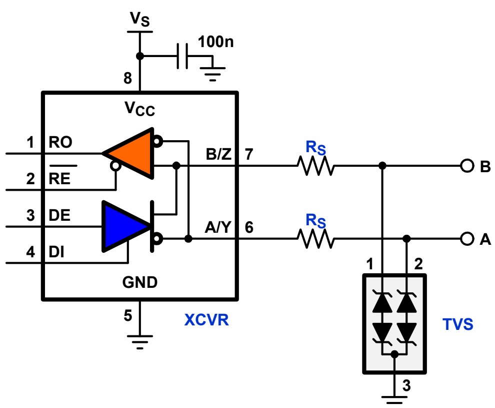
Because standard RS-485 transceivers have asymmetric stand-off voltages of -9V and +14V, external protection requires a bidirectional Transient Voltage Suppressor (TVS) with asymmetric breakdown voltages. The only device satisfying this requirement is the 400W TVS, SM712.

The SM712 operates across the asymmetrical common-mode voltage range from -7V to +12V. The device protects transceivers against ESD, EFT, and surge transients up to the following levels:

- IEC61000-4-2 (ESD) +15kV (air), +8kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)
- IEC61000-4-5 (Lightning) 12A (8/20µs)

Because the transceiver's ESD cells and the SM712 have a similar switching characteristics, series resistors (R_S) are used to prevent the two protection schemes from interacting with one another.

These resistors can be carbon composite or pulse-proof thick-film resistors which should be inserted between the TVS and the transceiver bus terminals to limit the bus currents into the transceiver during a surge event. Their value should be less than 20Ω to minimize the attenuation of the bus voltage during normal operation. Figure 45 shows the schematic of a 1kV surge protection example for the ISL3152E and its bill of materials.



Name	Function	Order No.	Vendor
XCVR	5V, 115kbps transceiver	ISL3152EIBZ	Renesas
TVS	400W (8,20µs), bidirectional TVS	SM712.TCT	Semtech
RS	10Ω, 0.2W, pulse-proof thick-film resistor	CRCW0603-HP e3 series	Vishay

Figure 45. IEC61000-4-5 Level 2 (1kV) Surge Protection and Associated Bill of Materials

For more information on transient protection, refer to AN1976, AN1977, AN1978, and AN1979.

7.3 Layout Guidelines

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design.

- For your PCB design to be successful, start with the design of the protection circuit in mind.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.

- Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize the effective via-inductance.
- Use 1kΩ to 10kΩ pull-up/down resistors for the transceiver enable lines to limit noise currents into these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

7.3.1 Layout Example

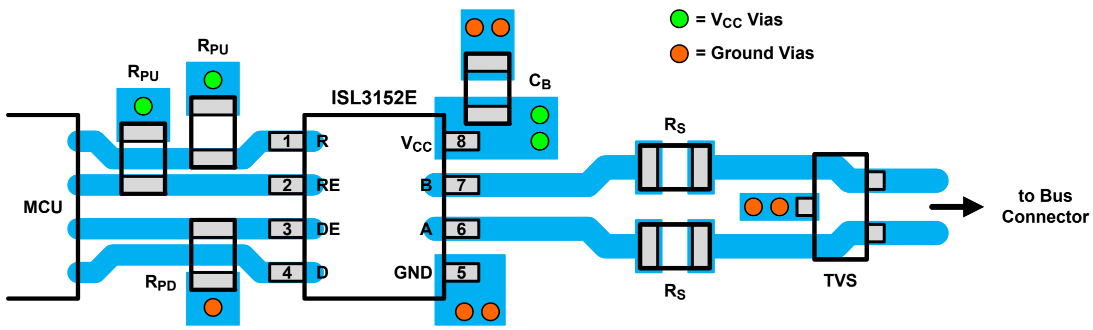


Figure 46. ISL3152E Layout Example

8. Revision History

Revision	Date	Description
5.2	Feb 16, 2023	Updated page 1 description. Added Feature bullet. Added High EFT Immunity section.
5.1	May 11, 2021	Updated Links throughout. Removed obsolete PDIP part and applicable information throughout. Updated Ordering Information table formatting. Updated Figure 18. Updated POD M8.15 to the latest revision, changes are as follows: -Added the coplanarity spec into the drawing Updated PODs M8.118 and M10.118 to the latest revisions, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated POD M14.15 to the latest revision, changes are as follows: -In Side View B and Detail A added lead length dimension (1.27 – 0.40) Changed angle of the lead to 0-8 degrees.
5.0	Jun 3, 2020	Changed minimum value for maximum data rate from 115kbps to 115.2kbps on page 8.
4.0	Apr 19, 2018	Updated to the latest Renesas formatting. Updated title. Updated Application and Features bullets. Updated Table 1. Updated Ordering Information table by adding all available parts, updating Note 1, and removing Notes 2 through 5. Updated Pin Descriptions. Updated Figures 1 through 9. Updated Recommended Operating Conditions - Supply Voltage. Added Device Description sections Rewrote the Application Information sections. Added the following Typical Performance curves: -Driver Output High and Low Voltages vs Output Current -Driver Output Voltages vs Common-Mode Voltage -Driver Output Voltage vs Supply Voltage -Supply Current vs Data Rate for all three data rate versions
3.0	Aug 23, 2017	Updated the Receiving Truth Table. Updated header/footer. Updated the POD M8.118 from revision 2 to revision 4. Changes since revision 2: -Updated to new format by adding land pattern and moving dimensions from the table to the drawing. -Corrected lead width dimension in side view 1 from “0.25 - 0.036” to “0.25 - 0.36”. Updated the POD M10.118 from revision 0 to revision 1. Changes since revision 0: -Updated to new format by adding land pattern and moving dimensions from the table to the drawing. Updated the POD M14.15 from revision 0 to revision 1. Changes since revision 0: -Updated to new format by adding land pattern and moving dimensions from the table to the drawing. Updated the POD M8.15 from revision 1 to revision 4. Changes since revision 1: -Changed Note 1 “1982” to “1994” -In the Typical Recommended Land pattern, changed the following: 2.41 (0.095) to 2.20 (0.087) 0.76 (0.030) to 0.60 (0.023) 0.20 to 5.20 (0.205) Updated to new format by adding land pattern and moving dimensions from the table to the drawing.
2.0	Jun 30 2009	Converted to new Intersil template. Rev. 2 changes are as follows: Page 1 – Introduction was reworded to fit graphs. Features section by listing only key features. Added performance graphs. Page – 2 Updated Ordering Information by numbering all notes and referencing them on each part. Added MSL Note as new standard with linked parts to device info page. Updated Pinout name to Pin Configurations with Pin Descriptions following on page 3. Page 5 – Added Boldface limit verbiage in Electrical specifications table and added bold formatting for Min and Max over-temperature limits. Page 17 – Added Revision History and Products information with all links included.

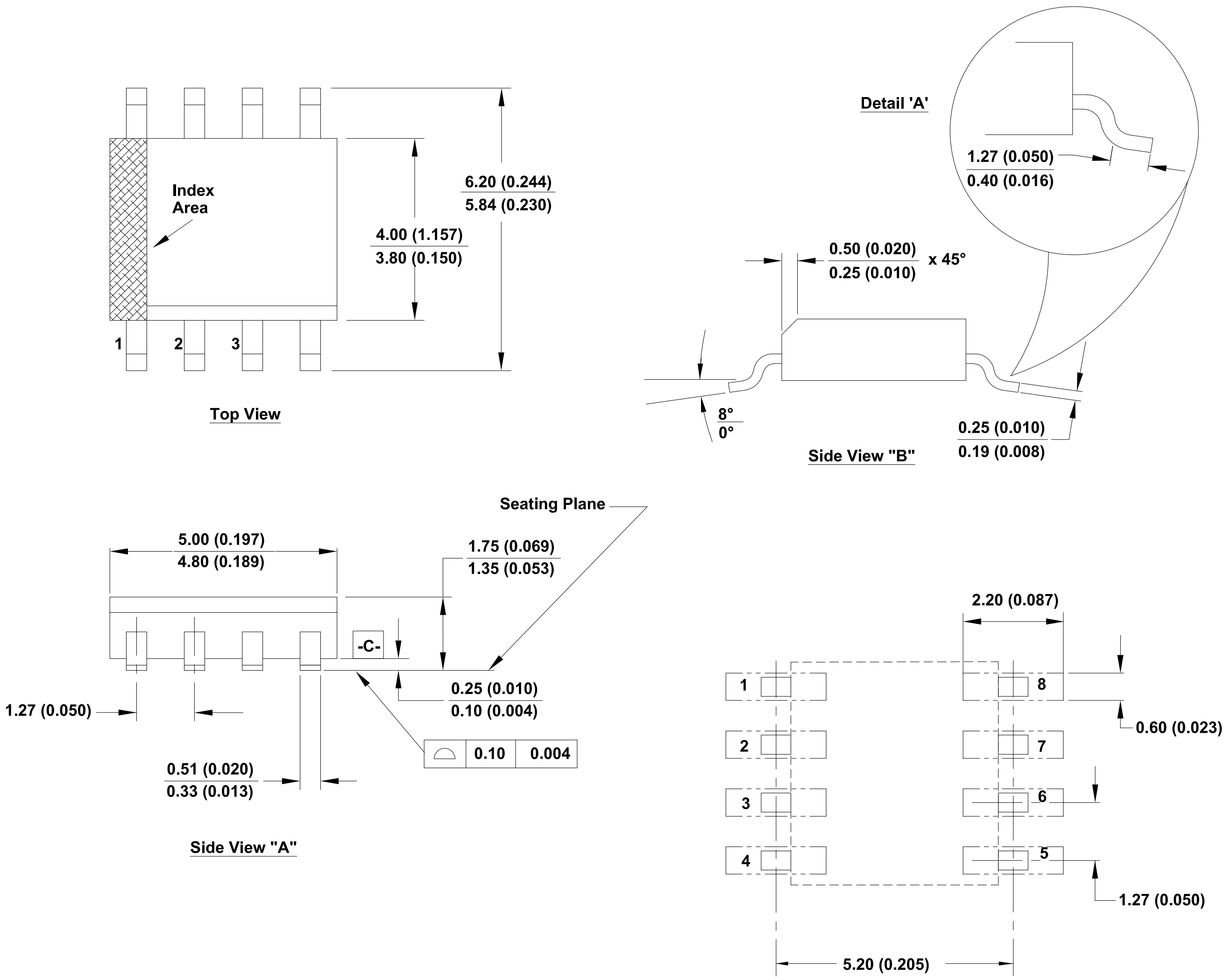
Revision	Date	Description
1.0	Jan 17 2008	Added 8 Ld PDIP to ordering information, POD, and Thermal resistance. Applied Intersil Standards as follows: Updated ordering information with Notes for tape and reel reference, Pb-free PDIP and lead finish. Added Pb-free reflow link and Pb-free note to Thermal Information. Added E8.3 POD.
0.0	Dec 14, 2006	Initial release

9. Package Outline Drawings

For the most recent package outline drawing, see M8.15.

M8.15

8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021

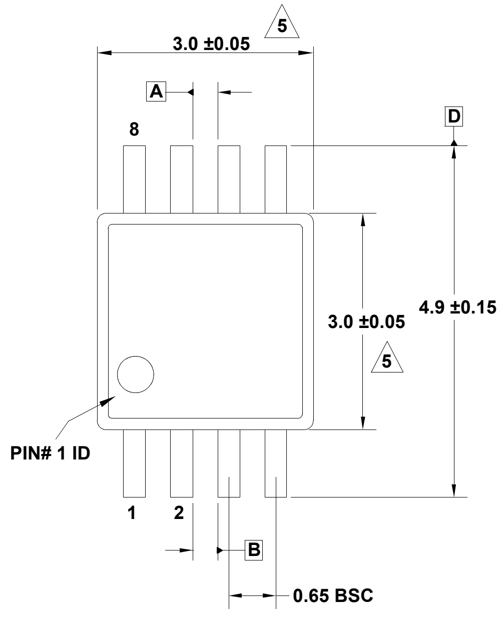


NOTES:

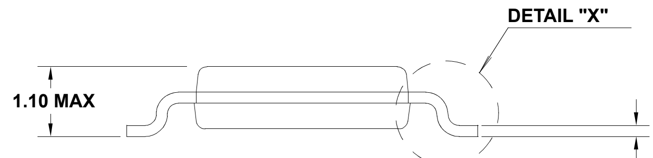
1 Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2 Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. if it is not present, a visual index feature must be located within the crosshatched area.
5 Terminal numbers are shown for reference only.
6 The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7 Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8 This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see M8.118.

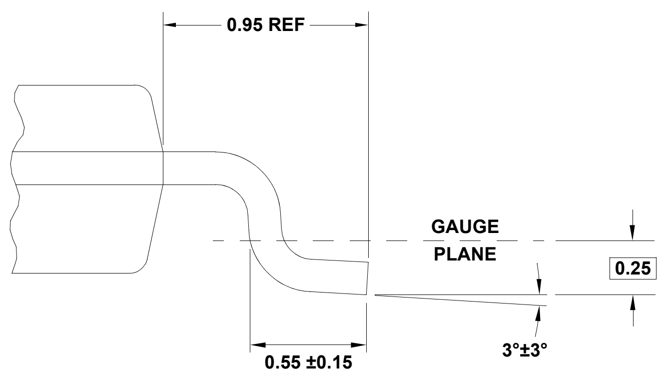
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



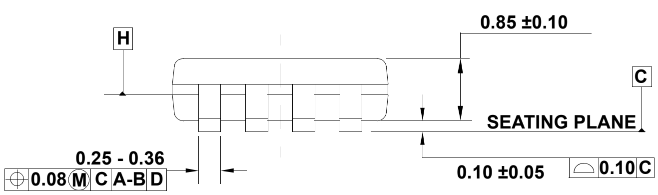
TOP VIEW



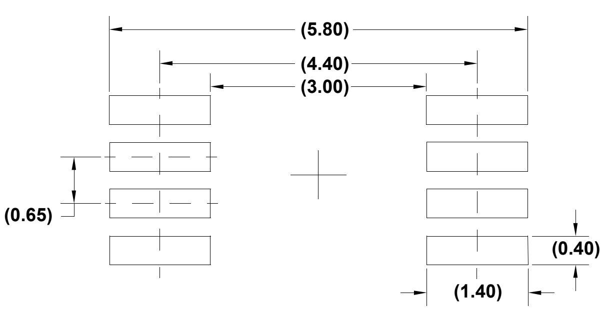
SIDE VIEW 2



DETAIL “X”



SIDE VIEW 1



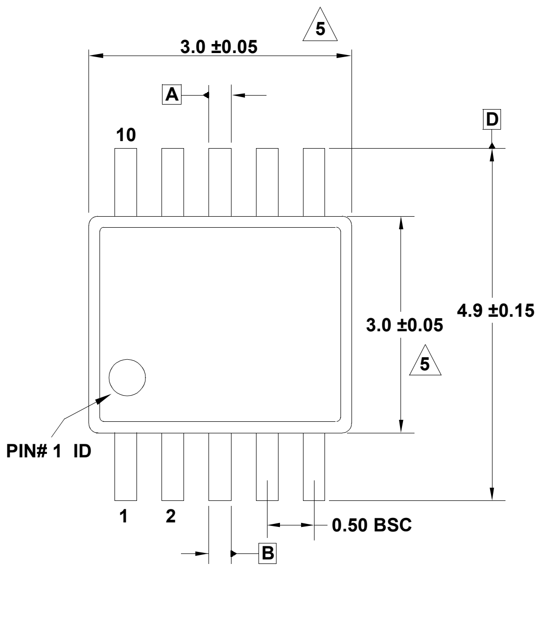
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

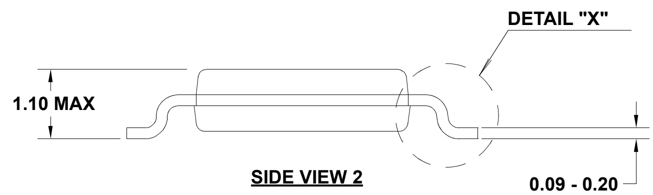
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane “H”.
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see M10.118.

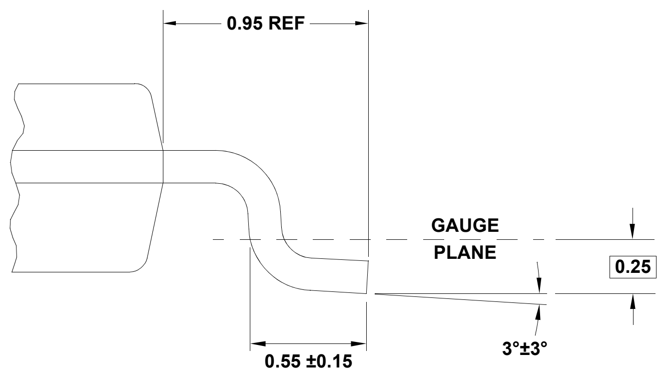
M10.118
10 Lead Mini Small Outline Plastic Package
Rev 2, 5/2021



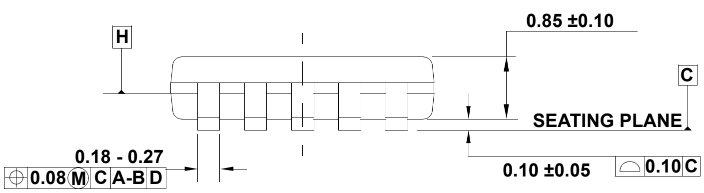
TOP VIEW



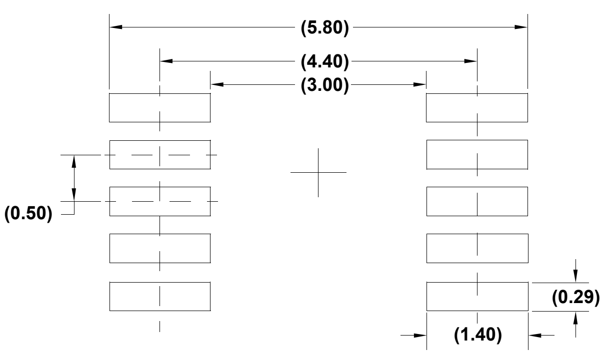
SIDE VIEW 2



DETAIL “X”



SIDE VIEW 1



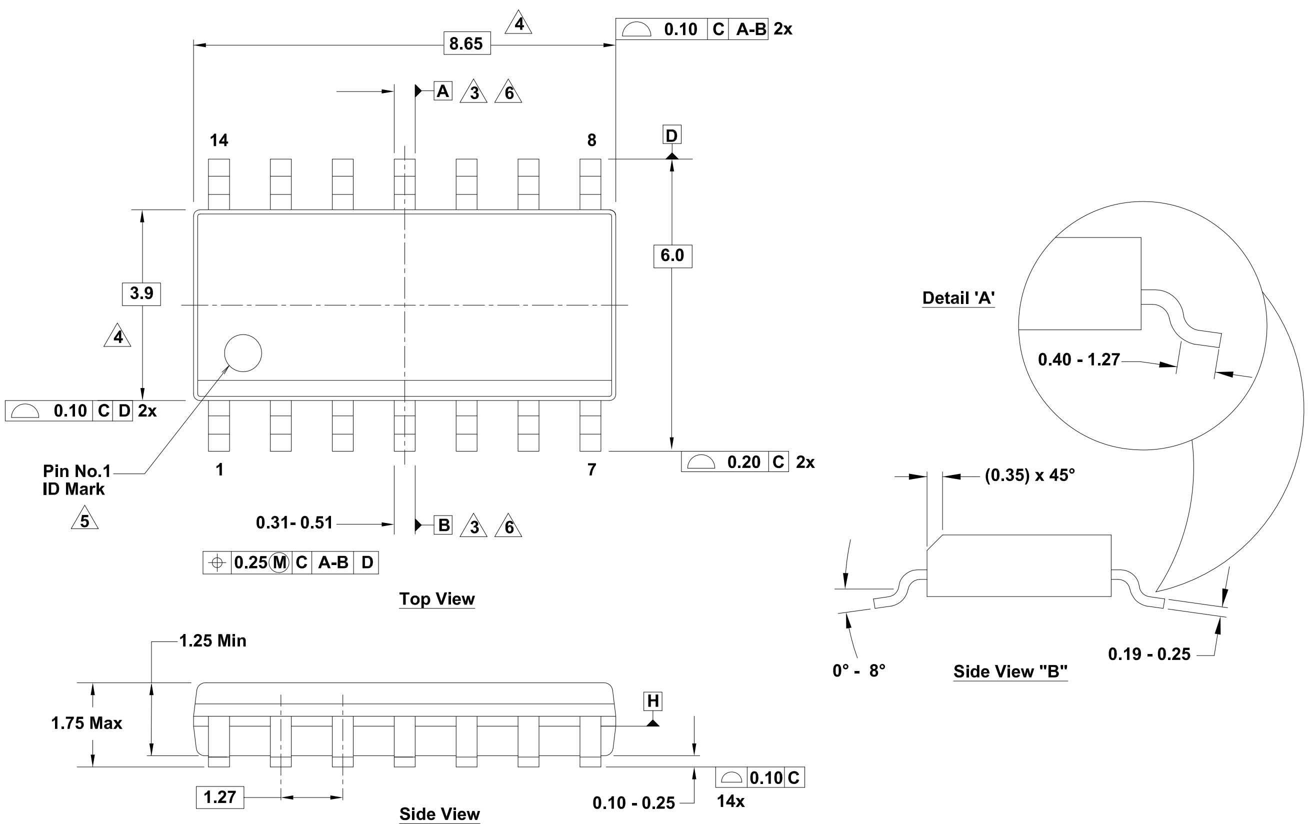
TYPICAL RECOMMENDED LAND PATTERN

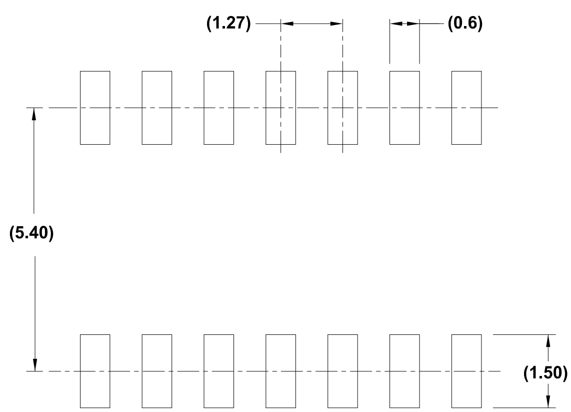
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane “H”.
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see M14.15.

M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

IMPORTANT NOTICE AND DISCLAIMER

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks