# CAT93C46

## 1K-Bit Microwire Serial EEPROM

## FEATURES

- **High speed operation: 1MHz**
- **Low power CMOS technology**
- **1.8 to 5.5 volt operation**
- **Selectable x8 or x16 memory organization**
- **Self-timed write cycle with auto-clear**
- **Hardware and software write protection**
- **Power-up inadvertant write protection**
- **1,000,000 Program/erase cycles**
- **100 year data retention**
- **Industrial temperature ranges**
- **RoHS-compliant packages**

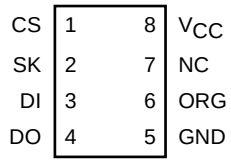
**For Ordering Information details, see page 14.**

## DESCRIPTION

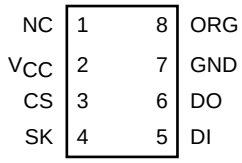
The CAT93C46 is a 1K-bit Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at $V_{CC}$) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP, 8-pin SOIC, 8-pin TSSOP and 8-pad TDFN packages.

## PIN CONFIGURATION

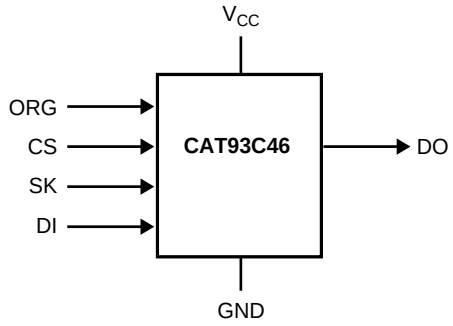
**PDIP (L)**
**SOIC (V, X)**
**TSSOP (Y)**
**TDFN (VP2)**




**SOIC (W)**




## FUNCTIONAL SYMBOL




## PIN FUNCTIONS

| Pin Name | Function |
|---|---|
| CS | Chip Select |
| SK | Clock Input |
| DI | Serial Data Input |
| DO | Serial Data Output |
| $V_{CC}$ | +1.8 to 5.5V Power Supply |
| GND | Ground |
| ORG | Memory Organization |
| NC | No Connection |

Note: When the ORG pin is connected to VCC, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.





Doc. No. 1106, Rev. E

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground (1) | -0.5 V to +6.5 V |

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

## RELIABILITY CHARACTERISTICS(2)

| Symbol | Parameter | Min | Units |
|---|---|---|---|
| $N_{END}$(*) | Endurance | 1,000,000 | Program/ Erase Cycles |
| $T_{DR}$ | Data Retention | 100 | Years |

(*) Block Mode, $V_{CC}$ = 5.0V, 25°C

## D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +1.8V to +5.5V, $T_A$=-40°C to +85°C, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Power Supply Current (Write) | $f_{SK}$ = 1MHz<br>$V_{CC}$ = 5.0V | | | 3 | mA |
| $I_{CC2}$ | Power Supply Current (Read) | $f_{SK}$ = 1MHz<br>$V_{CC}$ = 5.0V | | | 500 | µA |
| $I_{SB1}$ | Power Supply Current (Standby) (x8 Mode) | $V_{IN}$=GND or $V_{CC}$, CS =GND<br>ORG=GND | | | 10 | µA |
| $I_{SB2}$ | Power Supply Current (Standby) (x16Mode) | $V_{IN}$=GND or $V_{CC}$, CS =GND<br>ORG=Float or $V_{CC}$ | | 0 | 10 | µA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | | 2 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = GND to $V_{CC}$,<br>CS = GND | | | 2 | µA |
| $V_{IL1}$ | Input Low Voltage | 4.5V ≤ $V_{CC}$ < 5.5V | -0.1 | | 0.8 | V |
| $V_{IH1}$ | Input High Voltage | 4.5V ≤ $V_{CC}$ < 5.5V | 2 | | $V_{CC}$ + 1 | V |
| $V_{IL2}$ | Input Low Voltage | 1.8V ≤ $V_{CC}$ < 4.5V | 0 | | $V_{CC}$ x 0.2 | V |
| $V_{IH2}$ | Input High Voltage | 1.8V ≤ $V_{CC}$ < 4.5V | $V_{CC}$ x 0.7 | | $V_{CC}$+1 | V |
| $V_{OL1}$ | Output Low Voltage | 4.5V ≤ $V_{CC}$ < 5.5V<br>$I_{OL}$ = 2.1mA | | | 0.4 | V |
| $V_{OH1}$ | Output High Voltage | 4.5V ≤ $V_{CC}$ < 5.5V<br>$I_{OH}$ = -400µA | 2.4 | | | V |
| $V_{OL2}$ | Output Low Voltage | 1.8V ≤ $V_{CC}$ < 4.5V<br>$I_{OL}$ = 1mA | | | 0.2 | V |
| $V_{OH2}$ | Output High Voltage | 1.8V ≤ $V_{CC}$ < 4.5V<br>$I_{OH}$ = -100µA | $V_{CC}$ - 0.2 | | | V |

Note:
(1) The DC input voltage on any pin should not be lower than -0.5V or higher than $V_{CC}$ +0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than $V_{CC}$ +1.5V, for periods of less than 20 ns.
(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

## PIN CAPACITANCE

$T_A$=25°C, f=1MHz, $V_{CC}$=5V

| Symbol | Test | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $C_{OUT}$(1) | Output Capacitance (DO) | $V_{OUT}$=0V | | | 5 | pF |
| $C_{IN}$(1) | Input Capacitance (CS, SK, DI, ORG) | $V_{IN}$=0V | | | 5 | pF |

## A.C. CHARACTERISTICS

$V_{CC}$ = +1.8V to +5.5V, $T_A$=-40°C to +85°C, unless otherwise specified.

| | | Limits | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Units** |
| $t_{CSS}$ | CS Setup Time | 50 | | ns |
| $t_{CSH}$ | CS Hold Time | 0 | | ns |
| $t_{DIS}$ | DI Setup Time | 100 | | ns |
| $t_{DIH}$ | DI Hold Time | 100 | | ns |
| $t_{PD1}$ | Output Delay to 1 | | 0.25 | µs |
| $t_{PD0}$ | Output Delay to 0 | | 0.25 | µs |
| $t_{HZ}$(1) | Output Delay to High-Z | | 100 | ns |
| $t_{EW}$ | Program/Erase Pulse Width | | 10 | ms |
| $t_{CSMIN}$ | Minimum CS Low Time | 0.25 | | µs |
| $t_{SKHI}$ | Minimum SK High Time | 0.25 | | µs |
| $t_{SKLOW}$ | Minimum SK Low Time | 0.25 | | µs |
| $t_{SV}$ | Output Delay to Status Valid | | 0.25 | µs |
| $SK_{MAX}$ | Maximum Clock Frequency | DC | 1000 | kHz |
| | | | | |

## POWER-UP TIMING (1)(3)

| Symbol | Parameter | Max | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-up to Read Operation | 1 | ms |
| $t_{PUW}$ | Power-up to Write Operation | 1 | ms |

NOTES:
(1) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
(2) Test conditions according to “AC Test Conditions” table.
(3) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified operation can be initiated.

### A.C. TEST CONDITIONS

| | | |
|---|---|---|
| Input Rise and Fall Times | ≤ 50ns | |
| Input Pulse Voltages | 0.4V to 2.4V | $4.5V \le V_{CC} \le 5.5V$ |
| Timing Reference Voltages | 0.8V, 2.0V | $4.5V \le V_{CC} \le 5.5V$ |
| Input Pulse Voltages | $0.2V_{CC}$ to $0.7V_{CC}$ | $1.8V \le V_{CC} \le 4.5V$ |
| Timing Reference Voltages | $0.5V_{CC}$ | $1.8V \le V_{CC} \le 4.5V$ |
| Output Load | Current Source $I_{OLmax}/I_{OHmax}$; $C_L$=100pF | |

## DEVICE OPERATION

The CAT93C46 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The CAT93C46 operates on a single power supply and will generate on chip the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organization).

### Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ($t_{PD0}$ or $t_{PD1}$).

### Erase/Write Enable and Disable

The CAT93C46 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

### INSTRUCTION SET

| Instruction | Start Bit | Opcode | Address | | Data | | Comments |
|---|---|---|---|---|---|---|---|
| | | | x8 | x16 | x8 | x16 | |
| READ | 1 | 10 | A6-A0 | A5-A0 | | | Read Address AN– A0 |
| ERASE | 1 | 11 | A6-A0 | A5-A0 | | | Clear Address AN– A0 |
| WRITE | 1 | 01 | A6-A0 | A5-A0 | D7-D0 | D15-D0 | Write Address AN– A0 |
| EWEN | 1 | 00 | 11XXXXX | 11XXXX | | | Write Enable |
| EWDS | 1 | 00 | 00XXXXX | 00XXXX | | | Write Disable |
| ERAL | 1 | 00 | 10XXXXX | 10XXXX | | | Clear All Addresses |
| WRAL | 1 | 00 | 01XXXXX | 01XXXX | D7-D0 | D15-D0 | Write All Addresses |

**Figure 1. Sychronous Data Timing**

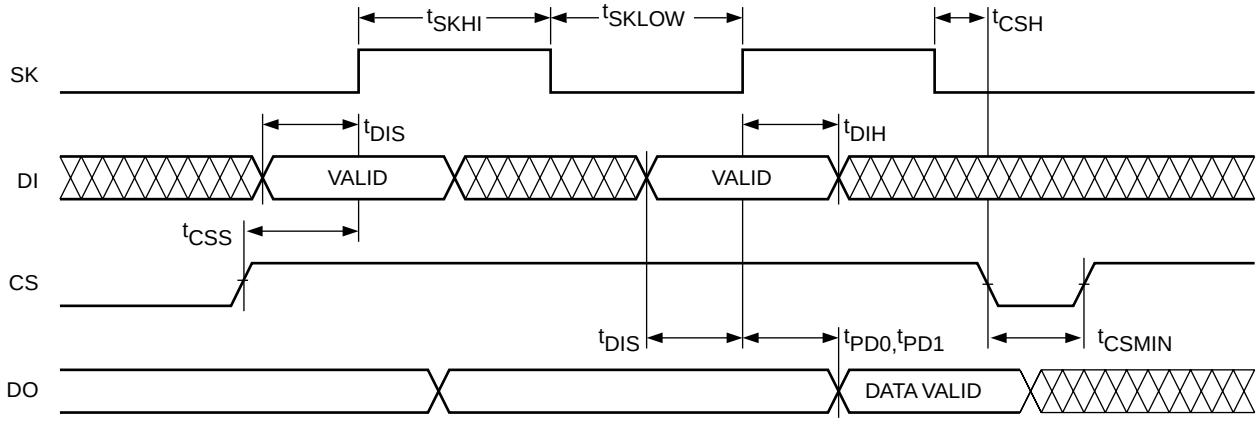



**Figure 2. Read Instruction Timing**

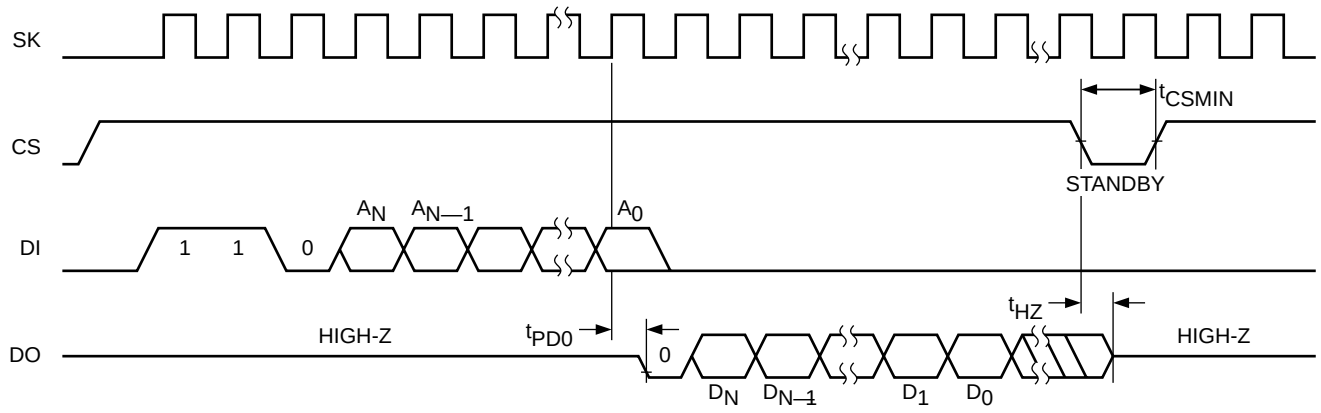
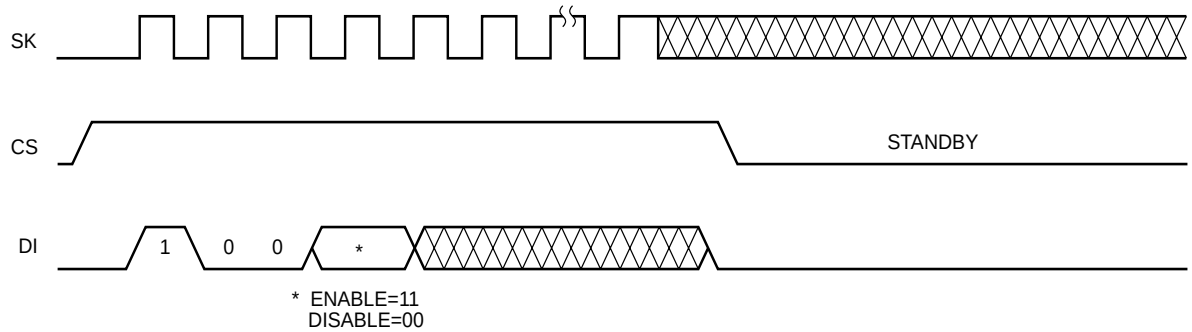



**Figure 3. EWEN/EWDS Instruction Timing**



### Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking for auto-clear and data store cycles on the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

### Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

### Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

### Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

**Figure 4. Write Instruction Timing**

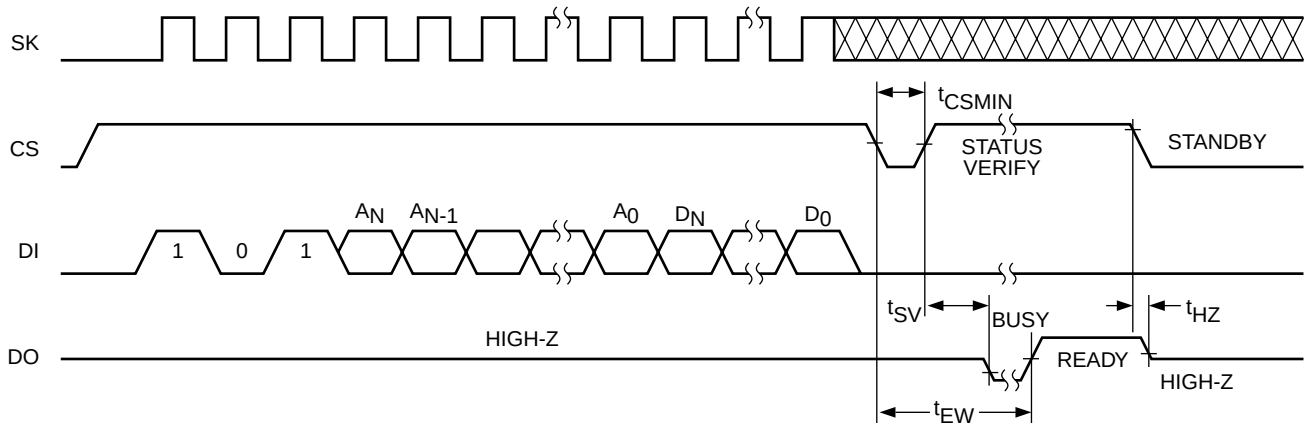


**Figure 5. Erase Instruction Timing**

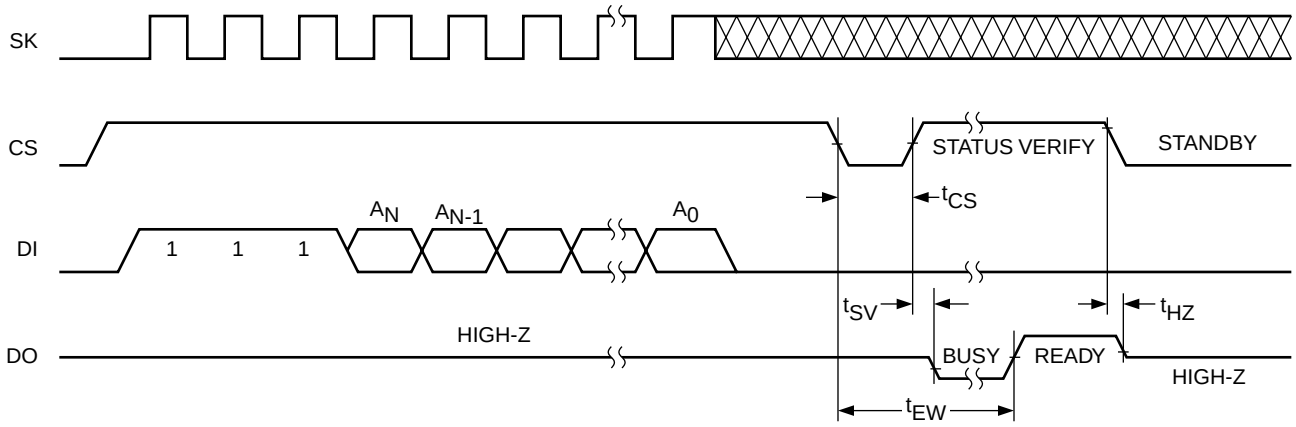



**Figure 6. ERAL Instruction Timing**

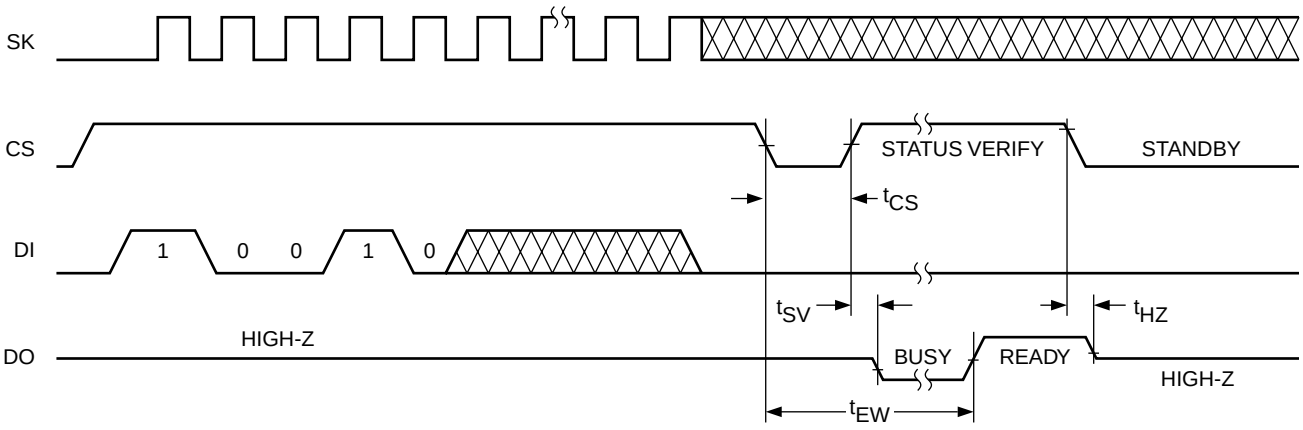
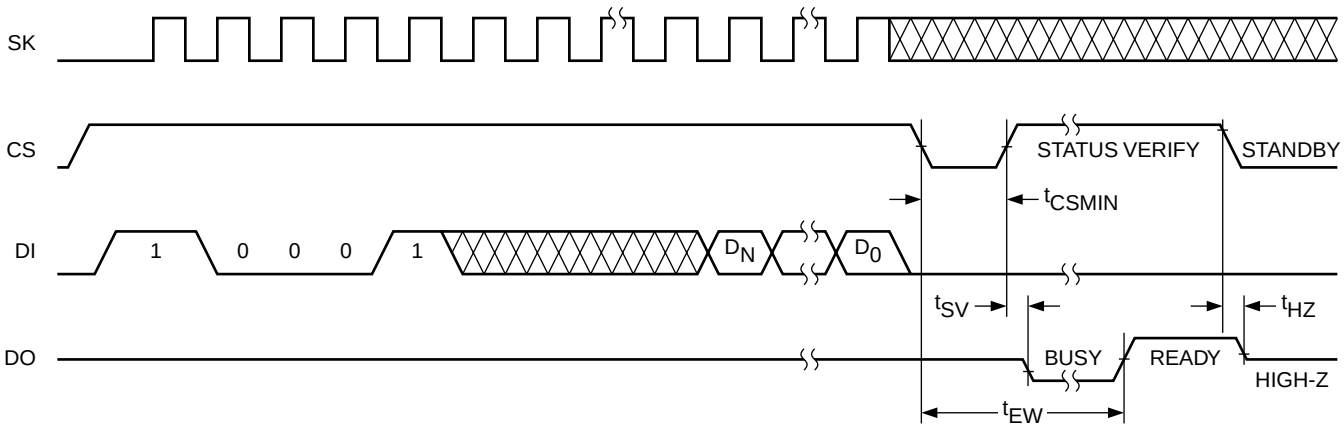
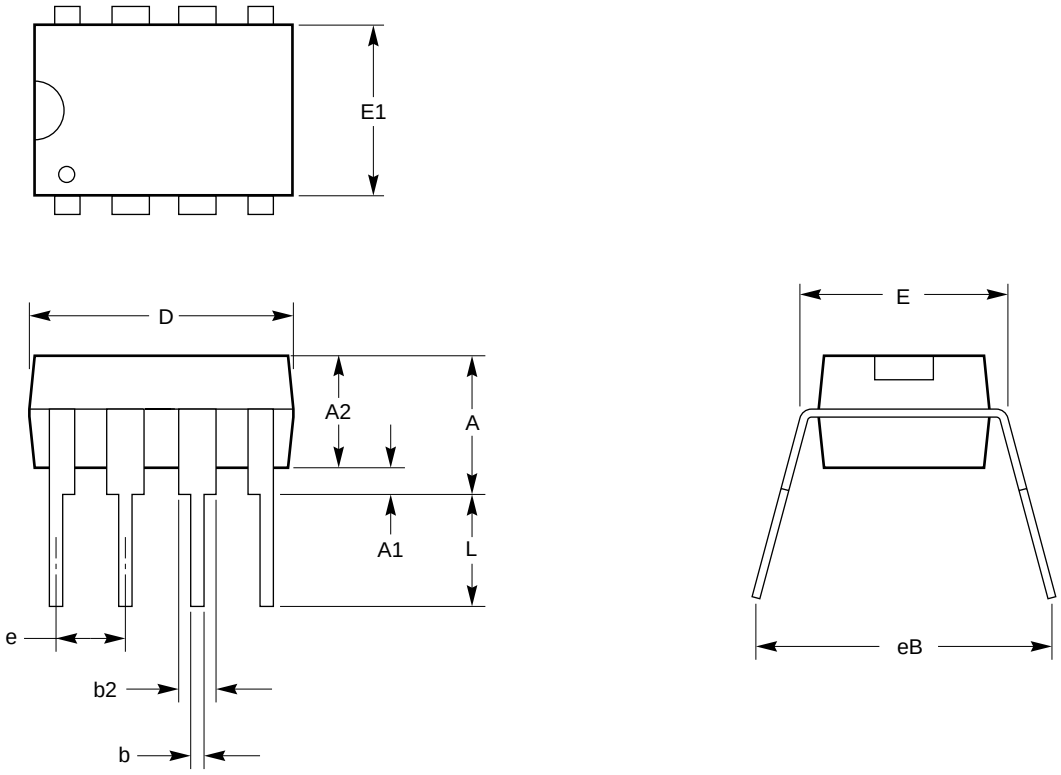



**Figure 7. WRAL Instruction Timing**



## 8-LEAD 300 MIL WIDE PLASTIC DIP (L)

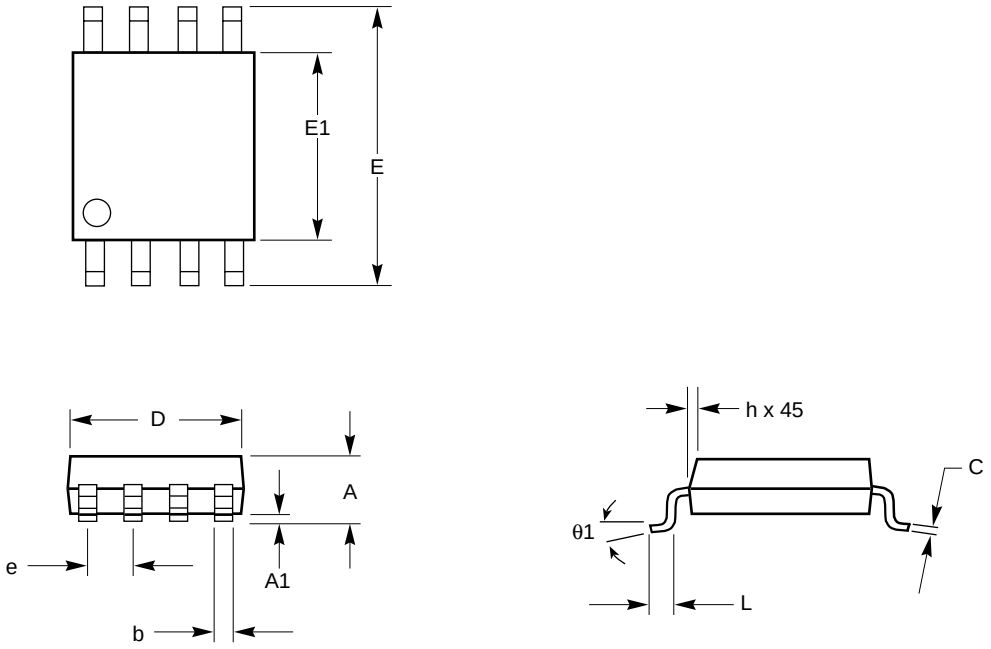



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 4.57 |
| A1 | 0.38 | | |
| A2 | 3.05 | | 3.81 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | | 1.77 |
| D | 9.02 | | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| E1 | 6.09 | 6.35 | 7.11 |
| e | | 2.54 BSC | |
| eB | 7.87 | | 9.65 |
| L | 0.115 | 0.130 | 0.150 |

24C16_8-LEAD_DIP_(300P).eps

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MS001.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

## 8-LEAD 150 MIL WIDE SOIC (V, W)

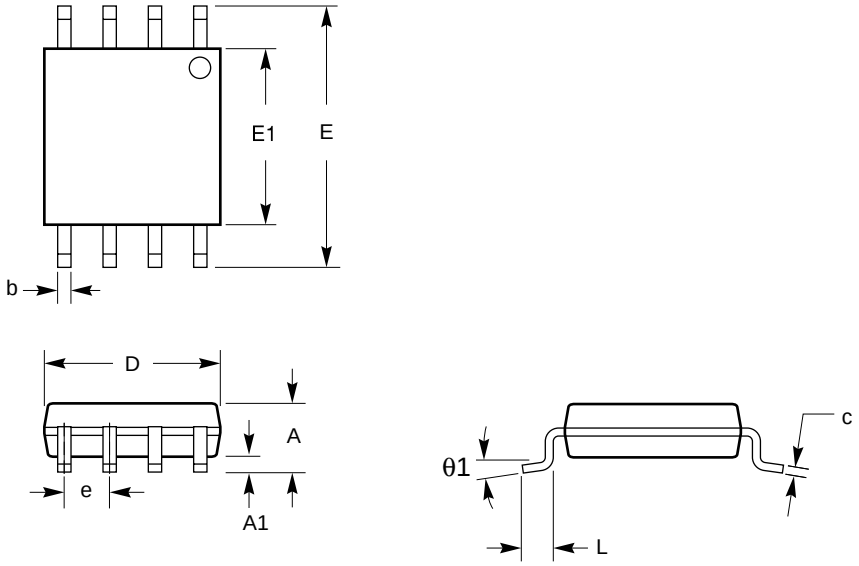



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A1 | 0.10 | | 0.25 |
| A | 1.35 | | 1.75 |
| b | 0.33 | | 0.51 |
| C | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ1 | 0° | | 8° |

24C16_8-LEAD_SOIC.eps

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-012.

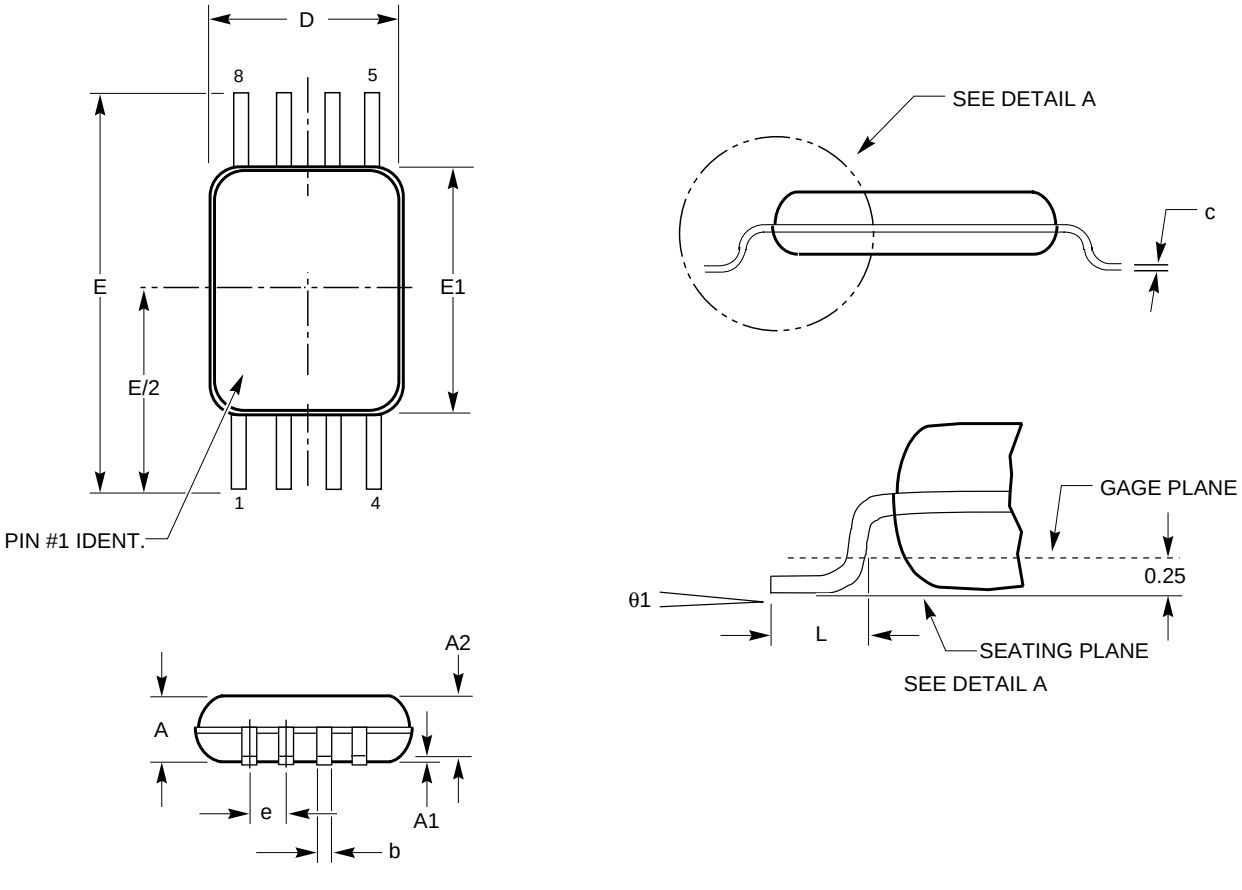
## 8-LEAD 208 MIL SOIC (X)




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A1 | 0.05 | | 0.25 |
| A | | | 2.03 |
| b | 0.36 | | 0.48 |
| c | 0.19 | | 0.25 |
| D | 5.13 | | 5.33 |
| E | 7.75 | | 8.26 |
| E1 | 5.13 | | 5.38 |
| e | | 1.27 BSC | |
| L | 0.51 | | 0.76 |
| θ1 | 0° | | 8° |

Notes:
1. All dimensions are in millimeters.
2. Complies with EIAJ specification EDR-7320.
3. D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.06in per side.
4. E1 does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010in per side.
5. Lead span/stand off height/coplanarity are considered as special characteristic (A1).

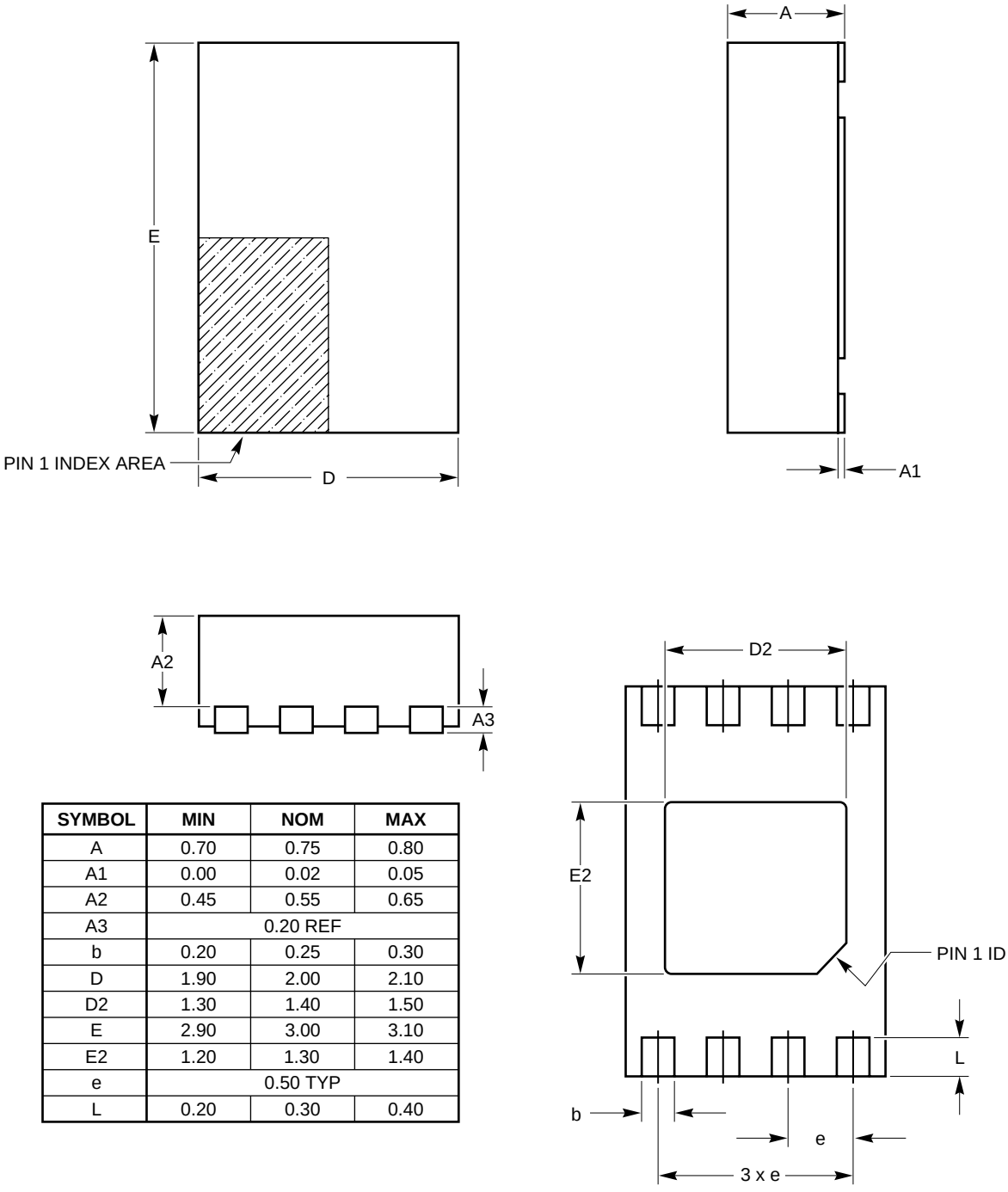
## 8-LEAD TSSOP (Y)




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.4 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 BSC | |
| L | 0.50 | 0.60 | 0.75 |
| θ1 | 0.00 | | 8.00 |

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MO-153

## 8-PAD TDFN 2X3 PACKAGE (VP2)

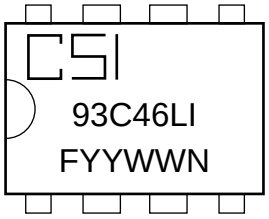



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.45 | 0.55 | 0.65 |
| A3 | | 0.20 REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.30 | 1.40 | 1.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.20 | 1.30 | 1.40 |
| e | | 0.50 TYP | |
| L | 0.20 | 0.30 | 0.40 |

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-229.

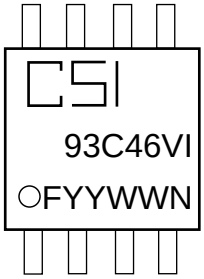
## PACKAGE MARKING

### 8-Lead PDIP



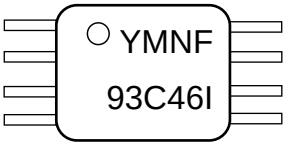

CSI = Catalyst Semiconductor, Inc.
93C46L = Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
N = Product Revision
F = Lead Finish
4 = NiPdAu
3 = MatteTin

### 8-Lead SOIC



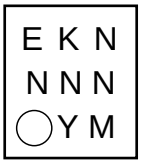

CSI = Catalyst Semiconductor, Inc.
93C46V = Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
N = Product Revision
F = Lead Finish
4 = NiPdAu
3 = MatteTin

### 8-Lead TSSOP




Y = Production Year
M = Production Month
N = Product Revision
93C46 = Device Code
I = Industrial Temperature Range
F = Lead Finish
4 = NiPdAu
3 = MatteTin

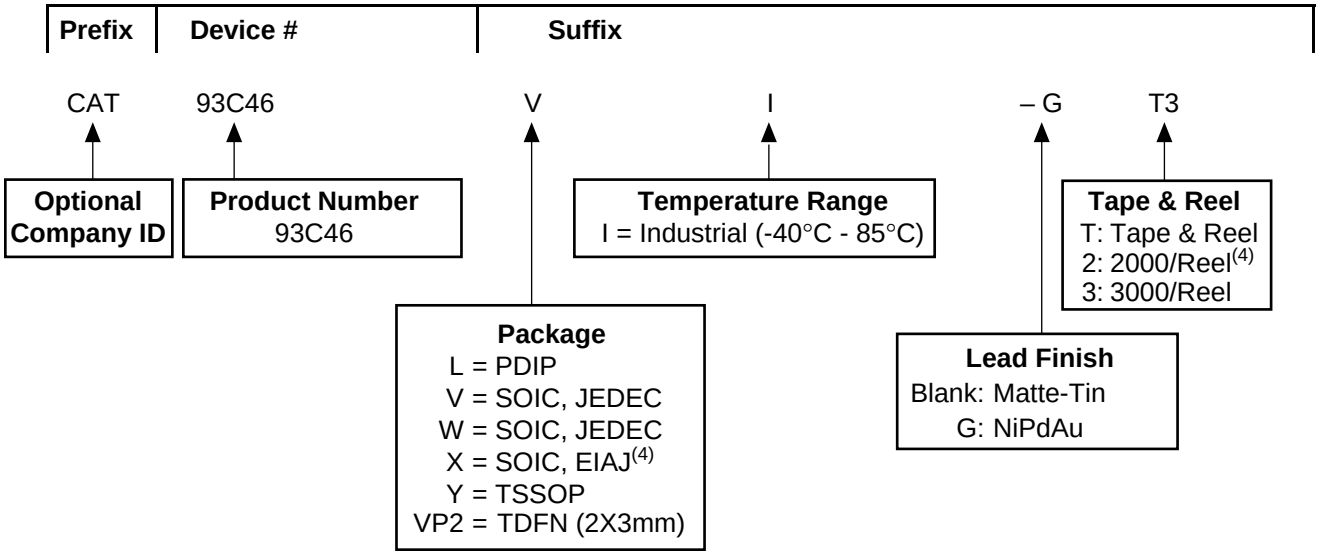
### 8-Lead TDFN




E K = Device Code (NiPdAu)*
EW = Device Code (Matte Tin)*
N = Traceability Code
Y = Production Year
M = Production Month

* The product revision is included in Device Code

## EXAMPLE OF ORDERING INFORMATION




Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu.
(3) The device used in the above example is a CAT93C46VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).
(4) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT93C46XI-T2.
(5) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

## REVISION HISTORY

| Date | Revision | Comments |
|---|---|---|
| 12/01/05 | A | Initial Issue |
| 12/08/05 | B | Update D.C Operating Characteristics |
| 02/22/06 | C | Update Pin Configuration<br>Update A.C. Charateristics<br>Update Package Dimensions<br>Update Ordering Information<br>Update Package Marking |
| 05/24/06 | D | Update Pin Configuration<br>Update Pin Functions<br>Update D.C. Operating Charateristics<br>Update A.C. Charateristics<br>Update Device Operation<br>Update Package Marking<br>Remove Tape and Reel<br>Update Example of Package Information |
| 08/03/06 | E | Update D.C. Operating Charateristics<br>Update Test Condition for Pin Capacitance<br>Update A.C. Test Conditions<br>Update Device Operation<br>Add 8 Lead 208 mil SOIC (X) Package<br>Update Package Marking<br>Update Example of Ordering Information |



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