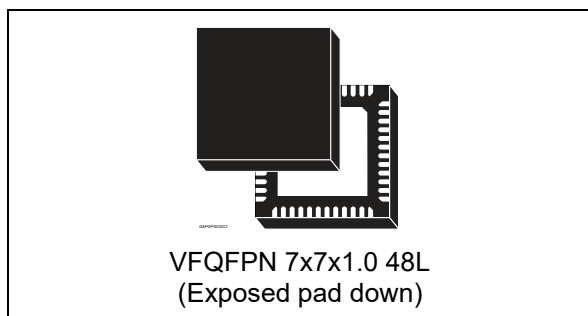


1 channel class D digital input automotive power amplifier with diagnostics, wide voltage operation range for car audio and telematic

Data brief



Features



- AEC-Q100 qualified
- Integrated 108 dB D/A conversion
- I²S and TDM digital input (4/8/16CH TDM)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I²C bus driving (3.3/1.8 V)
- CISPR 25 - Class V (Fourth edition)
- Very low quiescent current
- Output lowpass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range from 3.3 to 18 V, suitable for car radio, telematics and e-call
- MOSFET power outputs allowing high output power capability
 - 1 x 25 W /4 Ω @ 14.4 V, 1 kHz THD = 1%
 - 1 x 31 W /4 Ω @ 14.4 V, 1 kHz THD = 10%

- 2 Ω loads driving
- Amplitude limiter function (configurable through I²C)
- I²C bus diagnostics:
 - Short to V_{CC}/GND
 - Short load and open load detection (also in play mode)
 - Four thermal warnings
- DC offset detector (also in play) and 'hot spot' detection
- Clipping detector
- Integrated thermal protection
- Legacy mode ('no I²C' mode), 4 configurable settings
- Short circuit and ESD integrated protections
- Package: VFQFPN48 exposed pad down

Table 1. Device summary

| Order code | Package | Packing |
|-------------|--------------------|-------------|
| FDA803Q-V0T | VFQFPN48 | Tape & reel |
| FDA803Q-V0Y | (exposed pad down) | Tray |

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1 Description

The FDA803Q is a single bridge class D amplifier, designed in the most advanced BCD technology, intended for any automotive audio application (car radio, telematics and e-call, noise and tone generators, etc).

The FDA803Q integrates a high performance D/A converter together with powerful MOSFET outputs in class D, so it is very compact and powerful, moreover it reaches outstanding efficiency performances (90%).

It has a very wide operating range: it can be operated both with standard car battery levels (5.5-18 V operating, compatible to load dump pulse) and with external step-down generated voltages or emergency battery (since it is compatible to minimum 3.3 V operative).

The feedback loop includes the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion.

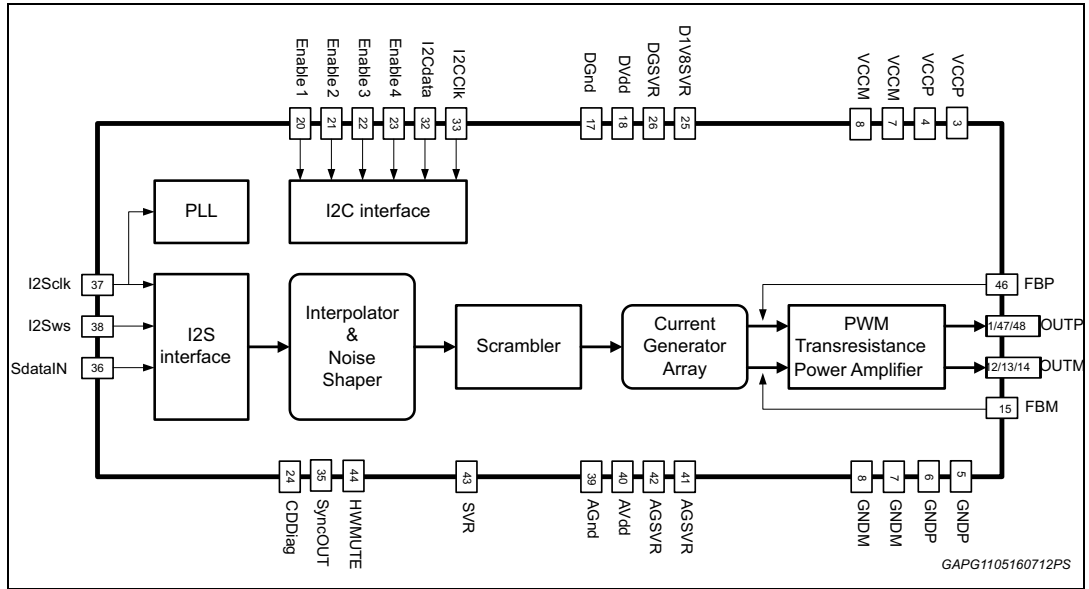
FDA803Q is configurable through I²C bus interface and integrates a complete diagnostics array specially intended for automotive applications including innovative open load and DC offset detection in play mode.

Thanks to the solutions implemented to solve the EMI problems, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover, FDA803Q features a configurable amplitude limiter function, and can be optionally operated under no I²C mode ('legacy mode').

2 Block diagram

Figure 1. Block diagram



3 Pin description

Figure 2. Pin connection diagram (BOTTOM view)

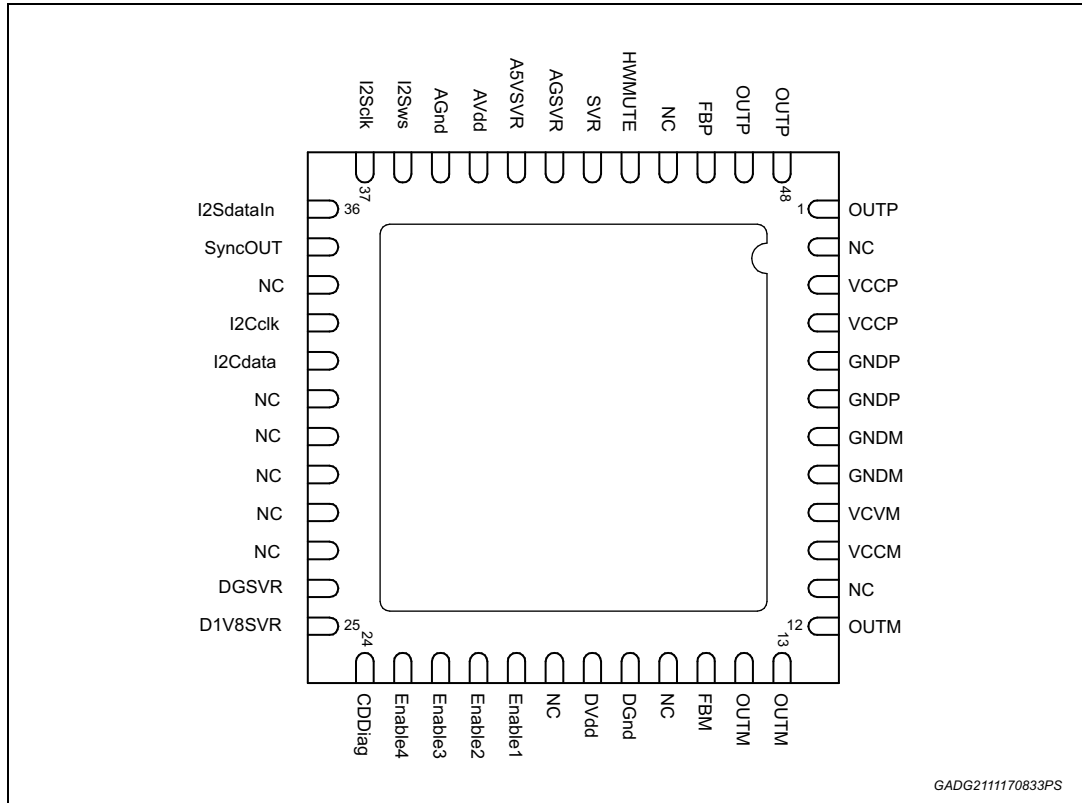


Table 2. Pin list function

| N# | Pin | Function | Definition | Internal structure |
|----|------|---------------------------|------------|--------------------|
| 1 | OUTP | Channel half bridge plus | Output | - |
| 2 | NC | Not connected | - | - |
| 3 | VCCP | Channel half bridge plus | Supply | - |
| 4 | VCCP | Channel half bridge plus | Supply | - |
| 5 | GNDP | Channel half bridge plus | Supply | - |
| 6 | GNDP | Channel half bridge plus | Supply | - |
| 7 | GNDM | Channel half bridge minus | Supply | - |
| 8 | GNDM | Channel half bridge minus | Supply | - |
| 9 | VCCM | Channel half bridge minus | Supply | - |
| 10 | VCCM | Channel half bridge minus | Supply | - |
| 11 | NC | Not connected | - | - |
| 12 | OUTM | Channel half bridge minus | Output | - |
| 13 | OUTM | Channel half bridge minus | Output | - |

Table 2. Pin list function (continued)

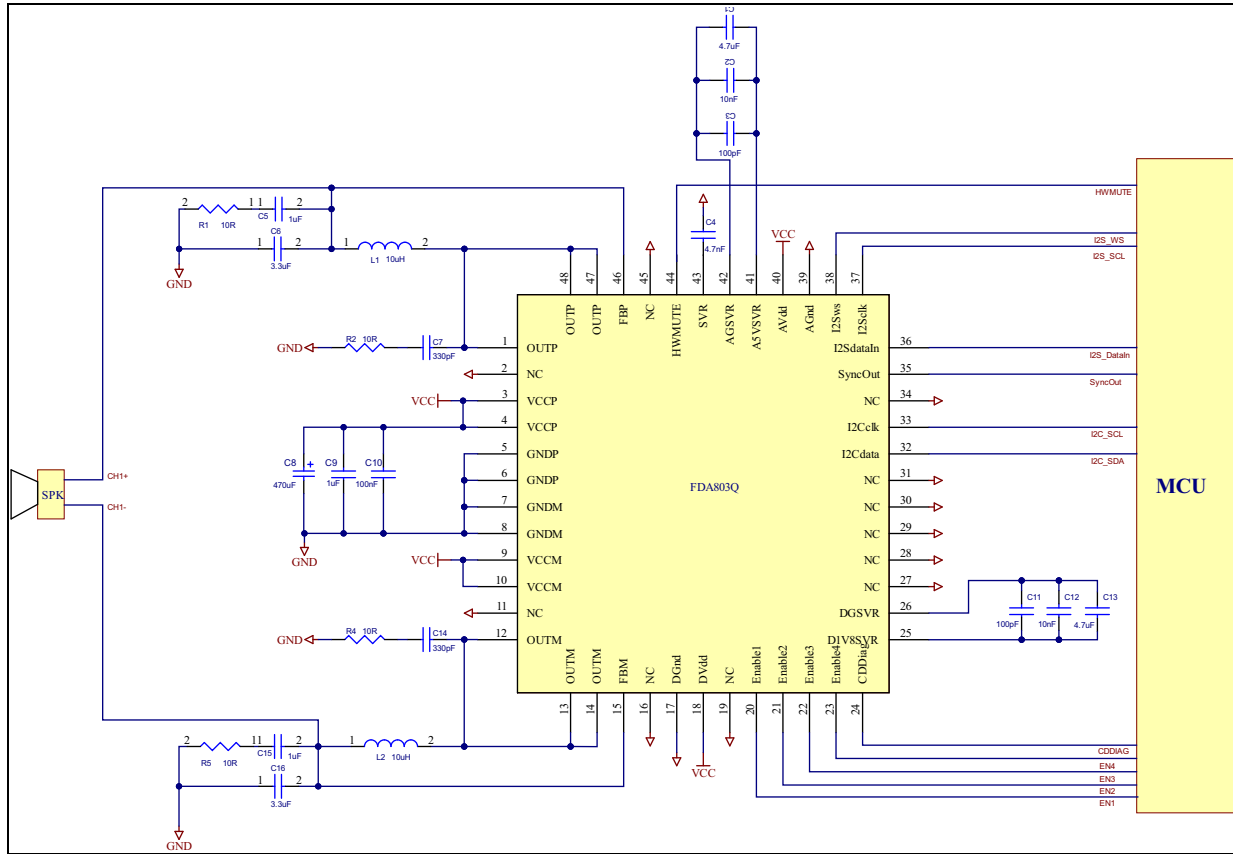
| N# | Pin | Function | Definition | Internal structure |
|----|-----------|--|--------------|---------------------|
| 14 | OUTM | Channel half bridge minus | Output | - |
| 15 | FBM | Channel half bridge minus, Feedback | Input | - |
| 16 | NC | Not connected | - | - |
| 17 | DGnd | Digital ground | Supply | - |
| 18 | DVdd | Digital supply | Supply | - |
| 19 | NC | Not connected | - | - |
| 20 | Enable1 | Enable pin | Input | - |
| 21 | Enable2 | Enable pin | Input | - |
| 22 | Enable3 | Enable pin | Input | - |
| 23 | Enable4 | Enable pin | Input | - |
| 24 | CDDiag | Clipping detector and diagnostic | Output | Open-Drain |
| 25 | D1V8SVR | Positive digital supply V(SVR) + 0.9 V (Internally generated) | Internal | - |
| 26 | DGSVR | Negative digital supply V(SVR) - 0.9 V (Internally generated) | Internal | - |
| 27 | NC | Not connected | - | - |
| 28 | NC | Not connected | - | - |
| 29 | NC | Not connected | - | - |
| 30 | NC | Not connected | - | - |
| 31 | NC | Not connected | - | - |
| 32 | I2Cdata | I ² C Data | Input/Output | Open-Drain |
| 33 | I2Cclk | I ² C Clock | Input | - |
| 34 | NC | Not connected | - | - |
| 35 | SyncOUT | PWM synchronization signal | Output | Pull-Up & Pull-Down |
| 36 | I2SdataIn | I ² S/TDM data | Input | - |
| 37 | I2Sclk | I ² S/TDM Clock | Input | - |
| 38 | I2Sws | I ² S/TDM Sync/Word Select | Input | - |
| 39 | AGnd | Analog ground | Supply | - |
| 40 | AVdd | Analog supply | Supply | - |
| 41 | A5VSVR | Positive Analog Supply V(SVR) + 2.5 V (Internally generated) | Internal | - |
| 42 | AGSVR | Negative Analog Supply V(SVR) - 2.5 V (Internally generated) | Internal | - |
| 43 | SVR | Supply Voltage Ripple Rejection Capacitor | Internal | - |
| 44 | HWMUTE | Hardware mute pin | Input | - |
| 45 | NC | Not connected | - | - |

Table 2. Pin list function (continued)

| N# | Pin | Function | Definition | Internal structure |
|----|------|------------------------------------|------------|--------------------|
| 46 | FBP | Channel half bridge plus, Feedback | Input | - |
| 47 | OUTP | Channel half bridge plus | Output | - |
| 48 | OUTP | Channel half bridge plus | Output | - |

4 Application diagram

Figure 3. Application diagram



5 Electrical specifications

5.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|--------------------|------|
| $V_{CC_{max}}$ [V_{CCP} , V_{CCM} , A_{VDD} , D_{VDD}] | DC supply voltage | -0.3 to 28 | V |
| | Transient supply voltage for $t = 100 \text{ ms}^{(1)}$ | -0.3 to 40 | V |
| GND_{max} [D_{GND} , A_{GND} , $GNDP$, $GNDM$] | Ground pin voltage difference | -0.3 to 0.3 | V |
| $\Delta V_{CC_{max}}$ [$D_{VDD}-A_{VDD}$, $V_{CCP}-D_{VDD}$, $V_{CCP}-A_{VDD}$, $V_{CCM}-D_{VDD}$, $V_{CCM}-A_{VDD}$, $V_{CCP}-V_{CCM}$] | Supply pins voltage difference | -0.3 to 0.3 | V |
| ΔGND_{max} [$A_{GND}-D_{GND}$, $GNDP-A_{GND}$, $GNDP-D_{GND}$, $GNDM-D_{GND}$, $GNDM-A_{GND}$, $GNDP-GNDM$] | Ground pin voltage difference | -0.3 to 0.3 | V |
| V_{I2C} [$I2Cdata$, $I2Cclk$] | I ² C bus pins voltage | -0.3 to 5.5 | V |
| V_{I2S} [$I2SdataIN$, $I2Sclk$, $I2Sws$, $SyncOUT$] | I ² S bus pins voltage and Synchronization pin | -0.3 to 5.5 | V |
| Enable [$Enable1$, $Enable2$, $Enable3$, $Enable4$] | Enables | -0.3 to 5.5 | V |
| V_{mute} [$HWMute$] | Hardware mute | -0.3 to 7 | V |
| V_{CD} [$CDDiag$] | CD/DIAG pins voltage | -0.3 to 5.5 | V |
| I_o | Output current (repetitive $f > 10 \text{ Hz}$) | Internally limited | A |
| T_{amb} | Ambient operating temperature | -40 to 125 | °C |
| T_{stg} , T_j | Storage and junction temperature | -55 to 150 | °C |
| ESDHBM | ESD protection HBM | 2000 | V |
| ESDCDM | ESD protection CDM | 500 | V |

1. $V_{CC} = 35 \text{ V}$ for $t < 400 \text{ ms}$ as per ISO16750-2 load dump with centralized load dump suppression.

5.2 Maximum operating voltage

Table 4. Maximum operating voltage

| Symbol | Parameter | Value | Unit |
|--|---|-------|------|
| $V_{CC_{max}}$ [V_{CCP} , V_{CCM} , A_{VDD} , D_{VDD}] | DC supply voltage | 18 | V |
| V_{I2C} [I2Cdata, I2Cclk] | I ² C bus pins voltage | 3.6 | V |
| V_{I2S} [I2SdataIN, I2Sclk, I2Sws, SyncOUT] | I ² S bus pins voltage and Synchronization pin | 3.6 | V |
| Enable [Enable1, Enable2, Enable3, Enable4] | Enables | 3.6 | V |
| V_{mute} [HWMute] | Hardware mute | 5 | V |
| VCD [CDDiag] | CD/DIAG pins voltage | 3.6 | V |

5.3 Thermal data

Table 5. Thermal data - QFN48 slug-down package

| Symbol | Parameter | Value | Unit |
|---------------------|--|-------|------|
| $R_{th\ j-a-2s2pv}$ | Thermal resistance junction-to-ambient (2s2p+vias) | 28.5 | °C/W |

2s2p is referred to a board with 2 layers dedicated to the signals and 2 layers dedicated to the power signals and supplies.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 VFQFPN (7x7x1.0 48L - opt. D) package information

Figure 4. VFQFPN (7x7x1.0 48L - opt. D) package outline

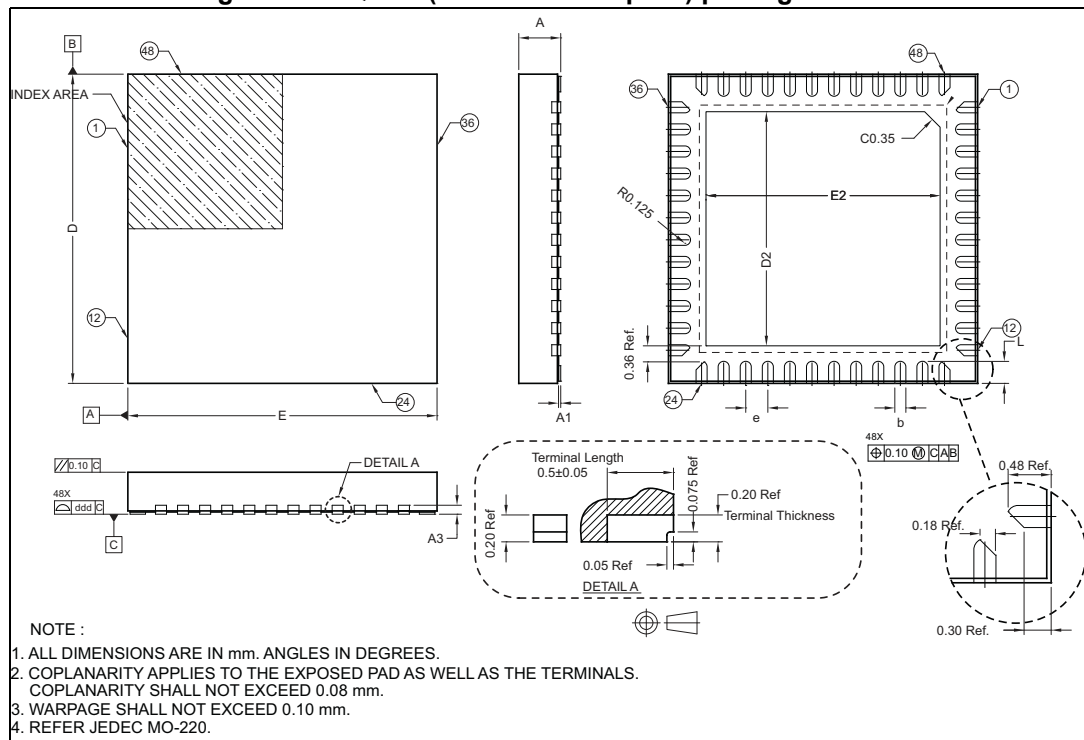


Table 6. VFQFPN (7x7x1.0 48L - opt. D) package mechanical data

| Symbol | Dimensions | | |
|--------|------------|------|------|
| | Min. | Typ. | Max. |
| A | 0.85 | 0.95 | 1.05 |
| A1 | - | 0.00 | 0.05 |
| A2 | - | 0.75 | - |
| A3 | - | 0.20 | - |
| b | 0.15 | 0.25 | 0.35 |
| D | 6.85 | 7.00 | 7.15 |
| D2 | 5.15 | 5.30 | 5.45 |
| E | 6.85 | 7.00 | 7.15 |
| E2 | 5.15 | 5.30 | 5.45 |
| e | 0.45 | 0.50 | 0.55 |
| L | 0.45 | 0.50 | 0.55 |
| ddd | - | - | 0.08 |

7 Revision history

Table 7. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 03-May-2021 | 1 | Initial release. |

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