

## Double channel high side driver

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VND830AEP-E	60m $\Omega$ <sup>(1)</sup>	6A <sup>(1)</sup>	36V

1. Per each channel.

- DC short circuit current: 6A
- CMOS compatible inputs
- Proportional load current sense
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against loss of ground and loss of  $V_{CC}$
- Reverse battery protection<sup>(a)</sup>
- In compliance with the 2002/95/EC european directive



### Description

The VND830AEP-E is a monolithic device made using STMicroelectronics VIPower™ M0-3 Technology. The VND830AEP-E is intended for driving any type of multiple load with one side connected to ground.

The Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device has two channels in high side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current. Built-in thermal shutdown and outputs current limitation protect the chip from over temperature and short circuit. The device automatically turns off in the case where the ground pin becomes disconnected.

a. See [Application schematic on page 16](#)

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VND830AEP-E	VND830AEPTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

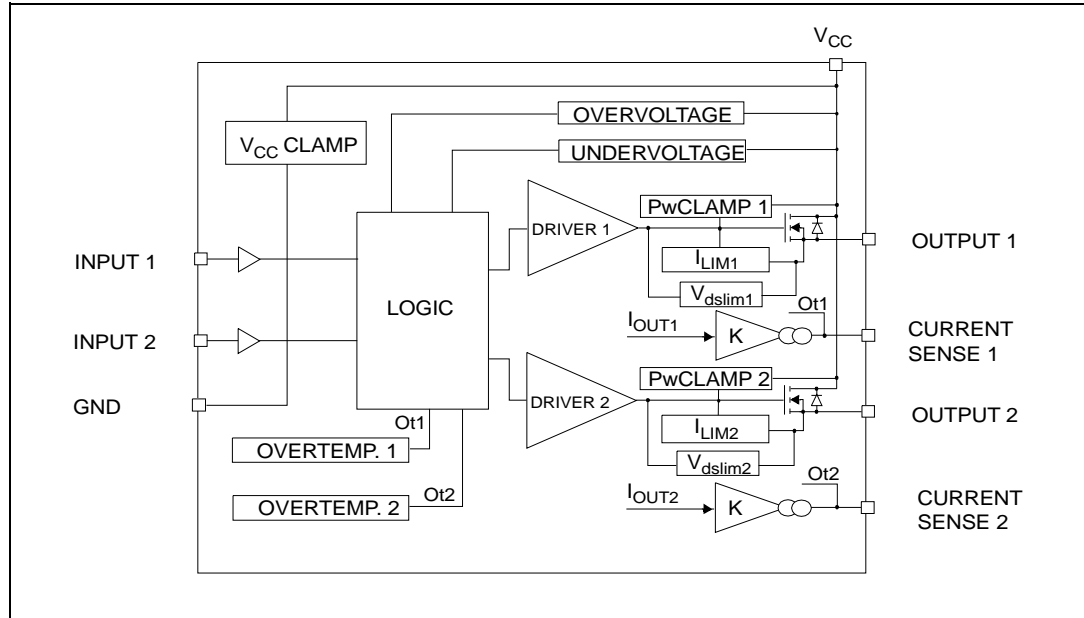


Figure 2. Configuration diagram (top view)

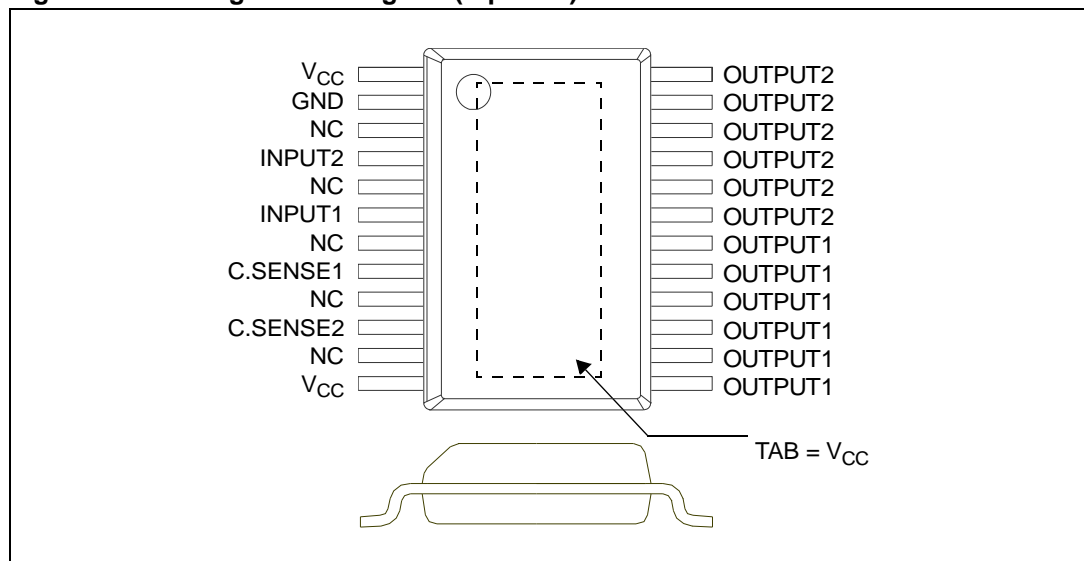


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10KΩ resistor

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$-I_{GND}$	DC reverse ground pin current	- 200	mA
$I_{OUT}$	DC output current	Internally limited	A
$I_R$	Reverse DC output current	- 6	A
$I_{IN}$	DC input current	+/- 10	mA
$V_{CSENSE}$	Current sense maximum voltage	- 3	V
		15	V
$V_{ESD}$	Electrostatic discharge (human body model:R=1.5K $\Omega$ ; C=100pF)		
	– Input	4000	V
	– Current sense	2000	V
	– Output	5000	V
	– $V_{CC}$	5000	V
$E_{MAX}$	Maximum switching energy (L = 2.2mH; $R_L = 0\Omega$ ; $V_{bat} = 13.5V$ ; $T_{jstart} = 150^\circ C$ ; $I_L = 10A$ )	153	mJ
$P_{tot}$	Power dissipation (per island) at $T_{lead} = 25^\circ C$	8.3	W
$T_j$	Junction operating temperature	Internally limited	$^\circ C$
$T_c$	Case operating temperature	- 40 to 150	$^\circ C$
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ C$

### 2.2 Thermal data

**Table 4. Thermal data (per island)**

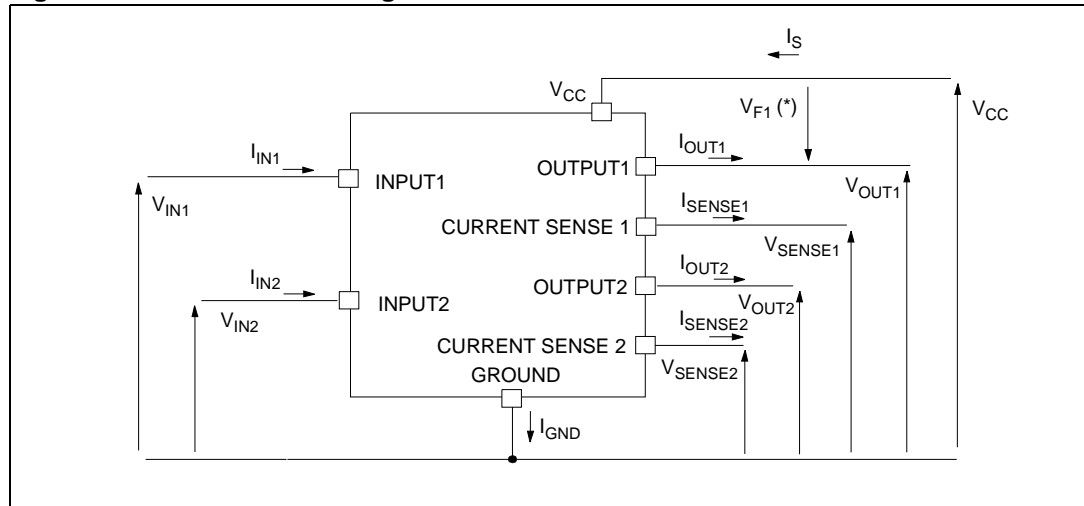
Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.7	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON)	55 <sup>(1)</sup>	$^\circ C/W$

- When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35  $\mu m$  thick) connected to all Vcc pins. Horizontal mounting and no artificial air flow.

### 2.3 Electrical characteristics

Values specified in this section are for  $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise stated.

**Figure 3. Current and voltage conventions**



Note:  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.

**Table 5. Power output**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 2A$ ; $T_j = 25^{\circ}C$ $I_{OUT} = 2A$ ; $T_j = 125^{\circ}C$			60 120	mΩ
$V_{CLAMP}$	Clamp voltage	$I_{CC} = 20mA$	41	48	55	V
$I_S$	Supply current	Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$		12	40	μA
		Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$ ; $T_j = 25^{\circ}C$		12	25	μA
		On-state; $V_{CC} = 13V$ ; $V_{IN} = 5V$ ; $I_{OUT} = 0A$ ; $R_{SENSE} = 3.9K\Omega$				7
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 36V$ ; $T_j = 125^{\circ}C$	0		50	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$			3	μA

**Table 6. Protections**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{lim}$	Current limitation	$V_{CC} = 13V$ $5.5V < V_{CC} < 36V$	6	10	15 15	A A
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		135			°C
$T_{hyst}$	Thermal hysteresis		7	15		°C
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2A; V_{IN} = 0V;$ $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 10mA$		50		mV

*Note:* To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 7.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT} = 1.3A; T_j = 150°C$			0.6	V

**Table 8. Switching ( $V_{CC} = 13V; T_j = 25°C$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ from $V_{IN}$ rising edge to $V_{OUT} = 1.3V$ (see <a href="#">Figure 5</a> )		30		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ from $V_{IN}$ falling edge to $V_{OUT} = 11.7V$ (see <a href="#">Figure 5</a> )		30		$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 1.3V$ to $V_{OUT} = 10.4V$ (see <a href="#">Figure 5</a> )		See <a href="#">Figure 10</a>		$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 11.7V$ to $V_{OUT} = 1.3V$ (see <a href="#">Figure 5</a> )		See <a href="#">Figure 12</a>		$V/\mu s$

**Table 9. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25V$	1			$\mu A$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25V$			10	$\mu A$



**Table 9. Logic inputs (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{mA}$ $I_{IN} = -1\text{mA}$	6	6.8 - 0.7	8	V V

**Table 10. Current sense**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_0$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2} = 0.05\text{A}$ ; $V_{SENSE} = 0.5\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	600	1300	2000	
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2} = 0.25\text{A}$ ; $V_{SENSE} = 0.5\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	1000	1400	1900	
$dK_1/K_1$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2} = 0.25\text{A}$ ; $V_{SENSE} = 0.5\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	-10		+10	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2} = 1.6\text{A}$ ; $V_{SENSE} = 4\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}$ $T_j = 25^\circ\text{C}...150^\circ\text{C}$	1280 1300	1500 1500	1800 1780	
$dK_2/K_2$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2} = 1.6\text{A}$ ; $V_{SENSE} = 4\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	-6		+6	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2} = 2.5\text{A}$ ; $V_{SENSE} = 4\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}$ $T_j = 25^\circ\text{C}...150^\circ\text{C}$	1280 1340	1500 1500	1680 1600	
$dK_3/K_3$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2} = 2.5\text{A}$ ; $V_{SENSE} = 4\text{V}$ ; other channels open; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	-6		+6	%
$I_{SENSE}$	Analog sense leakage current	$V_{IN} = 0\text{V}$ ; $I_{OUT} = 0\text{A}$ ; $V_{SENSE} = 0\text{V}$ ; $T_j = -40^\circ\text{C}...150^\circ\text{C}$ $V_{IN} = 5\text{V}$ ; $I_{OUT} = 0\text{A}$ ; $V_{SENSE} = 0\text{V}$ ; $T_j = -40^\circ\text{C}...150^\circ\text{C}$	0 0		5 10	$\mu\text{A}$ $\mu\text{A}$
$V_{SENSE}$	Max. analog sense output voltage	$V_{CC} = 5.5\text{V}$ ; $I_{OUT1,2} = 1.3\text{A}$ ; $R_{SENSE} = 10\text{k}\Omega$ $V_{CC} > 8\text{V}$ ; $I_{OUT1,2} = 2.5\text{A}$ ; $R_{SENSE} = 10\text{k}\Omega$	2 4			V V
$V_{SENSEH}$	Sense voltage in over temperature conditions	$V_{CC} = 13\text{V}$ ; $R_{SENSE} = 3.9\text{k}\Omega$		5.5		V

**Table 10. Current sense (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{VSENSEH}$	Analog sense output impedance in over temperature condition	$V_{CC} = 13V$ ; $T_j > T_{TSD}$ ; All channels open		400		$\Omega$
$t_{DSENSE}$	Current sense delay response	To 90% $I_{SENSE}^{(1)}$			500	$\mu s$

1. Current sense signal delay after positive input slope.

**Figure 4.  $I_{OUT}/I_{SENSE}$  versus  $I_{OUT}$**

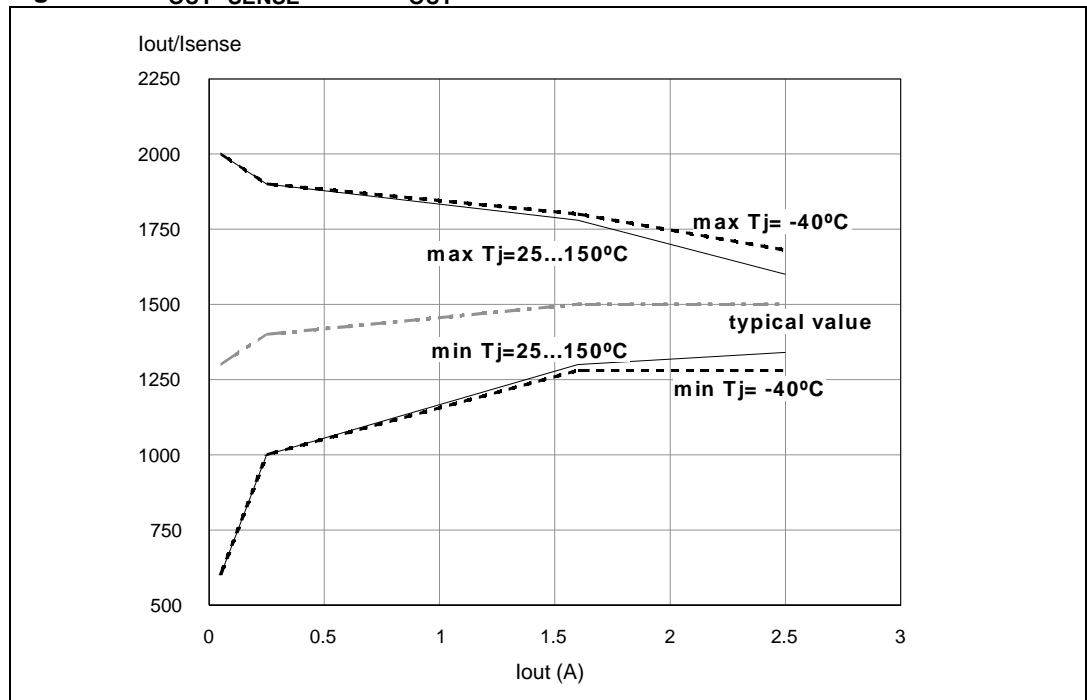


Figure 5. Switching characteristics

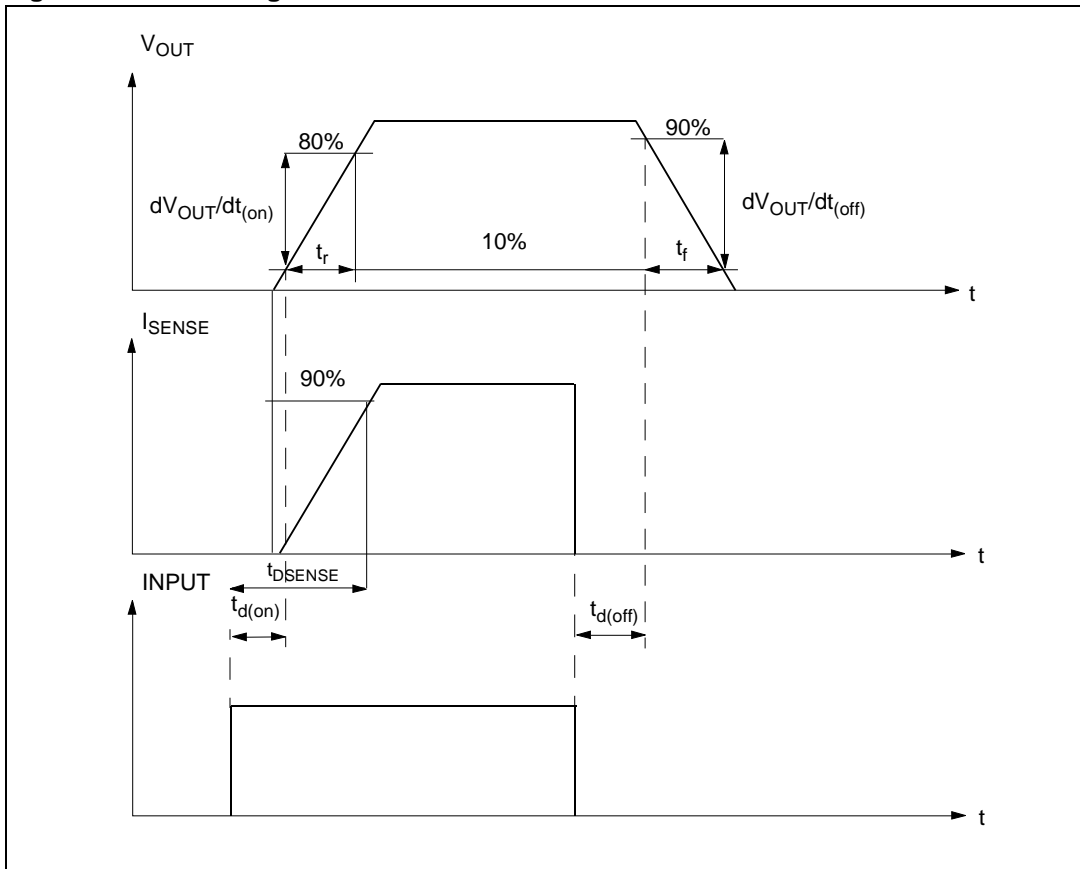


Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_J < T_{TSD})$ 0 $(T_J > T_{TSD})$ 0
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

**Table 12. Electrical transient requirements (part 1/3)**

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1μs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1μs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

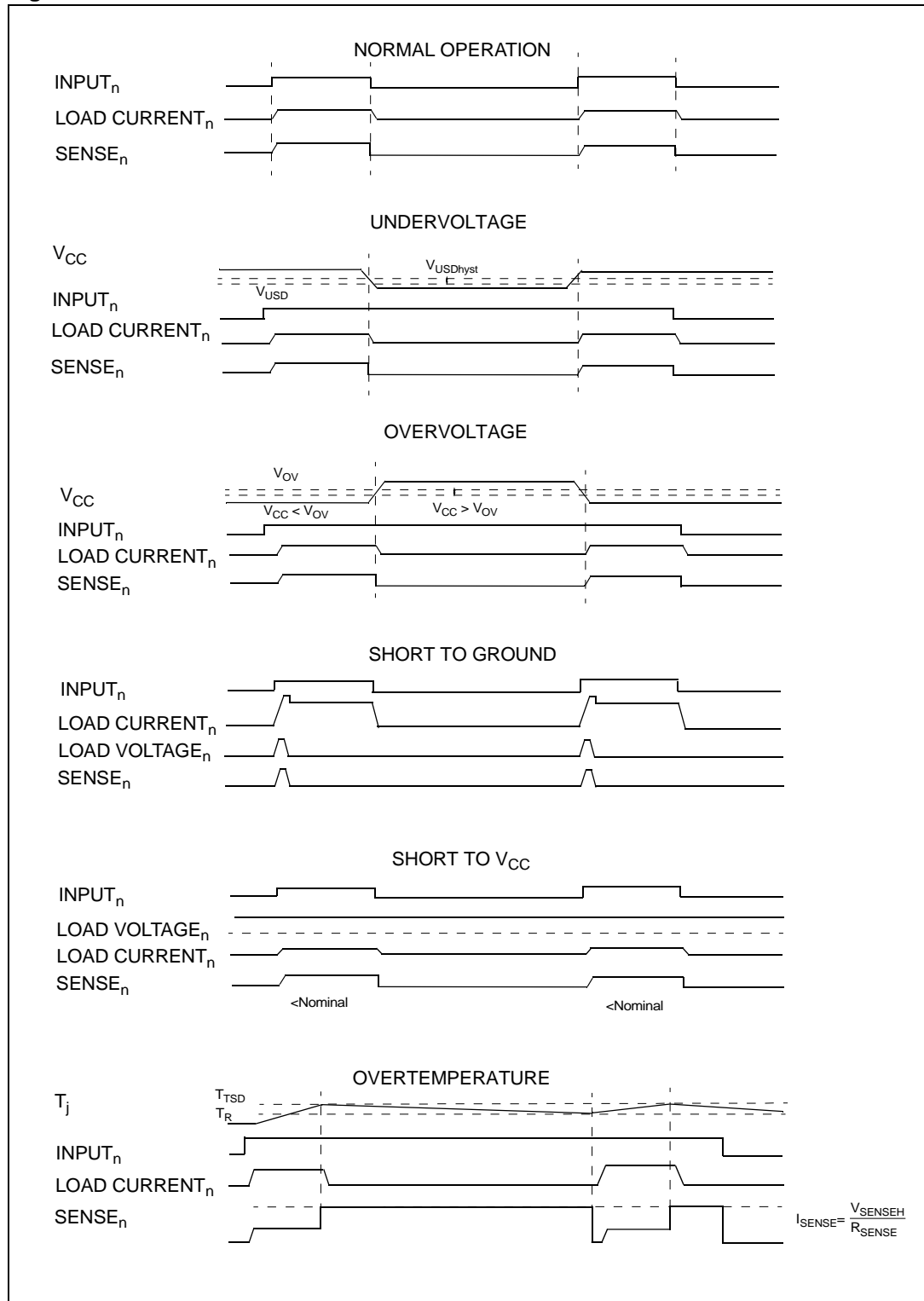
**Table 13. Electrical transient requirements (part 2/3)**

ISO T/R 7637/1 Test pulse	Test level			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

**Table 14. Electrical transient requirements (part 3/3)**

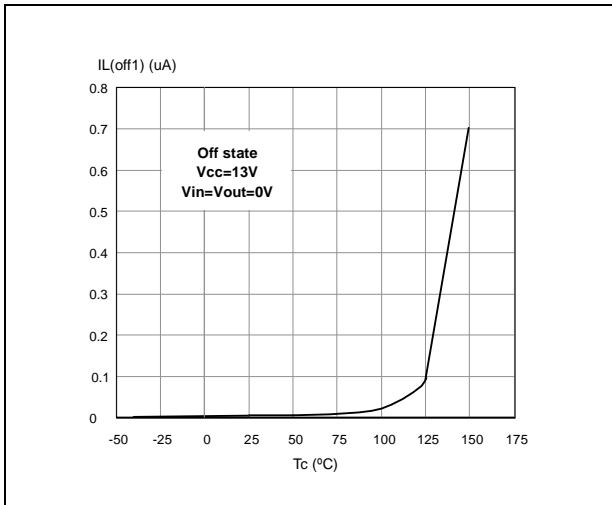
Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms

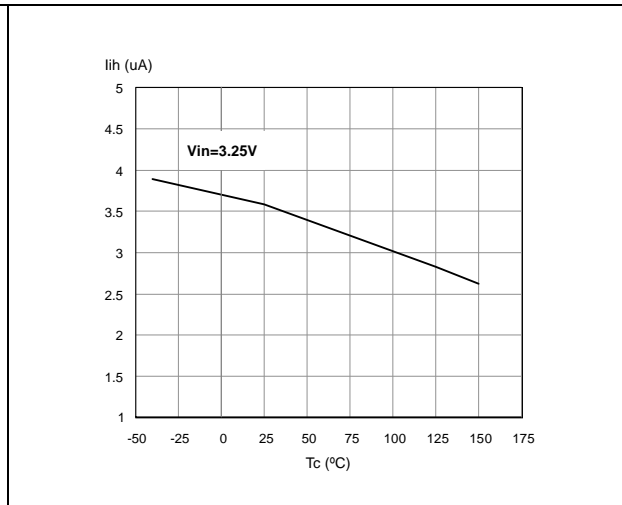


## 2.4 Electrical characteristics curves

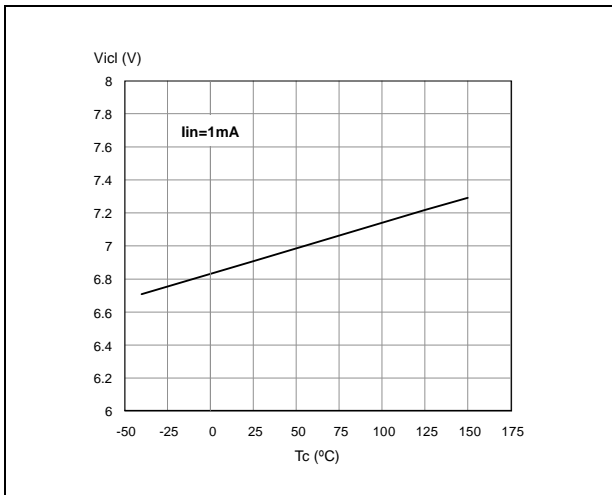
**Figure 7. Off-state output current**



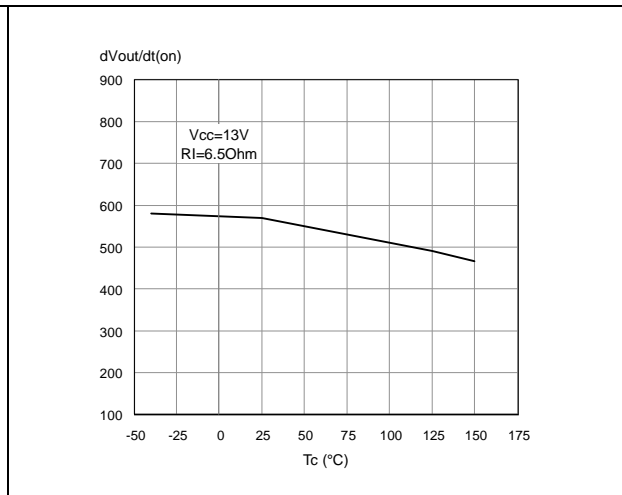
**Figure 8. High level input current**



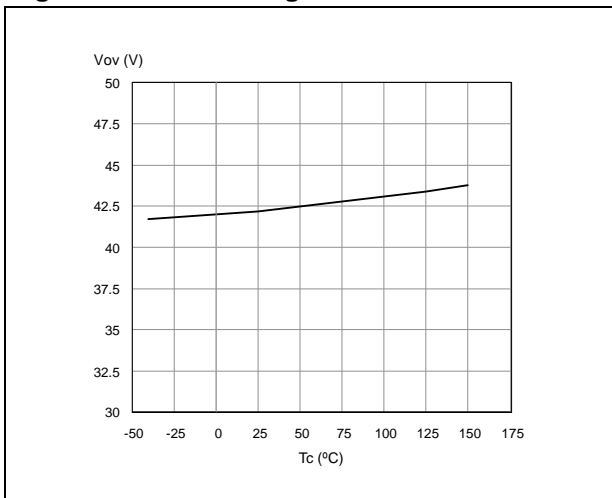
**Figure 9. Input clamp voltage**



**Figure 10. Turn-on voltage slope**



**Figure 11. Overvoltage shutdown**



**Figure 12. Turn-off voltage slope**

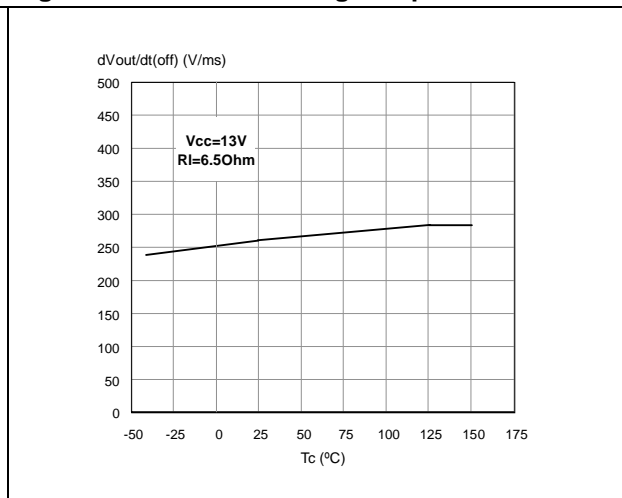


Figure 13.  $I_{LIM}$  vs  $T_{case}$

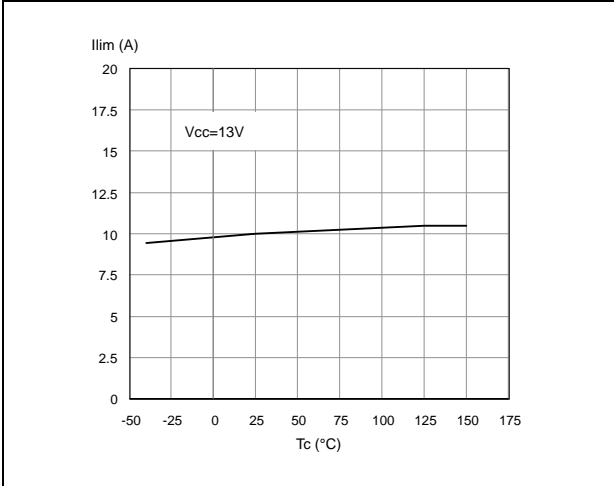


Figure 14. On-state resistance vs  $V_{CC}$

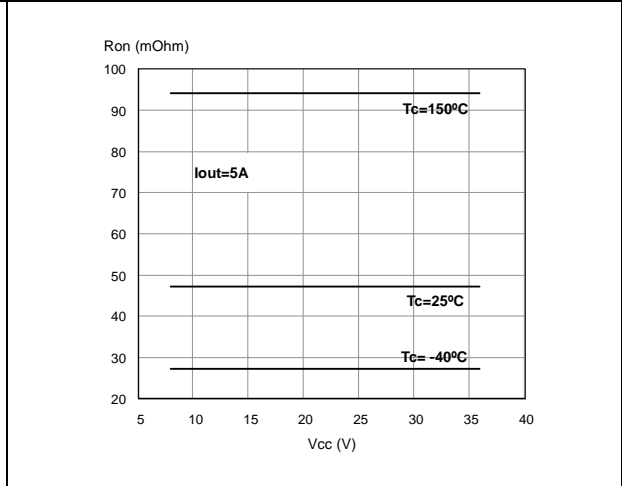


Figure 15. Input high level

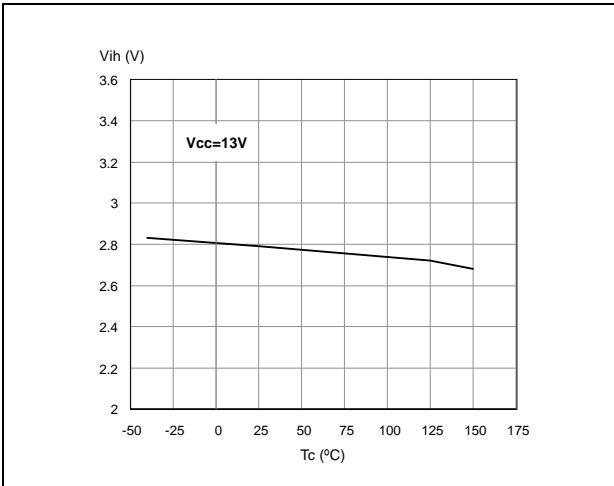


Figure 16. Input hysteresis voltage

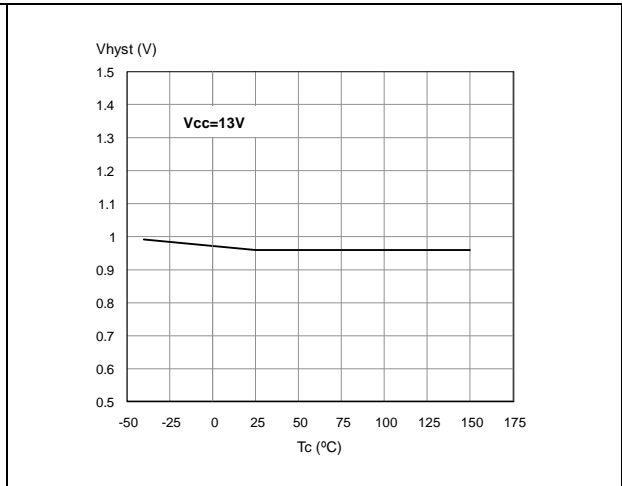


Figure 17. On-state resistance vs  $T_{case}$

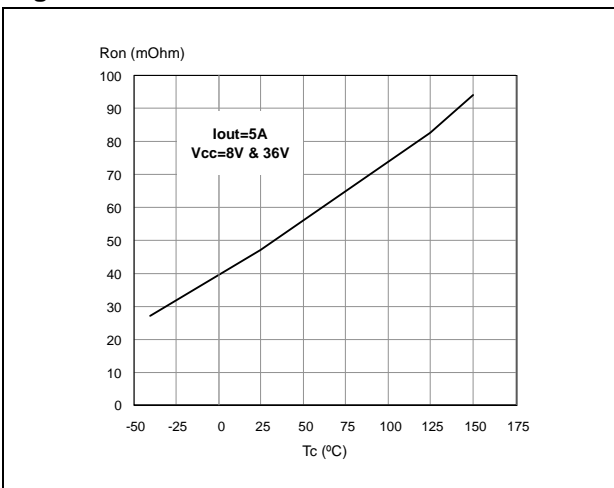
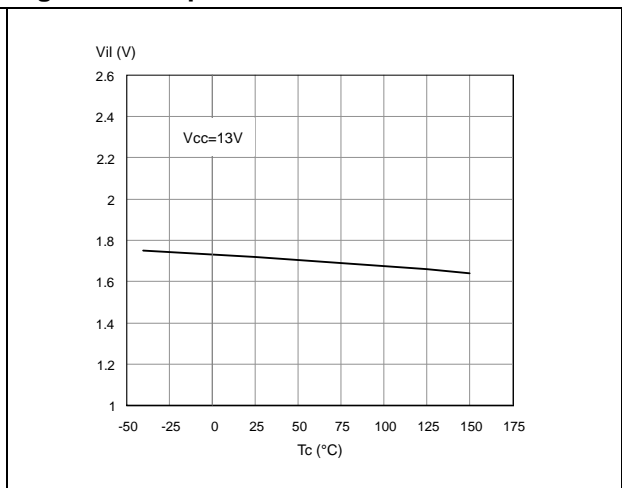
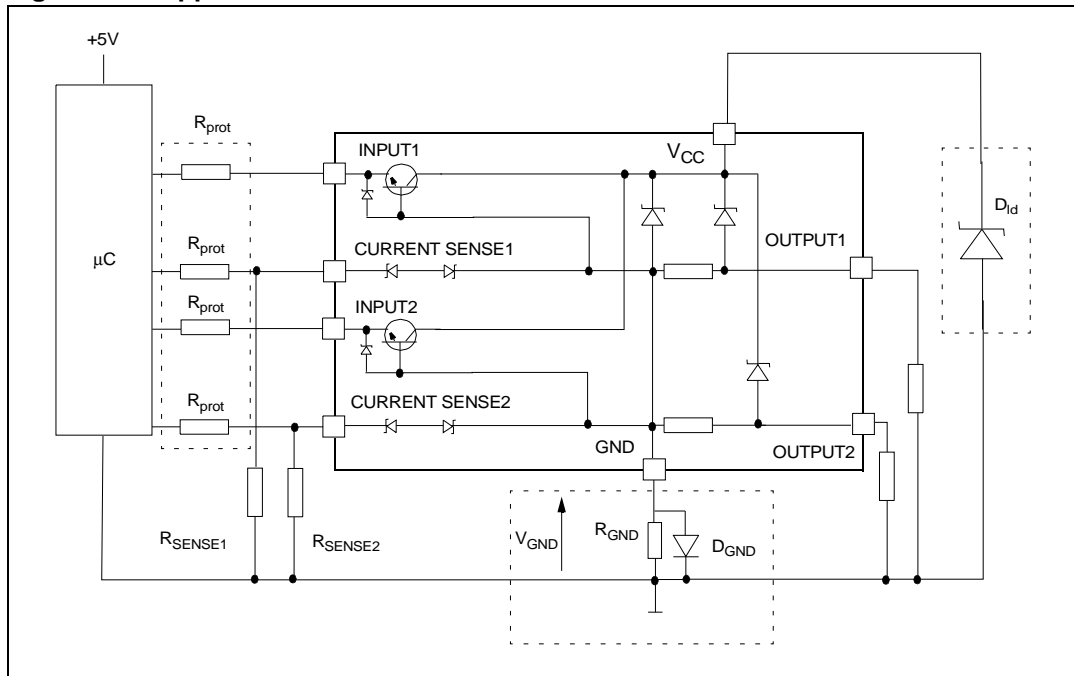


Figure 18. Input low level



### 3 Application information

Figure 19. Application schematic



#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: a resistor in the ground line (R\_GND only)

This can be used with any type of load.

The following show how to dimension the R\_GND resistor:

1.  $R_{GND} \leq 600\text{mV} / 2 (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R\_GND (when  $V_{CC} < 0$  during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R\_GND will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R\_GND.



If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\pm 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than those shown in the ISO T/R 7637/1 table.

## 3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

### Example

For the following conditions:

$$V_{CCpeak} = -100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

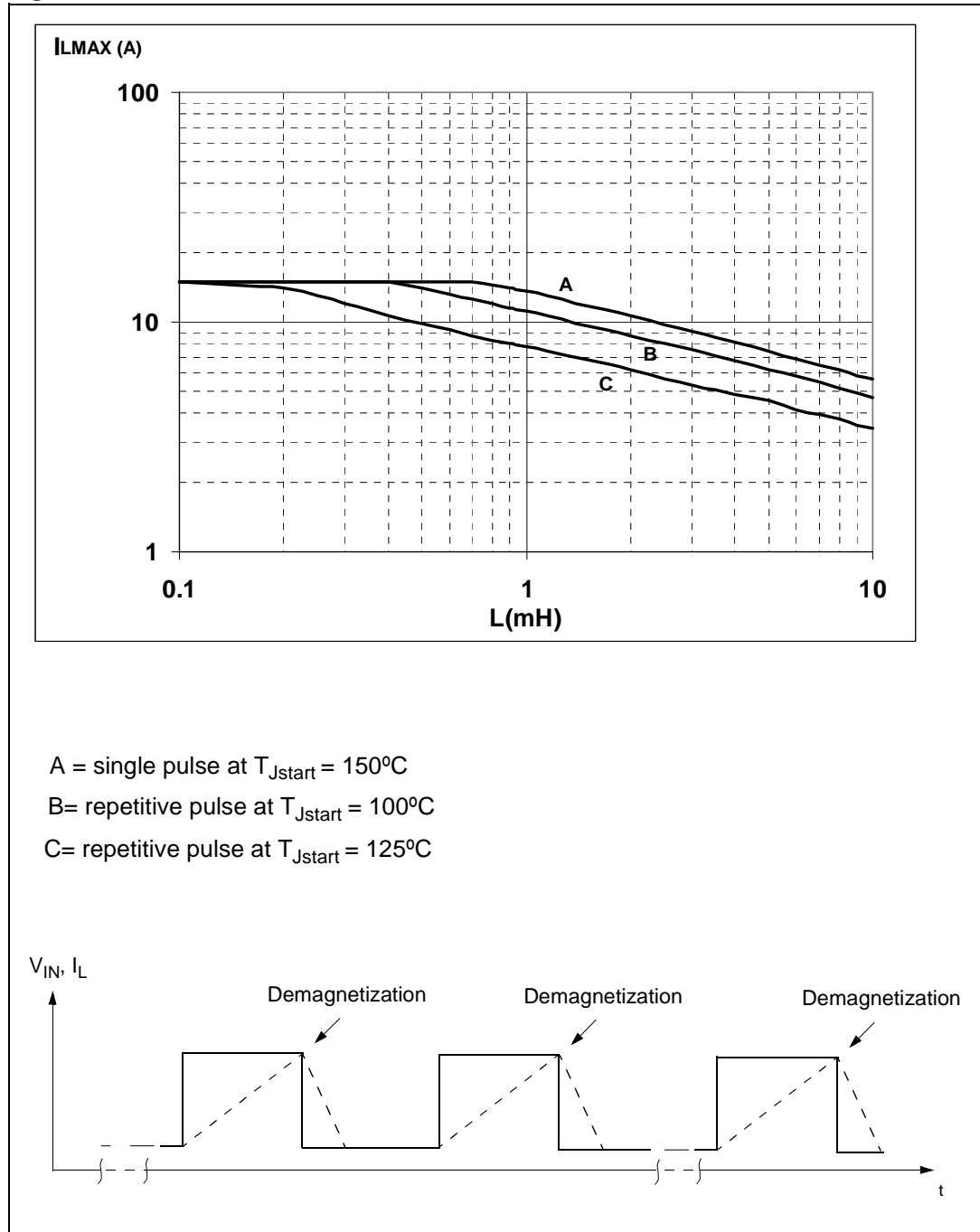
$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 20. Maximum turn-off current versus load inductance

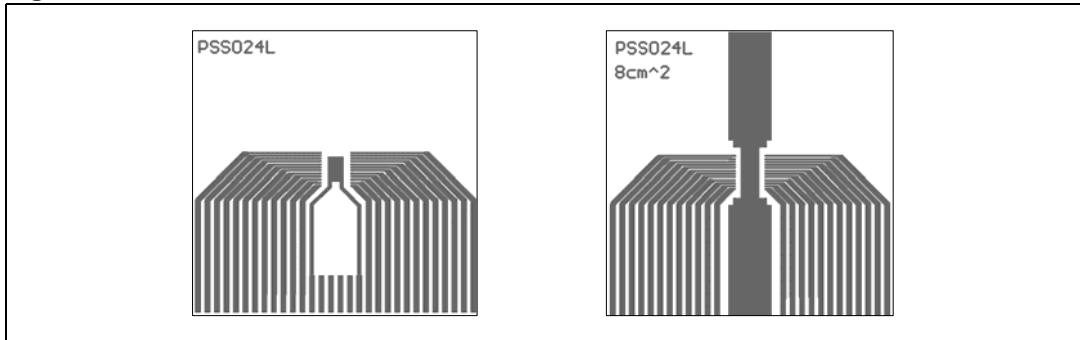


Note: Values are generated with  $R_L = 0\Omega$ .  
 In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

## 4 Package and PC board thermal data

### 4.1 PowerSSO-24 thermal data

Figure 21. PowerSSO-24 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 78 mm x 78 mm, PCB thickness=2 mm, Cu thickness=70 mm (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 22.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel ON)

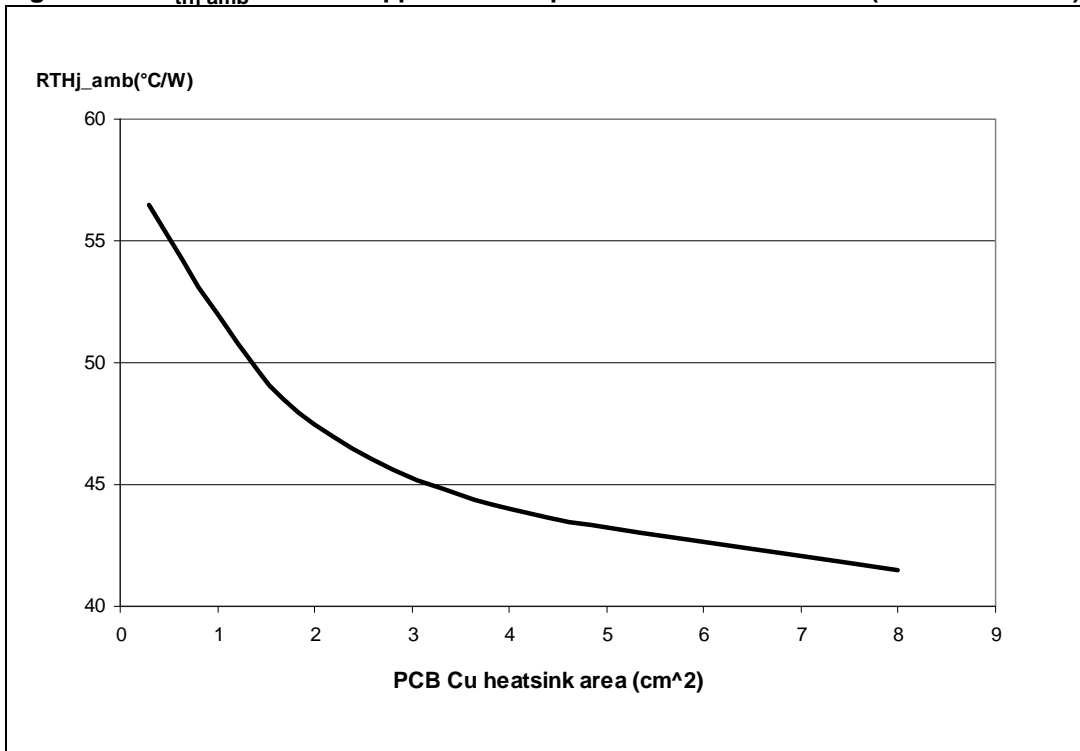


Figure 23. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

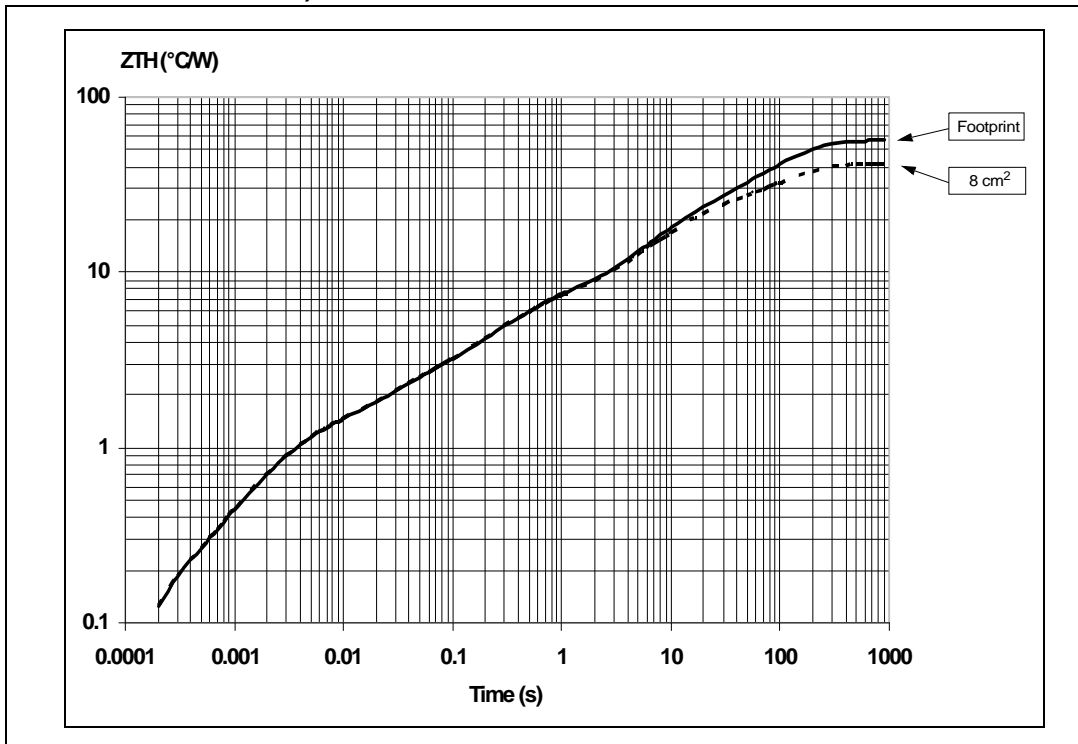
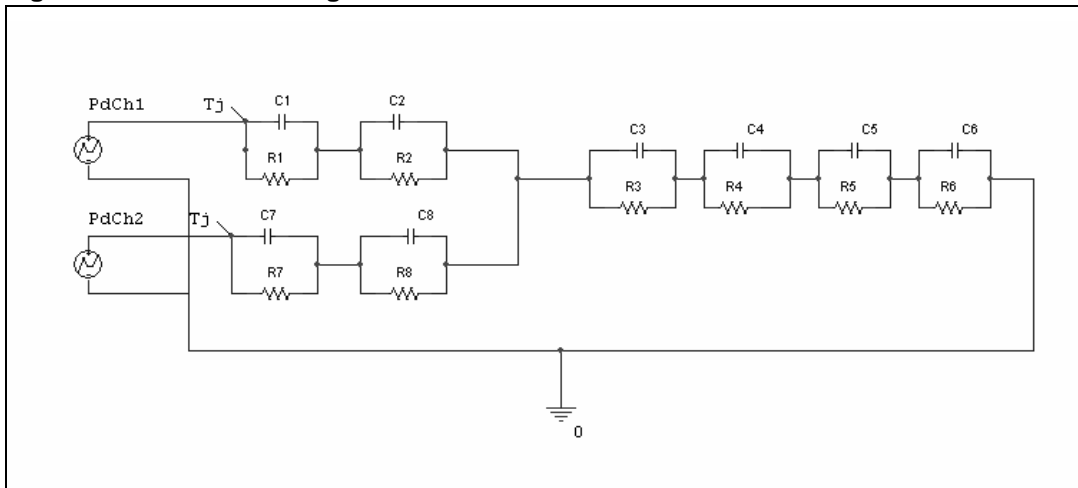


Figure 24. Thermal fitting model of a double channel HSD in PowerSSO-24 (b)



Equation 1: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

- b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	8
R1 = R7 (°C/W)	0.1	
R2 = R8 (°C/W)	0.9	
R3 (°C/W)	1	
R4 (°C/W)	4	
R5 (°C/W)	13.5	
R6 (°C/W)	37	22
C1 = C7 (W.s/°C)	0.0006	
C2 = C8 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.025	
C4 (W.s/°C)	0.08	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 PowerSSO-24 mechanical data

Figure 25. PowerSSO-24 package dimensions

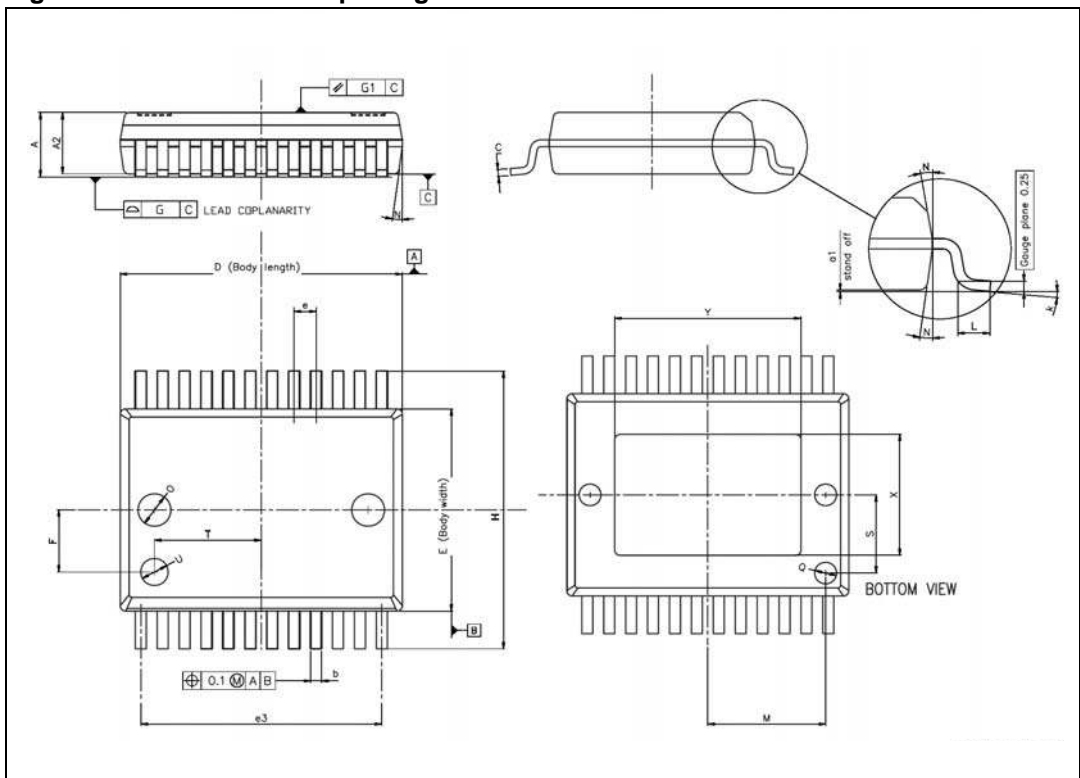


Table 16. PowerSSO-24 mechanical data<sup>(1) (2)</sup>

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D <sup>(3)</sup>	10.10		10.50
E <sup>(3)</sup>	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10°
X	4.1		4.7
Y	6.5 4.9 <sup>(4)</sup>		7.1 5.5 <sup>(4)</sup>

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. "D and E" do not include mold flash or protusions. Mold flash or protusions shall not exceed 0.15 mm.
4. Variations for small window leadframe option.

### 5.3 Packing information

Figure 26. PowerSSO-24 tube shipment (no suffix)

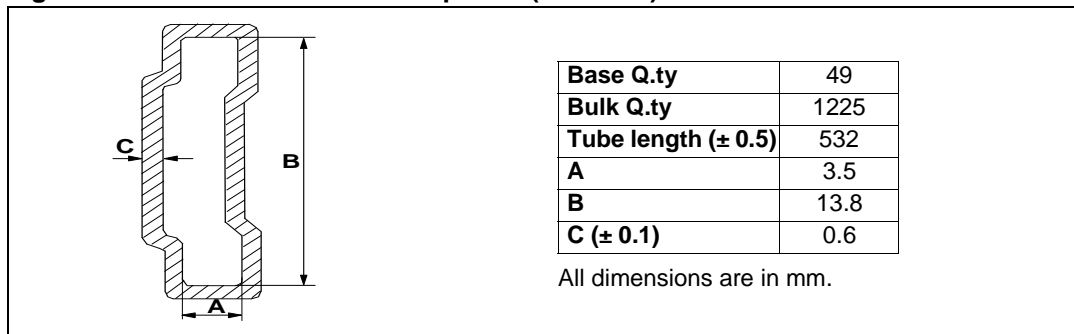
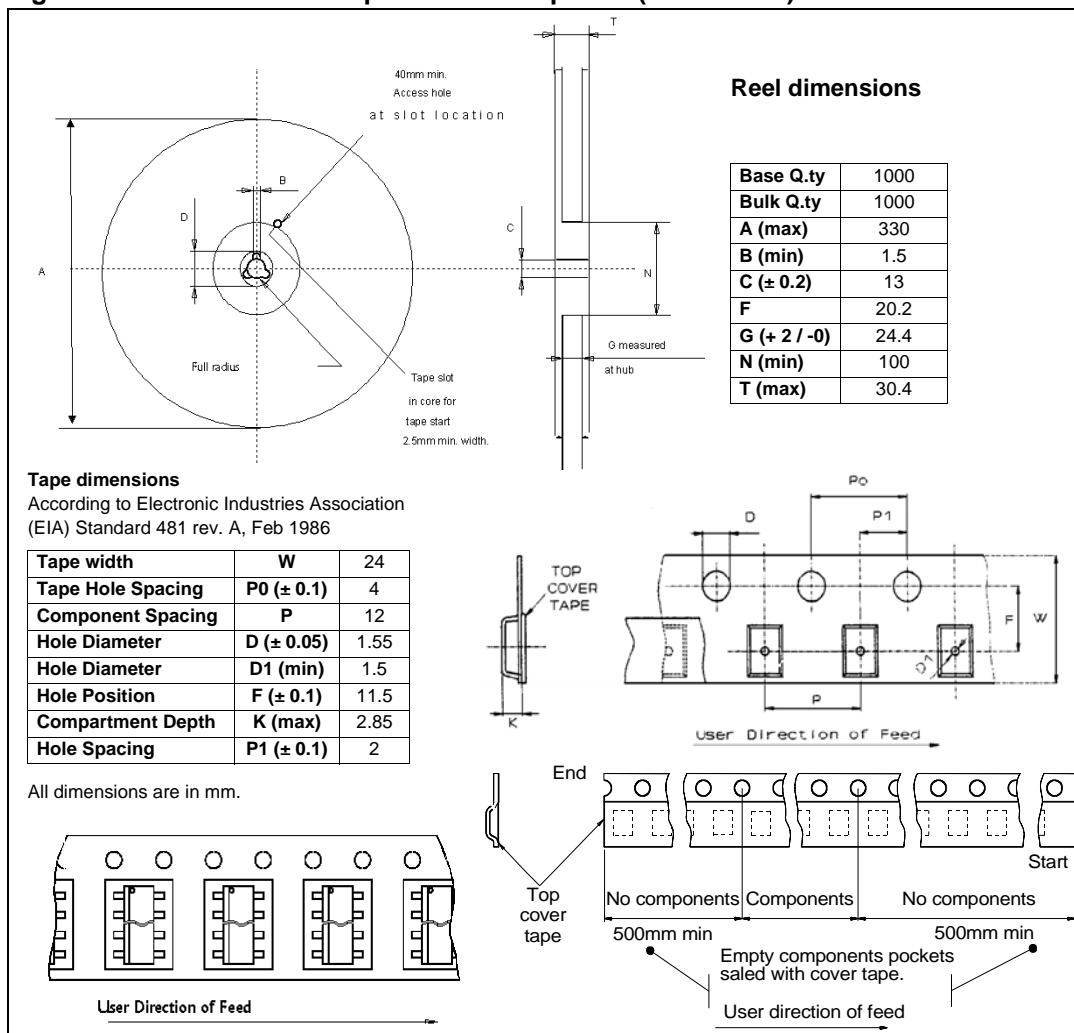


Figure 27. PowerSSO-24 tape and reel shipment (suffix "TR")





## 6 Revision history

Table 17. Document revision history

Date	Revision	Changes
04-Feb-2005	1	Initial release.
27-Nov-2008	2	Document reformatted and restructured. Added list of contents, tables and figures. Added <i>ECOPACK® packages</i> information. Update <i>PowerSSO-24 mechanical data</i> .
01-Jul-2009	3	Updated <i>Figure 16: PowerSSO-24 mechanical data</i> : <ul style="list-style-type: none"><li>– Deleted A (min) value</li><li>– Changed A (max) value from 2.50 to 2.45</li><li>– Changed A2 (max) value from 2.40 to 2.35</li><li>– Updated k values</li><li>– Changed L (min) value from 0.6 to 0.55</li><li>– Changed L (max) value from 1 to 0.85</li></ul>
23-Sep-2013	4	Updated disclaimer.

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