Description

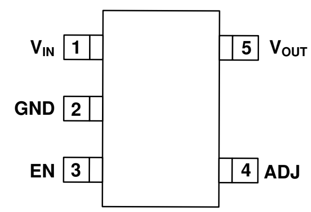
The AP7330 is a low dropout regulator with high output voltage accuracy, low $R_{DS(ON)}$, high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

The AP7330 includes a voltage reference, error amplifier, current limit circuit and an enable input to turn it on and off. With its low power consumption and line and load transient response, the AP7330 is well suited for low power handheld communication equipment.

The AP7330 is packaged in SOT25 package, allows for smallest footprint and dense PCB layout.

Pin Assignments

(Top View)



SOT25

Features

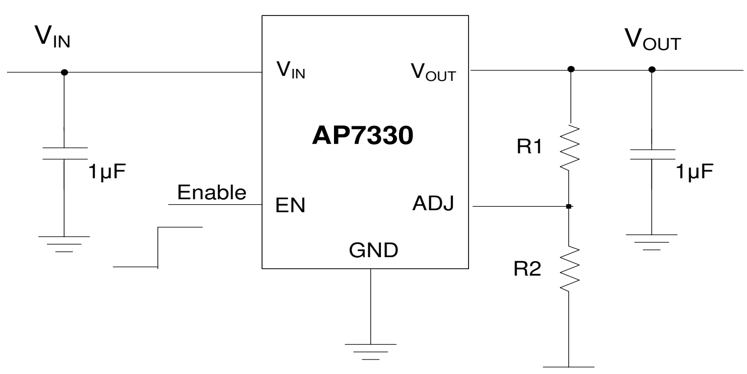
- Low V_{IN} and Wide V_{IN} Range: 1.8V to 5.5V
- Wide V_{OUT} Range: 1.0V to 4.5V
- Guarantee Output Current: 300mA
- V_{OUT} Accuracy ±1%
- Ripple Rejection 80dB at 1kHz
- Low Output Noise, 60µVrms from 10Hz to 100kHz
- Quiescent Current as Low as 45µA
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**

Applications

- Smart Phone/Tablet
- RF Supply
- Cameras
- Portable Video
- Portable Media Player
- Wireless Adapter
- Wireless Communication

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen, Antimony and Beryllium-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl), <1000ppm antimony compounds and <1000ppm Beryllium.

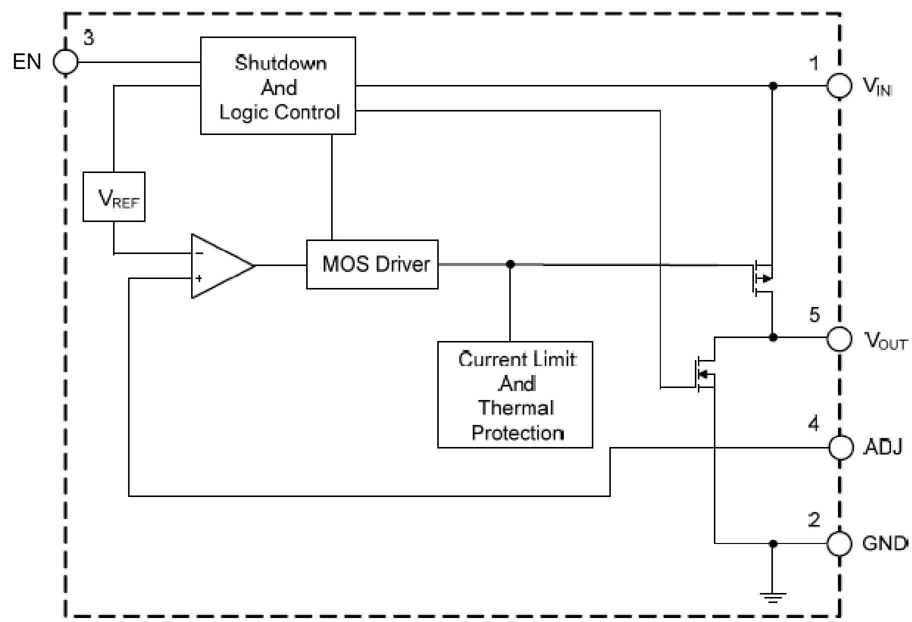
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	V_{IN}	Power Input Pin
2	GND	Ground
3	EN	Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, while pulling it low puts the regulator into shutdown mode
4	ADJ	Output Feedback Pin
5	V_{OUT}	Power Output Pin

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Mode ESD Protection	> 2	kV
ESD MM	Machine Mode ESD Protection	> 200	V
V_{IN}	Input Voltage	6.0	V
V_{EN}	Input Voltage for EN Pin	6.0	V
V_{OUT}	Output Voltage	-0.3 to V_{IN} + 0.3	V
I_{OUT}	Output Current	300	mA
P_D	Power Dissipation	300	mW
T_A	Operating Ambient Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C

Note: 4. a). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.
b). Ratings apply to ambient temperature at +25°C. The JEDEC High-K board design used to derive this data was a 2 inch x 2 inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

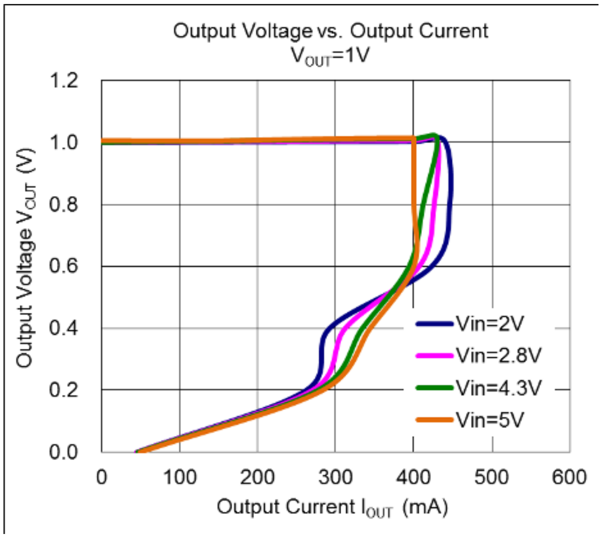
Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.8	5.5	V
V_{OUT}	Output Voltage	1.0	4.5	V
I_{OUT}	Output Current	0	300	mA
T_A	Operating Ambient Temperature	-40	+85	°C

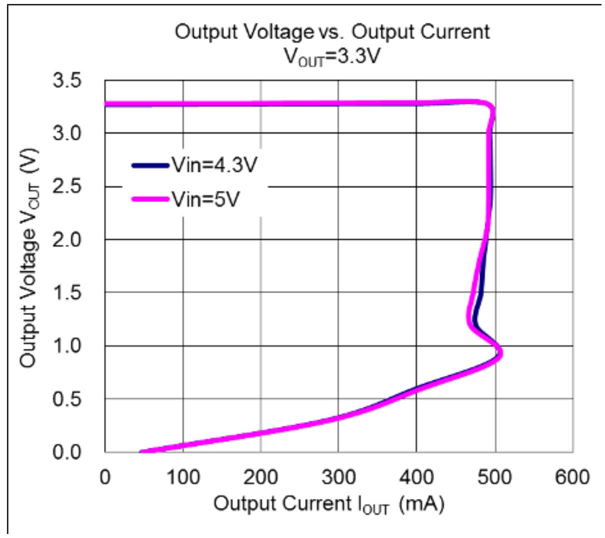
Electrical Characteristics (@T_A = +25°C, V_{IN} = V_{OUT} +1.0V, C_{IN} = C_{OUT} = 1.0µF, I_{OUT} = 1.0mA, unless otherwise specified.)

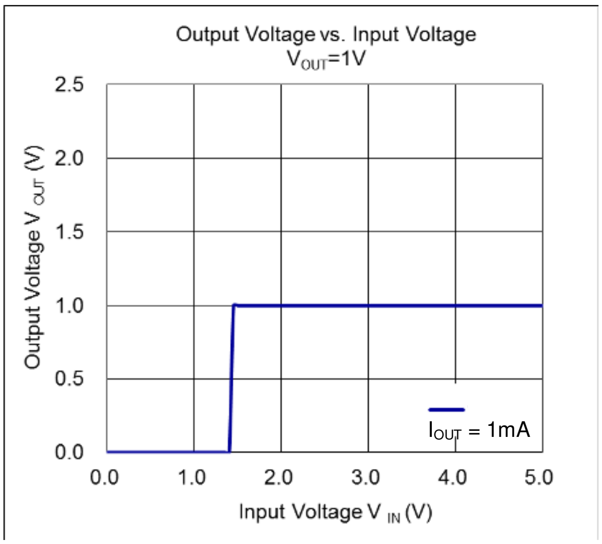
Parameter	Condition		Min	Typ	Max	Unit
Input Voltage	T_A = -40°C to +85°C		1.8	—	5.5	V
Output Voltage Accuracy (Note 11)	V_{IN} = V_{OUT}(T)+1V	T_A = +25°C	V_{OUT}(T)* 0.99	V_{OUT}(T)	V_{OUT}(T)* 1.01	V
ADJ Leakage Current	—		—	0.1	1	µA
V_{ADJ}	Reference Voltage	V_{IN} = V_{OUT} +1V 1mA ≤ I_{OUT} ≤ 300mA	0.792	0.8	0.808	V
Line Regulation ($dV_{OUT}/dV_{IN}/V_{OUT}$)	V_{IN} = ($V_{OUT – Nom}$ +1.0V) to 5.5V, I_{OUT} = 1.0mA		—	0.02	0.1	%/V
Load Regulation	V_{IN} = $V_{OUT - Nom}$ +1.0V, I_{OUT} = 1mA to 300mA		—	15	30	mV
Quiescent Current (Note 6)	I_{OUT} = 0mA		—	45	78	µA
$I_{STANDBY}$	V_{EN} = 0V (Disabled)		—	0.01	1.0	µA
Output Current	—		300	—	—	mA
Fold-back Short Current (Note 7)	V_{OUT} Short to Ground		—	55	—	mA
PSRR (Note 8)	V_{IN} = V_{OUT}+1V, Ripple 0.2Vp-pAC, V_{OUT} = 1.0V to 4.5V, I_{OUT} = 30mA	f = 1kHz	—	80	—	dB
Output Noise Voltage (Note 8) (Note 9)	BW = 10Hz to 100kHz, V_{OUT} = 1.0V, I_{OUT} = 30mA		—	60	—	µVrms
Dropout Voltage (Note 5)	I_{OUT} = 300mA (SOT25)	1.0V ≤ V_{OUT} ≤ 1.2V	—	0.67	0.89	V
		1.2V < V_{OUT} ≤ 1.4V	—	0.57	0.70	
		1.4V < V_{OUT} ≤ 1.7V	—	0.50	0.63	
		1.7V < V_{OUT} ≤ 2.1V	—	0.37	0.50	
		2.1V < V_{OUT} ≤ 2.5V	—	0.32	0.45	
		2.5V < V_{OUT} ≤ 3.0V	—	0.29	0.40	
		3.0V < V_{OUT} ≤ 3.6V	—	0.24	0.33	
		3.6V < V_{OUT} ≤ 4.5V	—	0.22	0.31	
Output Voltage Temperature Coefficient	I_{OUT} = 30mA, T_A = -40°C to +85°C		—	±80	—	ppm/°C
Thermal Shutdown Threshold (TSHDN)	—		—	+150	—	°C
Thermal Shutdown Hysteresis (THYS)	—		—	+20	—	°C
EN Input Low Voltage	—		0	—	0.5	V
EN Input High Voltage	—		1.4	—	5.5	V
EN Input Leakage	V_{EN} = 0, V_{IN} = 5.0V or V_{EN} = 5.0V, V_{IN} = 0V		-1.0	—	+1.0	µA
On Resistance of N-Channel for Auto-Discharge (Note 10)	V_{IN} = 4.0V, V_{EN} = 0V (Disabled)		—	40	—	Ω
Thermal Resistance Junction to Ambient (θ_{JA})	SOT25		—	179	—	°C/W
Thermal Resistance Junction to Case (θ_{JC})	SOT25		—	52	—	

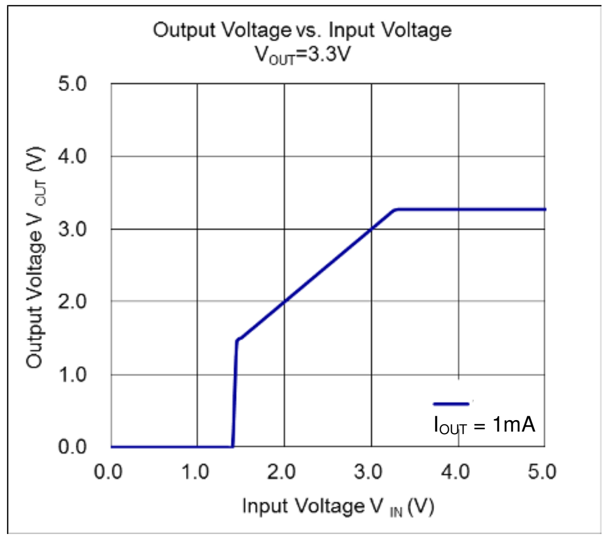
Notes:
5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
6. Quiescent current is defined here is the difference in current between the input and the output.
7. Short circuit current is measured with V_{OUT} pulled to GND.
8. This specification is guaranteed by design.
9. To make sure lowest environment noise minimizes the influence on noise measurement.
10. AP7330 has 2 options for output, built-in discharge and non-discharge.
11. Potential multiple grades based on following output voltage accuracy.

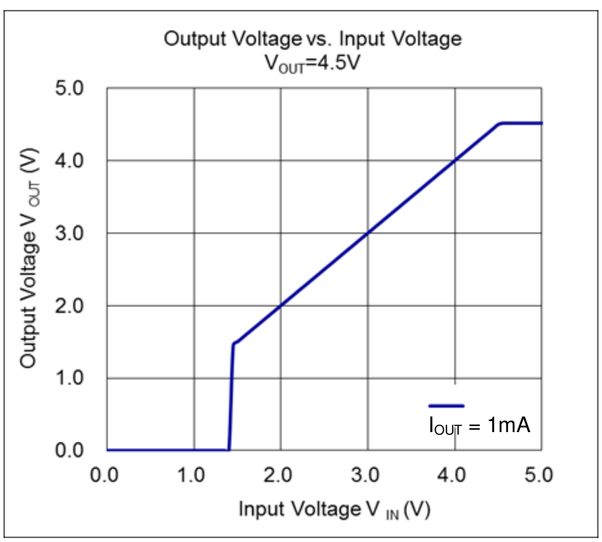
Typical Characteristics

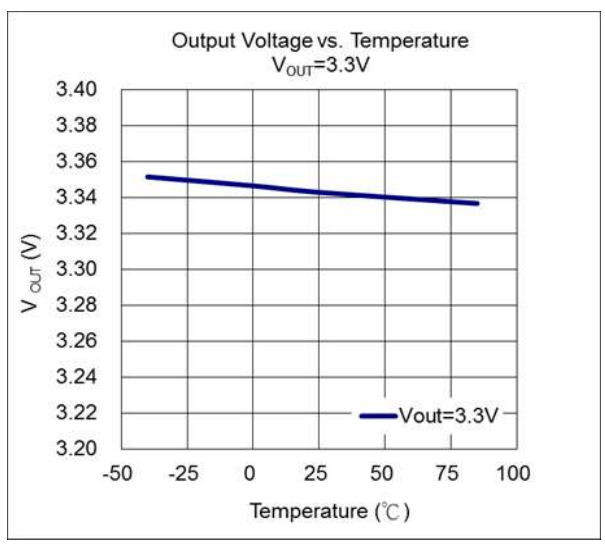




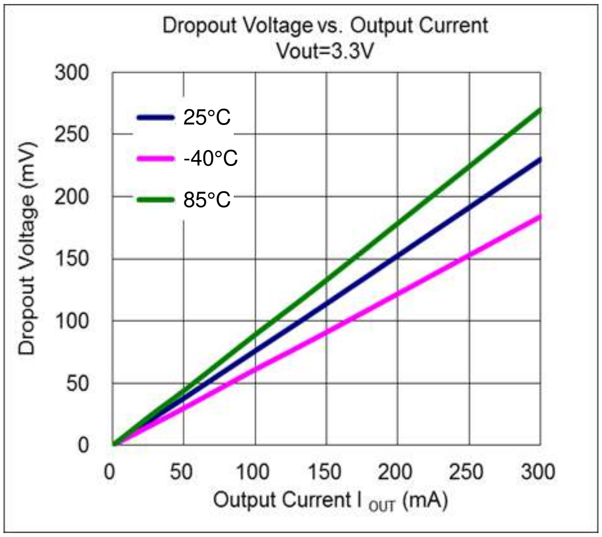


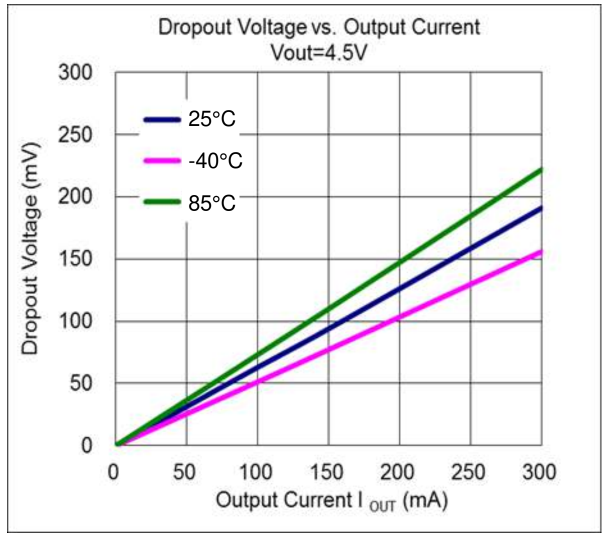


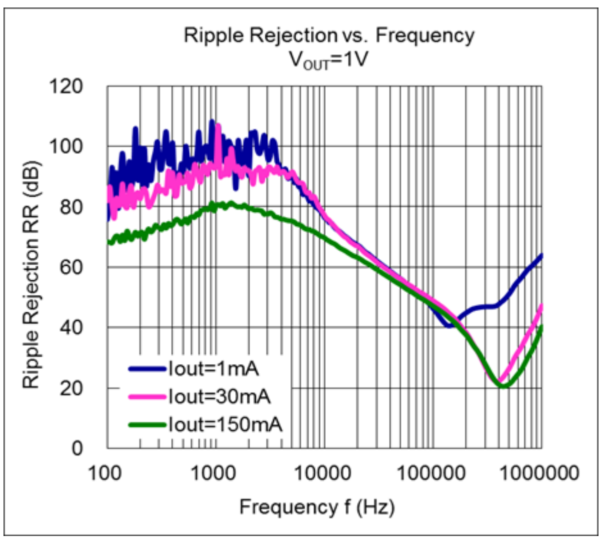


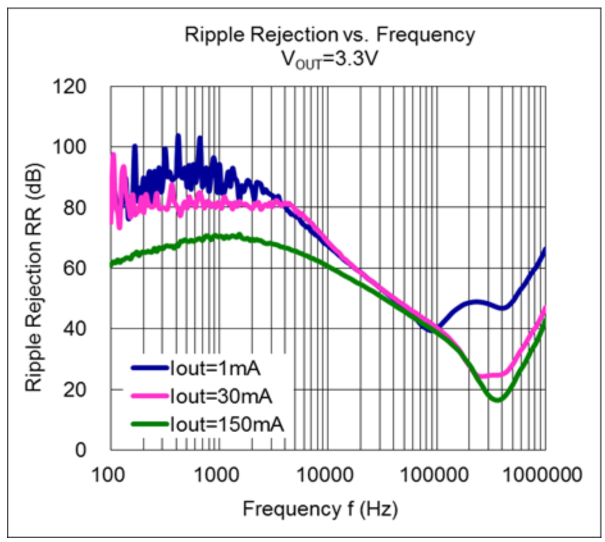


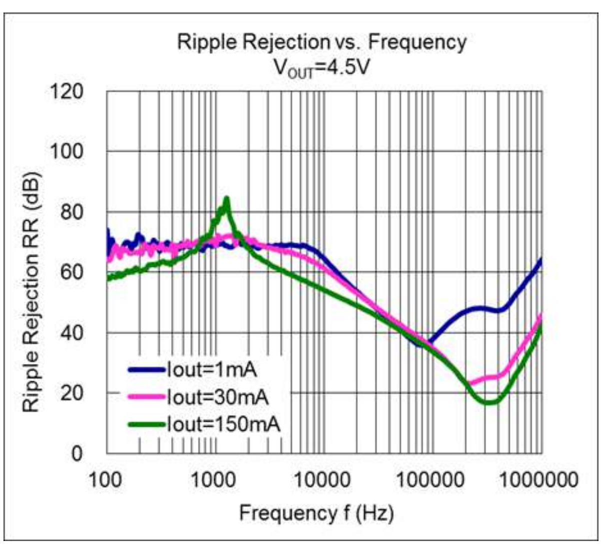
Typical Characteristics (Cont.)



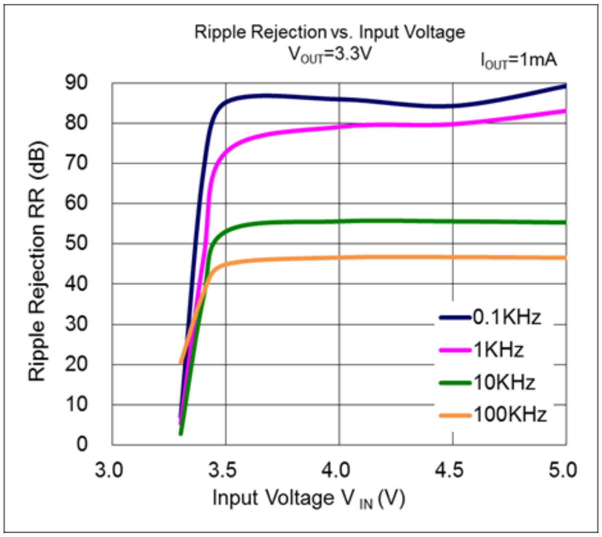


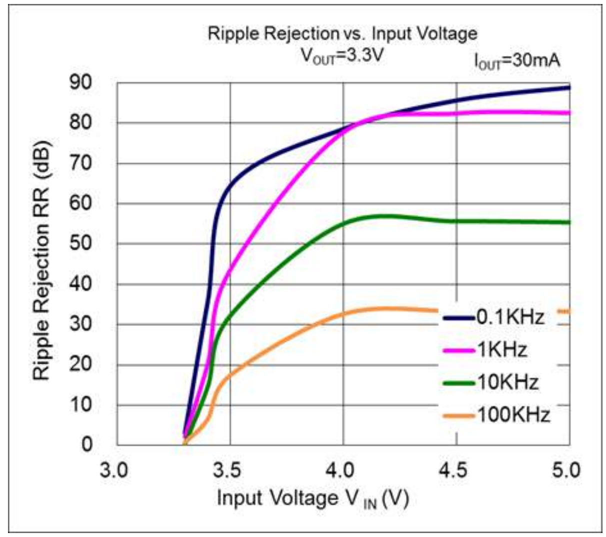




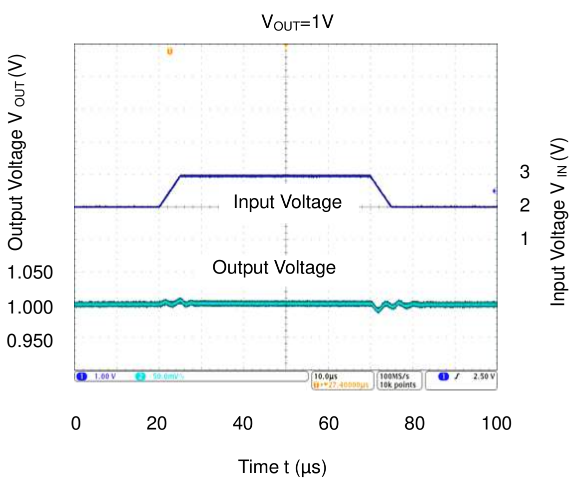


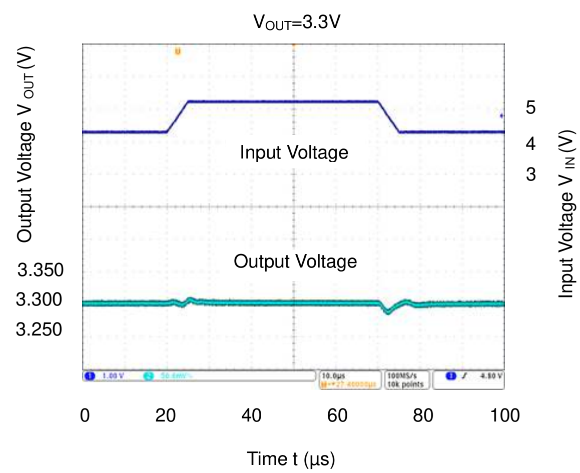
Typical Characteristics (Cont.)

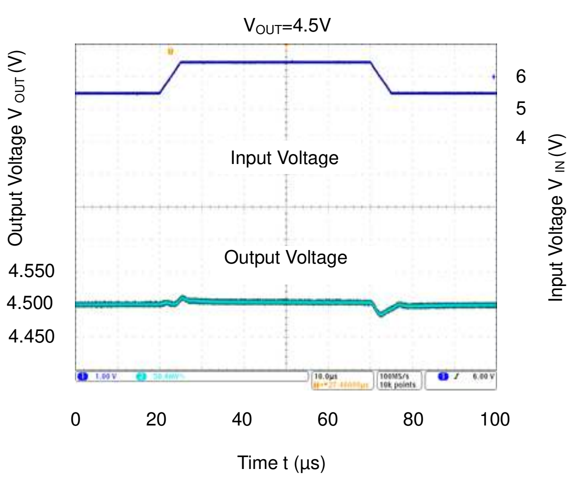




Line Transient Response Waveforms (I_{OUT} = 30mA, t_R = t_F = 5μs, C_{IN} = None, C_{OUT} = 1μF, T_A = +25°C)

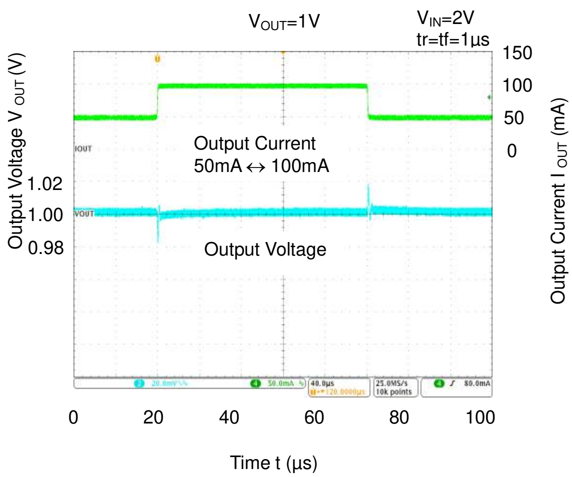


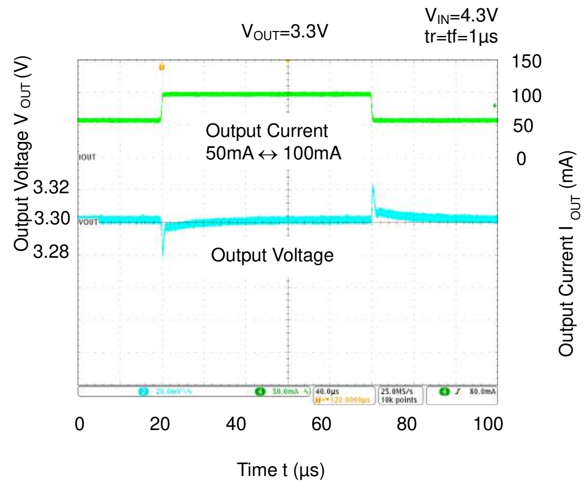


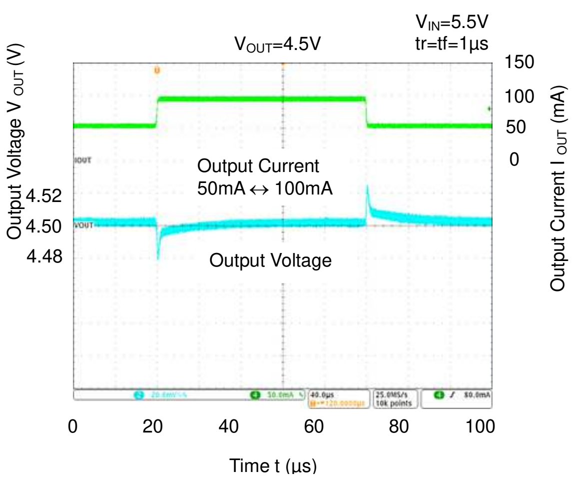


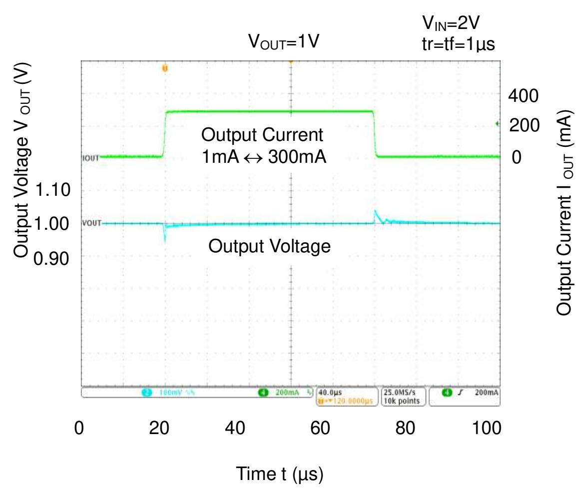
Typical Characteristics (Cont.)

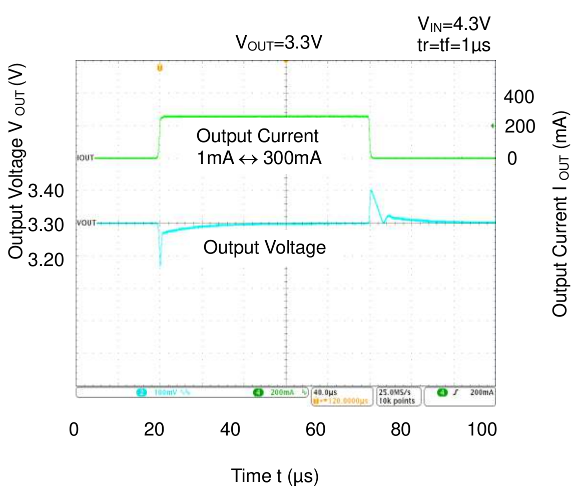
Load Transient Response Waveforms (V_{IN} = V_{OUT}+1V, C_{IN} = C_{OUT} = 1μF, T_A = +25°C)

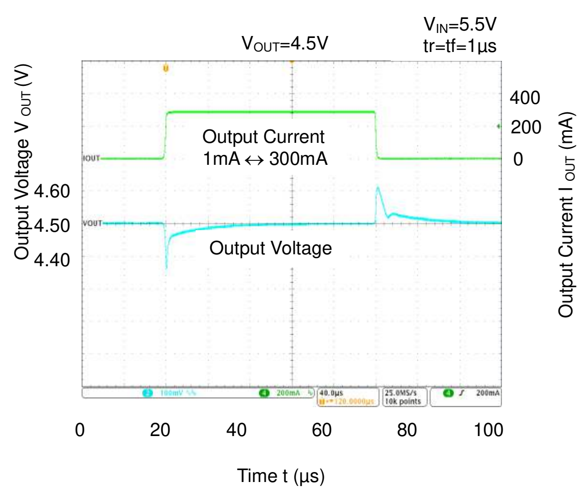






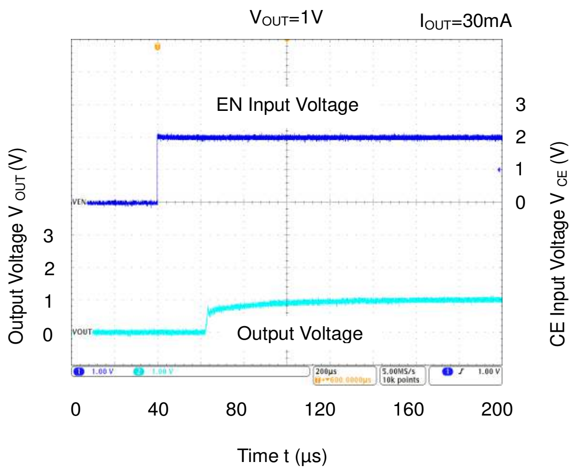


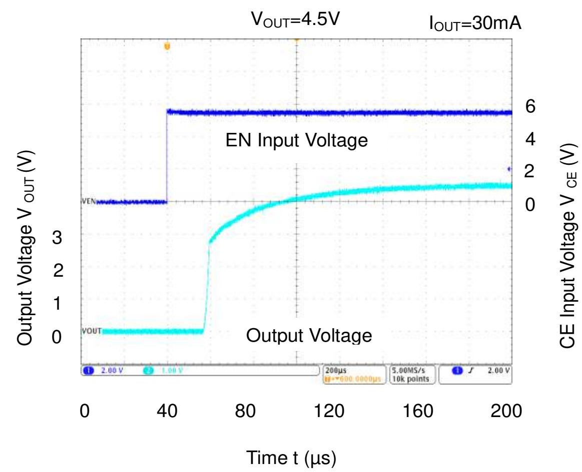


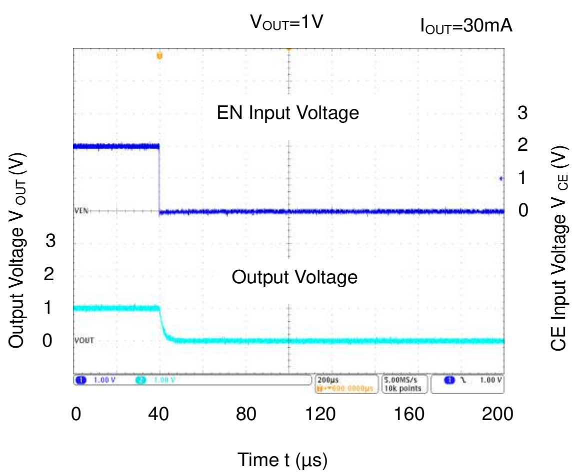


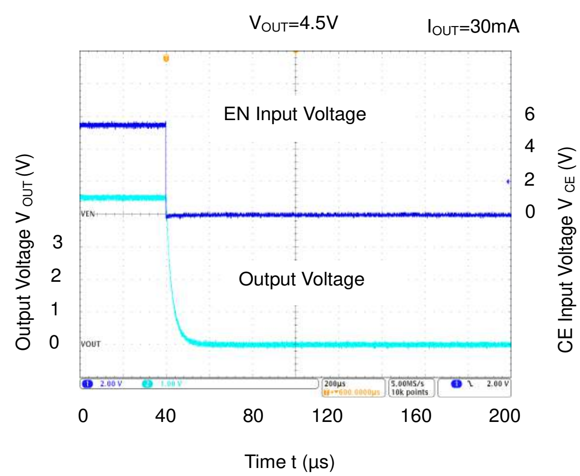
Typical Characteristics (Cont.)

Turn On & Off Waveforms (V_{IN} = V_{OUT}+1V, C_{IN} = 1μF, C_{OUT} = 1μF, T_A = +25°C)









Application Information

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The AP7330 is stable with very small ceramic output capacitors. The ESR (equivalent series resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor (C_{IN}). A minimum 0.47μF ceramic capacitor is recommended between V_{IN} and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND pins.

Enable Control

The AP7330 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to V_{IN} pin to keep the regulator output on at all times. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

Short Circuit Protection

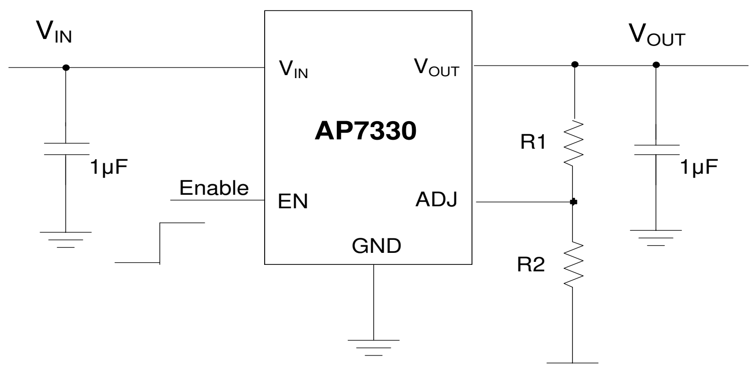
When V_{OUT} pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from overcurrent and damage due to overheating.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

Adjustable Operation

The AP7330 provides output voltage from 1V to 4.5V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

Where V_{REF} = 0.8V (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

To maintain the stability of the internal reference voltage, R2 need to be kept smaller than 10k.

Ordering Information (Note 12)

AP7330X - X - X

Output Discharge	Package	Packing
Blank : Non-discharge D : Output Discharge	W5 : SOT25	7 : Tape & Reel

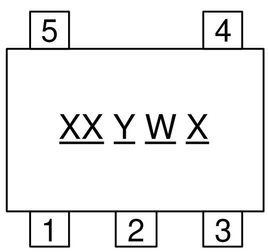
Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7330-W5-7	W5	SOT25	3,000/Tape & Reel	-7
AP7330D-W5-7	W5	SOT25	3,000/Tape & Reel	-7

Note: 12. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

(1) SOT25

(Top View)



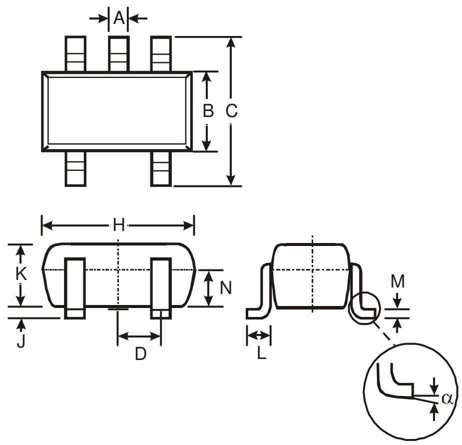
XX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package Type	Identification Code
AP7330-W5-7	SOT25	YH
AP7330D-W5-7	SOT25	YJ

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SOT25

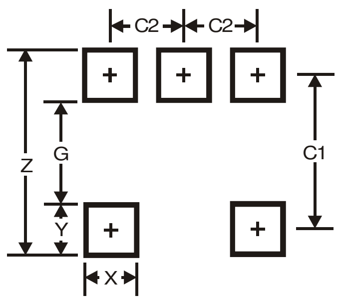


SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

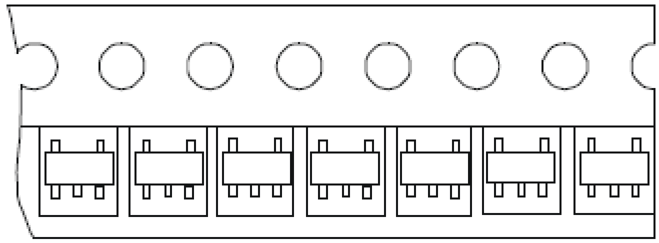
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SOT25



Dimensions	Value
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

Tape Orientation



Note: 13. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf.

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   2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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