1200V Cascoded N-Channel MOSFET

Features

- 1200V breakdown voltage
- Low threshold, 1.6V max.
- High input impedance
- Low input capacitance
- Integrated high voltage resistor divider
- Integrated 1000:1 resistor divider
- Compact 3x3 LFGA package

Applications

- High voltage shunt regulator
- High voltage linear amplifier
- High voltage digital pulsers
- High voltage sensing circuit

General Description

The LN100 is a 1200V cascoded N-channel MOSFET with an integrated high value high voltage resistor divider. Multiple devices can be used in series for voltages greater than 1200V. A resistor divider ratio of 1000:1 is provided. High value resistors are used to minimize power consumption.

The maximum Gate-to-Source threshold voltage is 1.6V. This allows the Gate to be controlled by low voltage circuitry. The LN100 can be used as a high voltage low power pulser. It can also be used in a high voltage low current amplifier application where it is used to charge and discharge a small capacitive load.

Ordering Information

Part Number	Package Option	Packing
LN100LA-G	6-Lead LFGA	3000/Reel

ESD Sensitive Device

Product Summary

BV_{DSS} min (V)	$R_{DS(ON)}$ max (kΩ)	$I_{D(ON)}$ min (mA)
1200	3.0	3.0

Absolute Maximum Ratings

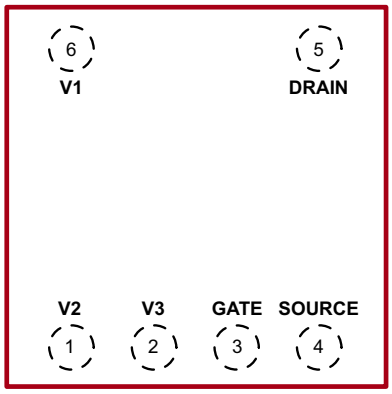
Parameter	Value
Drain-to-Source voltage	1200V
V_1 - V_2 differential voltage	1200V
V_2 - V_3 differential voltage	5.0V
Operating temperature range	-25°C to +125°C
Power dissipation, T_A = 25°C	350mW[1]

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

1. *Device mounted on a 25mm x 25mm x 1.57mm board.*

Pin Configuration



6-Lead LFGA
(top view)
Pads are at bottom of package.

Typical Thermal Resistance

Package	θ_{ja}
6-Lead LFGA	186°C/W

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

Package may or may not include the following marks: Si or

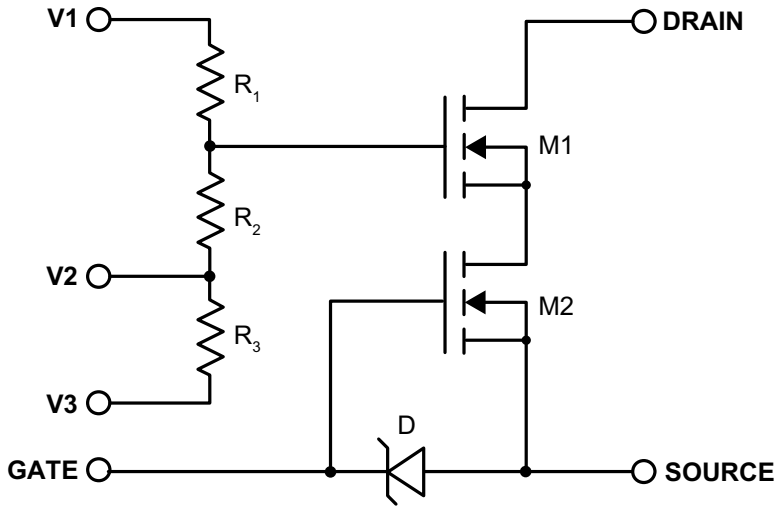
6-Lead LFGA

Electrical Characteristics

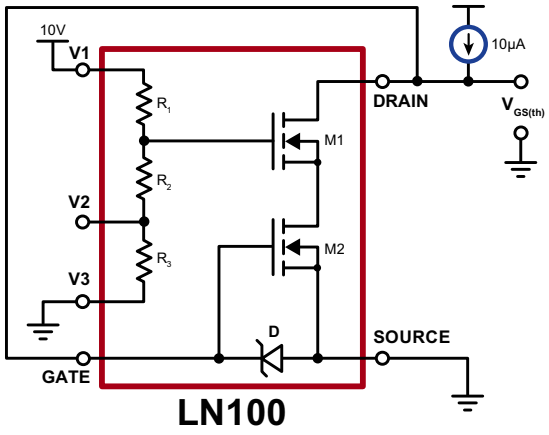
(T_j = 25ºC unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
MOSFET M1 and M2						
BV_{DSS1}	Drain-to-Source breakdown voltage of M1	600	-	-	V	V_{GS} = 0V, I_D = 1.0µA
BV_{DSS2}	Drain-to-Source breakdown voltage of M2	600	-	-	V	V_{GS} = 0V, I_D = 1.0µA
$V_{GS(th)}$	Gate-to-Source threshold voltage	0.5	-	1.6	V	V_{GS} = V_{DS}, I_D = 10µA See test circuit
$R_{DS(ON)}$	Static Drain-to-Source On-State resistance	-	-	3.0	kΩ	V_{GS} = 2.8V, I_D = 2.0mA See test circuit
$I_{D(ON)}$	On-State Drain current	3.0	-	-	mA	V_{GS} = 2.8V, V_{DS} = 25V See test circuit
C_{ISS}	Input capacitance	-	-	50	pF	V_{GS} = 0V, V_{DS} = 25V
Zener Diode						
V_Z	M2 Gate-to-Source Zener diode clamp	6.5	-	12	V	I_{GS} = 1.0mA, V_S = 0V
I_{GS}	Gate-to-Source Zener diode leakage	-	-	100	nA	V_{GS} = 4.5V
I_Z	Maximum Zener current	-	10	-	mA	---
Resistors R_1, R_2, and R_3						
$R_1 + R_2$	Resistor divider $R_1 + R_2$	54	-	-	MΩ	V_1 = 0 to 1000V, V_2 = 0V
R_1	Resistor R_1	27	-	-	MΩ	V_{R1} = 0 to 500V
R_2	Resistor R_2	27	-	-	MΩ	V_{R2} = 0 to 500V
R_3	Resistor R_3	54	-	-	kΩ	V_{R3} = 0 to 5.0V
ΔR	R_1, R_2, and R_3 matching	-	-	±18	%	---

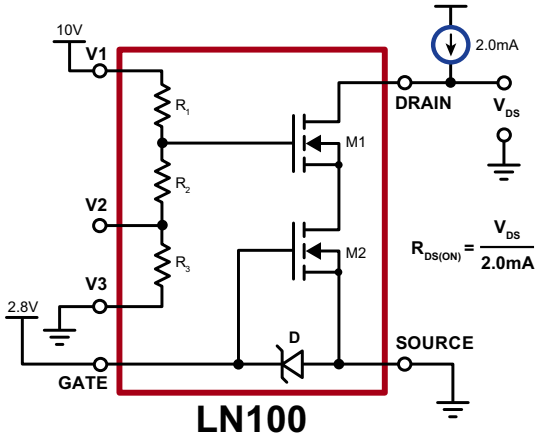
Block Diagram



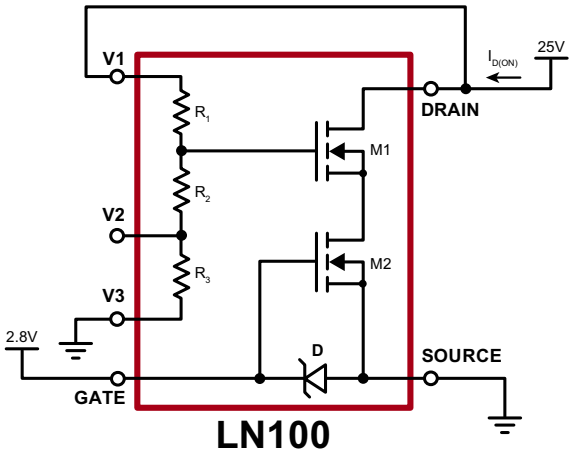
Test Circuits



Gate-to-Source Threshold Voltage



Drain-to-Source On-Resistance



On-State Drain Current

Typical Application Circuits

High Voltage, Low Current Shunt Regulator

The LN100 can be used as a high voltage, low current shunt regulator as shown in Figure 1. Resistor divider R_1, R_2, and R_3 divides the output voltage by approximately 1000. V2 is the feedback voltage for the op-amp. If the reference voltage, V_{REF}, is 1.0V, the output voltage will be shunted to 1000V.

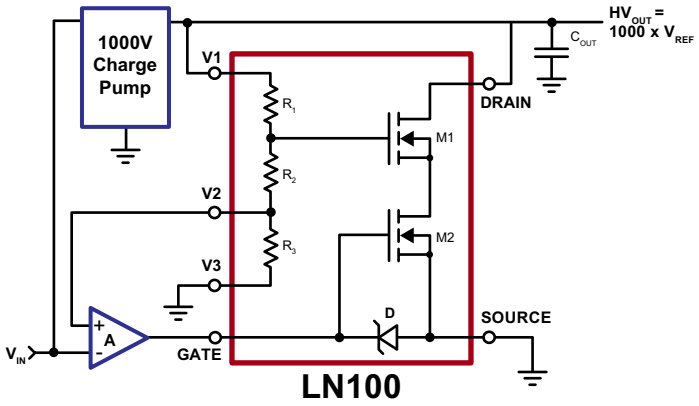


Figure 1: High Voltage, Low Current, Shunt Regulator

High Voltage, Low Current Linear Amplifier

In Figure 2, the two LN100's are used as the main output stage for a 1000V low frequency amplifier to drive capacitive loads. The top LN100 is used to actively charge the load up to the desired voltage. The bottom LN100 is used to actively discharge the load to the desired voltage.

The Gate is driven with a low voltage op-amp. V_2 is the feedback voltage for the op-amp setting it to a gain of 60dB. A 0 to 1.0V sinusoidal waveform on V_{IN} will create a 0 to 1000V sinusoidal waveform on HV_{OUT}. Output frequency only needs to go up to 300Hz.

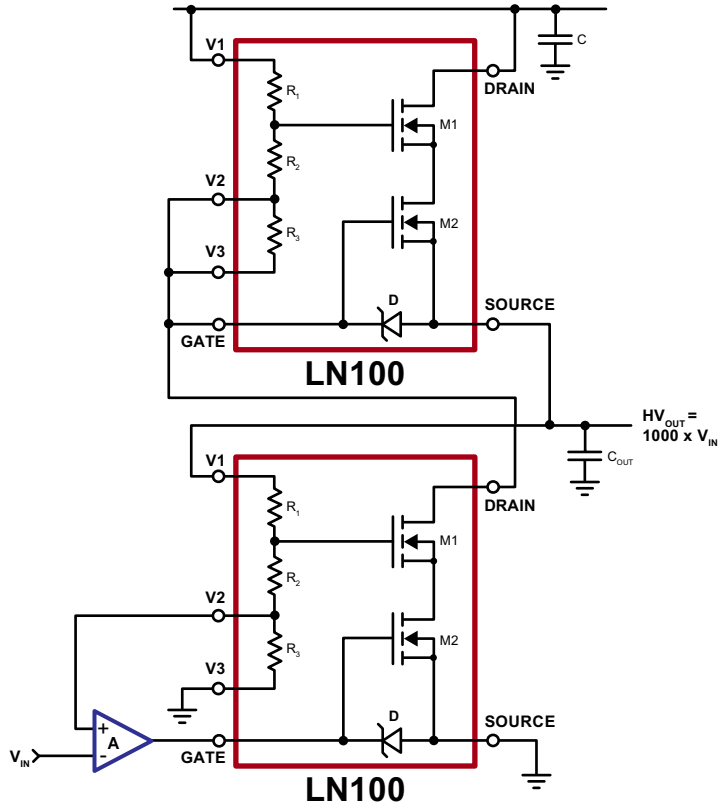


Figure 2: High Voltage Low Current Linear Amplifier

Typical Application Circuits *(cont.)*

High Voltage, Low Current Digital Pulser

In Figure 3, the six LN100's are used as the main output stage for a 3000V low frequency digital pulser. The first three LN100s are used to charge the load up to 3000V. The next three LN100s are used to discharge the load back to ground. The integrated resistors in each of the LN100 allows the 3000V to be divided into thirds. Each LN100 will only need to hold off 1000V.

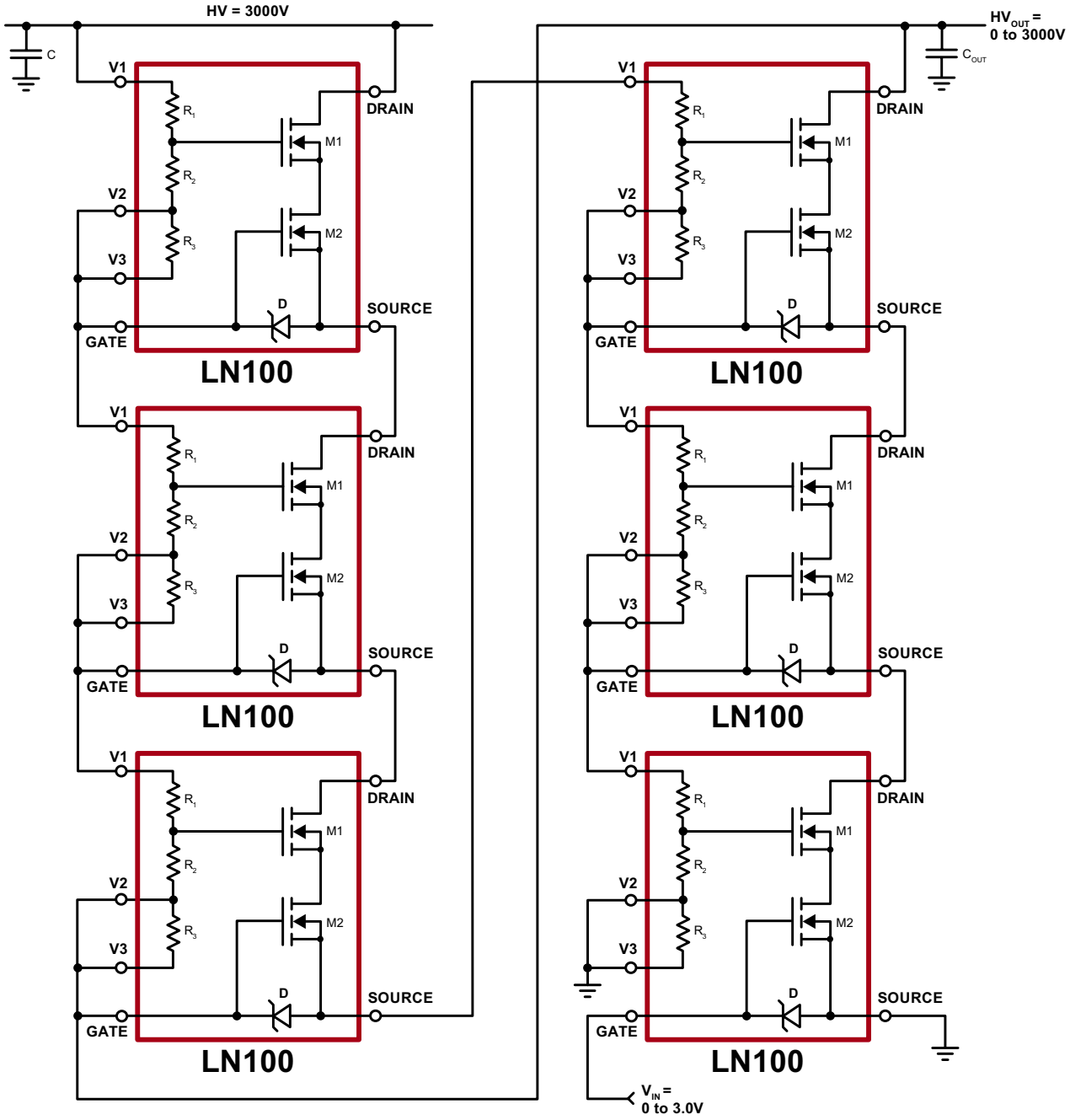
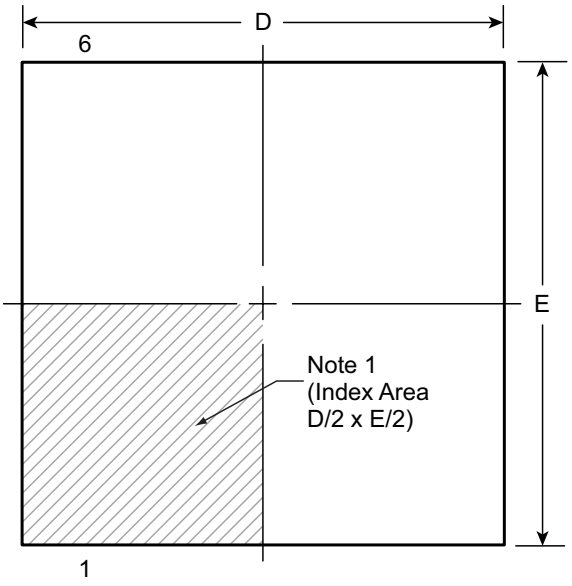


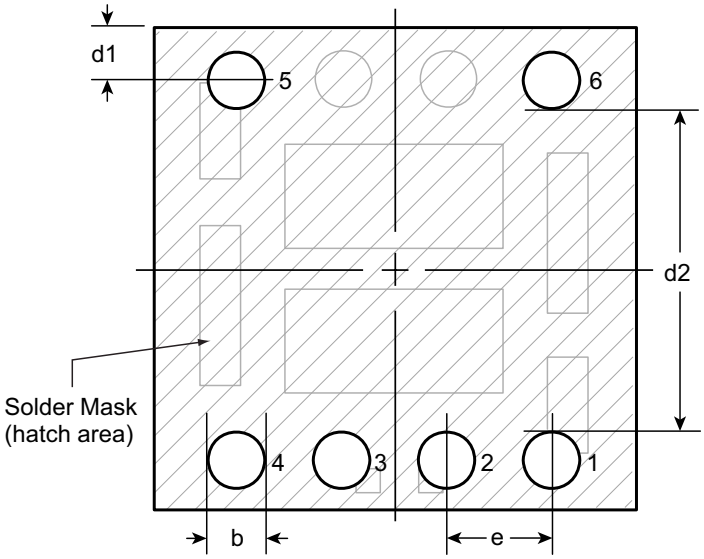
Figure 3: High Voltage Low Current 3000V Digital Pulser

6-Lead LFGA Package Outline (LA)

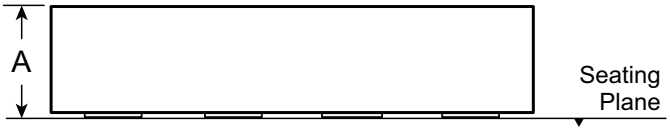
3.00x3.00mm body, 0.85mm height (max), 0.65mm pitch



Top View



Bottom View



Side View

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	b	D	E	d1	d2	e
Dimension (mm)	MIN	0.75	0.30	2.925	2.925	0.225	2.00 BSC	0.65 BSC
	NOM	0.80	0.35	3.000	3.000	0.325		
	MAX	0.85	0.40	3.075	3.075	0.425		

Drawings not to scale

Supertex Doc. #: *DSPD-6LFGALA3X3P065, Version A110811*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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