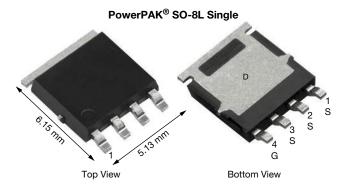


Vishay Siliconix

Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	,
V _{DS} (V)	30
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0093
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.0138
I _D (A)	30
Configuration	Single
Package	PowerPAK SO-8L



FEATURES

- TrenchFET[®] power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

N-Channel MOSFET

D



KOHS COMPLIANT HALOGEN FREE

ABSOLUTE MAXIMUM RATINGS	S (T _C = 25 °C, unless	s otherwise noted)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current ^a	T _C = 25 °C	L_	30		
	T _C = 125 °C	ID	30		
Continuous Source Current (Diode Conduction) ^a		I _S	30	А	
Pulsed Drain Current ^b		I _{DM}	120		
Single Pulse Avalanche Current L = 0.1 mH		I _{AS}	23		
Single Pulse Avalanche Energy		E _{AS}	26	mJ	
Maximum Power Dissipation ^b	$T_{\rm C} = 25 ^{\circ}{\rm C}$ 46	46	W		
Maximum Fower Dissipation	T _C = 125 °C	P _D	15	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260	C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	65	°C/W
Junction-to-Case (Drain)		R _{thJC}	3.2	0/10

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR4 material).

d. See Solder Profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

1

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SQJ840EP

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Static Drain-Source Breakdown Voltage Gate-Source Threshold Voltage Gate-Source Leakage Zero Gate Voltage Drain Current On-State Drain Current ^a Drain-Source On-State Resistance ^a	V _{DS} V _{GS(th)} I _{GSS} I _{DSS} I _{D(on)}	V _{DS} =	= 0 V, $I_D = 250 \mu A$ = V_{GS} , $I_D = 250 \mu A$ = 0 V, $V_{GS} = \pm 20 V$ $V_{DS} = 30 V$ $V_{DS} = 30 V$, $T_J = 125 \ ^{\circ}C$	30 1.2 -	- 1.7 -	- 2.2	v
Gate-Source Threshold Voltage Gate-Source Leakage Zero Gate Voltage Drain Current On-State Drain Current ^a	V _{GS(th)} IGSS I _{DSS}	$V_{DS} = V_{DS} = V_{DS} = V_{GS} = 0 V$ $V_{GS} = 0 V$	= V_{GS} , $I_D = 250 \ \mu A$ = 0 V, $V_{GS} = \pm 20 \ V$ $V_{DS} = 30 \ V$	1.2 -		- 2.2	v
Gate-Source Leakage	I _{GSS} I _{DSS}	$V_{DS} = V_{GS} = 0 V$ $V_{GS} = 0 V$		-		2.2	v
Zero Gate Voltage Drain Current On-State Drain Current ^a	I _{GSS} I _{DSS}	$V_{GS} = 0 V$ $V_{GS} = 0 V$	V _{DS} = 30 V		-		
On-State Drain Current ^a		V _{GS} = 0 V		-		± 100	nA
On-State Drain Current ^a			V _{DS} = 30 V, T _J = 125 °C		-	1	
	I _{D(on)}	$V_{GS} = 0 V$		-	-	50	
	I _{D(on)}		V _{DS} = 30 V, T _J = 175 °C	-	-	150	
Drain-Source On-State Resistance ^a		$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	30	-	-	Α
Drain-Source On-State Resistance ^a		$V_{GS} = 10 V$	I _D = 10.3 A	-	0.0075	0.0093	nA μA Α Δ Δ Δ Δ Δ Δ Δ Δ Δ Δ Δ Δ
Drain-Source On-State Resistance ~	Р	$V_{GS} = 10 V$	I _D = 10.3 A, T _J = 125 °C	-	0.0115	0.0150	
	R _{DS(on)}	V _{GS} = 10 V	I _D = 10.3 A, T _J = 175 °C	-	0.0140	0.0170	
		$V_{GS} = 4.5 V$	I _D = 8.7 A	-	0.0110	0.0138	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 16 A		-	38	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 15 V, f = 1 MHz	-	1550	1900	pF
Output Capacitance	Coss			-	575	690	
Reverse Transfer Capacitance	C _{rss}			-	210	260	
Total Gate Charge ^c	Qg			-	25.3	38	
Gate-Source Charge ^c	Q_gs	$V_{GS} = 10 V$	$V_{DS} = 15 \text{ V}, I_D = 16.5 \text{ A}$	-	3.7	-	nC
Gate-Drain Charge ^c	Q _{gd}			-	5.4	-	
Gate Resistance	Rg	f = 1 MHz		0.4	-	1.5	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	11	15	
Rise Time ^c	t _r	$\label{eq:V_DD} \begin{array}{l} V_{DD} = 15 \; V, \; R_L = 15 \; \Omega \\ I_D \cong 1 \; A, \; V_GEN = 10 \; V, \; R_g = 1 \; \Omega \end{array}$		-	11	15	- ns
Turn-Off Delay Time ^c	t _{d(off)}			-	28	35	
Fall Time ^c	t _f	1	-	17	25		
Source-Drain Diode Ratings and Character	ristics ^b						
Pulsed Current ^a							
Forward Voltage	I _{SM}			-	- 1	120	А

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

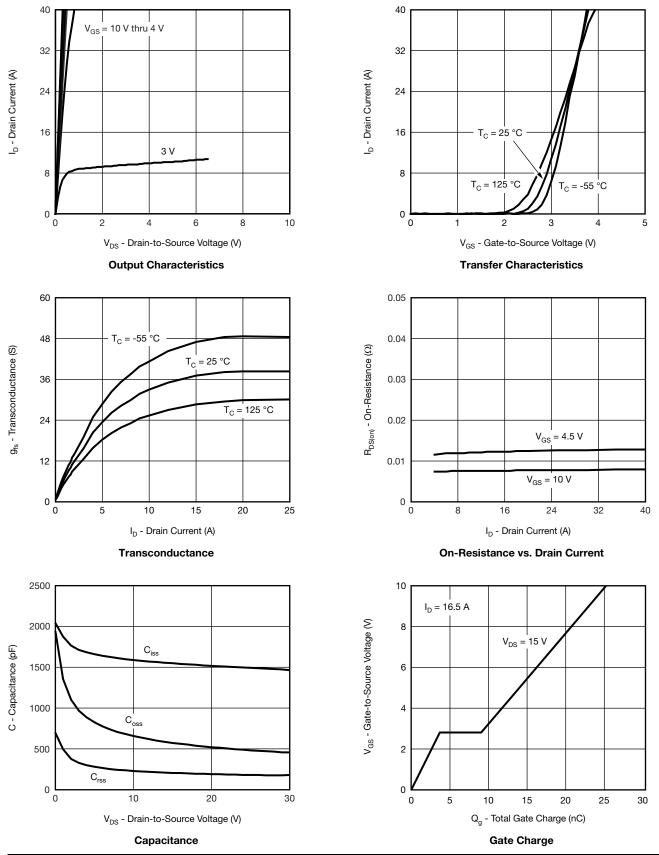
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



S15-1878-Rev. C, 17-Aug-15

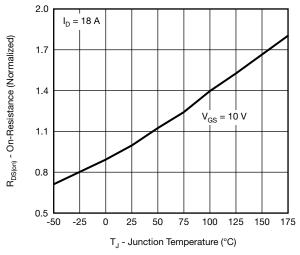
3

Document Number: 70325

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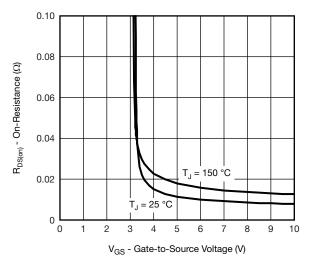
SQJ840EP

TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)

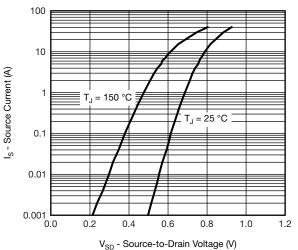


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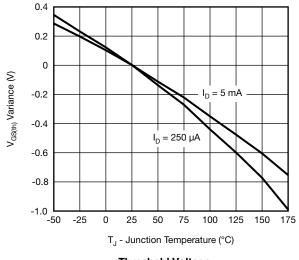
On-Resistance vs. Junction Temperature



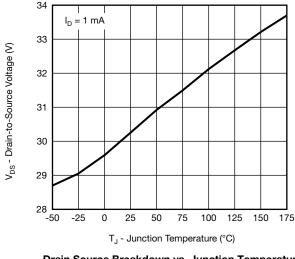
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage







Drain Source Breakdown vs. Junction Temperature

S15-1878-Rev. C, 17-Aug-15

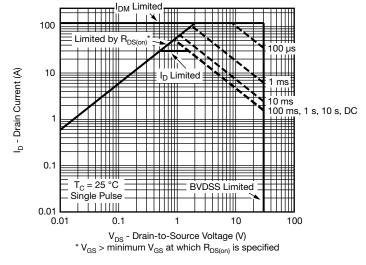
Document Number: 70325

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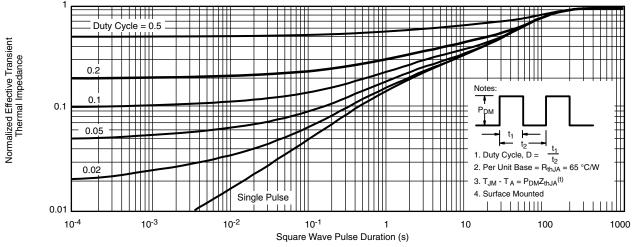
4



THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Safe Operating Area

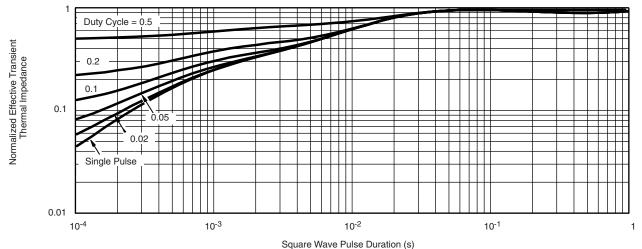


Normalized Thermal Transient Impedance, Junction-to-Ambient



Vishay Siliconix

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70325.



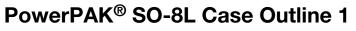
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REVISION	HISTORY ^a	
REVISION	DATE	DESCRIPTION OF CHANGE
С	04-Aug-15	Revised R _g minimum limit

Note

a. As of April 2014

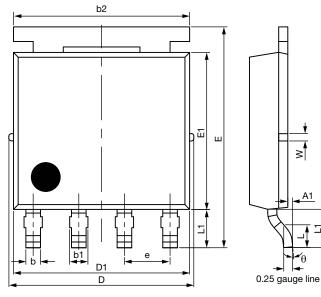


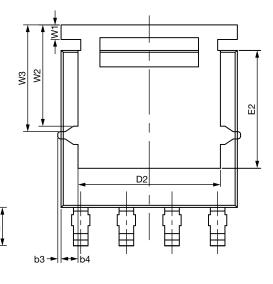


1

A1

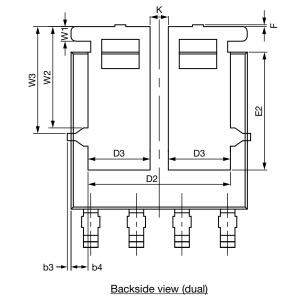
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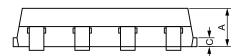




Topside view

Backside view (single)





Package Information



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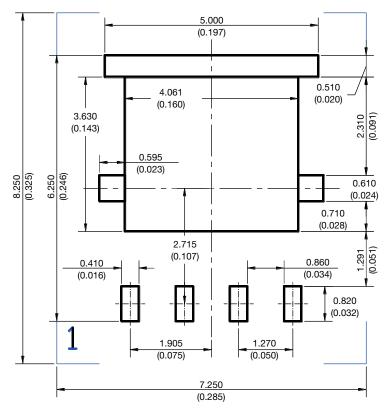
514		MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094		0.004				
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC			0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	3.18	3.28	3.38	0.125	0.129	0.133		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
К		0.51			0.020			
W		0.23			0.009			
W1	0.41			0.016				
W2	2.82			0.111				
W3		2.96		0.117				
θ	0°	-	10°	0°	-	10°		

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK[®] SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)

Revision: 07-Feb-12



Vishay

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