SA5211

Transimpedance amplifier (180 MHz)

Rev. 03 — 07 October 1998 **Product specification**

1. Description

The SA5211 is a 28 kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

2. Features

- Extremely low noise: 1.8 pA / $\sqrt{Hz}$
- Single 5 V supply
- Large bandwidth: 180 MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 28 kΩ differential transresistance

3. Applications

- Fiber optic receivers, analog and digital
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific Instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

PHILIPS

4. Pinning information

4.1 Pinning

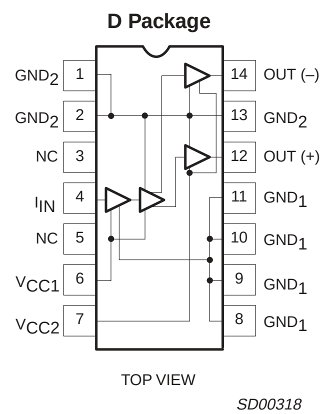


Fig 1. Pin configuration.

5. Ordering information

Table 1: Ordering information

Type number	Package			
	Name	Description	Version	Temperature range (°C)
SA5211D	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	–40 to +85

6. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	power supply		–	6	V
T_{amb}	operating ambient temperature range		-40	+85	°C
T_J	operating junction temperature range		-55	+150	°C
T_{STG}	storage temperature range		-65	+150	°C
$P_{D\ MAX}$	power dissipation, T_A = 25 °C (still-air) [1]		–	1.0	W
$I_{IN\ MAX}$	maximum input current [2]		–	5	mA
θ_{JA}	thermal resistance		–	125	°C/W

[1] Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA} = 125 °C/W

[2] The use of a pull-up resistor to V_{CC}, for the PIN diode is recommended.

Table 3: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
T_{amb}	ambient temperature range		-40	+85	°C
T_J	junction temperature range		-40	+105	°C

7. Static characteristics

Table 4: DC electrical characteristics

Min and Max limits apply over operating temperature range at V_{CC} = 5 V, unless otherwise specified. Typical data apply at V_{CC} = 5 V and T_{amb} = 25 °C.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}	input bias voltage		0.55	0.8	1.00	V
$V_{O\pm}$	output bias voltage		2.7	3.4	3.7	V
V_{OS}	output offset voltage		–	0	130	mV
I_{CC}	supply current		20	26	31	mA
I_{OMAX}	output sink/source current [1]		3	4	–	mA
I_{IN}	input current (2% linearity)	Test Circuit 8, Procedure 2	±20	±40	–	µA
$I_{IN\ MAX}$	maximum input current overload threshold	Test Circuit 8, Procedure 4	±30	±60	–	µA

[1] Test condition: output quiescent voltage variation is less than 100 mV for 3 mA load current.

8. Dynamic characteristics

Table 5: AC electrical characteristics

Typical data and Min and Max limits apply at V_{CC} = 5 V and T_{amb} = 25 °C

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_T	transresistance (differential output)	DC tested RL = ∞ Test Circuit 8, Procedure 1	21	28	36	kΩ
R_O	output resistance (differential output)	DC tested	–	30	–	Ω
R_T	transresistance (single-ended output)	DC tested RL = ∞	10.5	14	18.0	kΩ
R_O	output resistance (single-ended output)	DC tested	–	15	–	Ω
f_{3dB}	bandwidth (-3dB)	T_A = 25°C Test circuit 1	–	180	–	MHz
R_{IN}	input resistance		–	200	–	Ω
C_{IN}	input capacitance		–	4	–	pF
ΔR/ΔV	transresistance power supply sensitivity	V_{CC} = 5±0.5 V	–	3.7	–	%/V
ΔR/ΔT	transresistance ambient temperature sensitivity	$\Delta T_{amb} = T_{amb\ MAX} - T_{amb\ MIN}$	–	0.025	–	%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10 MHz TA = 25 °C	–	1.8	–	pA/√Hz
I_T	integrated RMS noise current over the bandwidth (referred to input)	TA = 25 °C Test Circuit 2	–	–	–	–

Table 5: AC electrical characteristics...*continued*
Typical data and Min and Max limits apply at V_{CC} = 5 V and T_{amb} = 25 °C

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_n	C_S = 0 [1]	Δf = 50 MHz Δf = 100 MHz Δf = 200 MHz	– – –	13 20 35	– – –	nA
I_n	C_S = 1pF	Δf = 50 MHz Δf = 100 MHz Δf = 200 MHz	– – –	13 21 41	– – –	nA
PSRR	power supply rejection ratio [2] (V_{CC1} = V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	23	32	–	dB
PSRR	power supply rejection ratio [2] (V_{CC1})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 4	23	32	–	dB
PSRR	power supply rejection ratio [2] (V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 5	45	65	–	dB
PSRR	power supply rejection ratio (ECL configuration) [2]	f = 0.1 MHz Test Circuit 6	–	23	–	dB
V_{OMAX}	maximum differential output voltage swing	RL = ∞ Test Circuit 8, Procedure 3	1.7	3.2	–	V_{P-P}
$V_{IN\ MAX}$	maximum input amplitude for output duty cycle of 50±5% [3]	Test Circuit 7	160	–	–	mV_{P-P}
t_R	rise time for 50mV output signal [4]	Test Circuit 7	–	0.8	1.8	ns

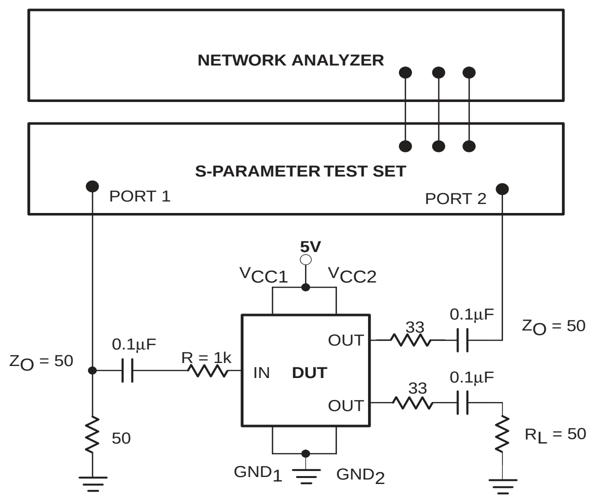
[1] Package parasitic capacitance amounts to about 0.2pF

[2] PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.

[3] Guaranteed by linearity and overload tests.

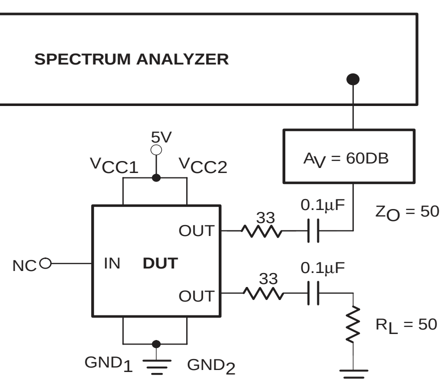
[4] t_R defined as 20 to 80% rise time. It is guaranteed by -3dB bandwidth test.

9. Test circuits



SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}}$ R = 2 × S21 × R	$R_T = \frac{V_{OUT}}{V_{IN}}$ R = 4 × S21 × R
$R_O \approx Z_O \left\| \frac{1 + S22}{1 - S22} \right\| - 33$	$R_O = 2Z_O \left\| \frac{1 + S22}{1 - S22} \right\| - 66$

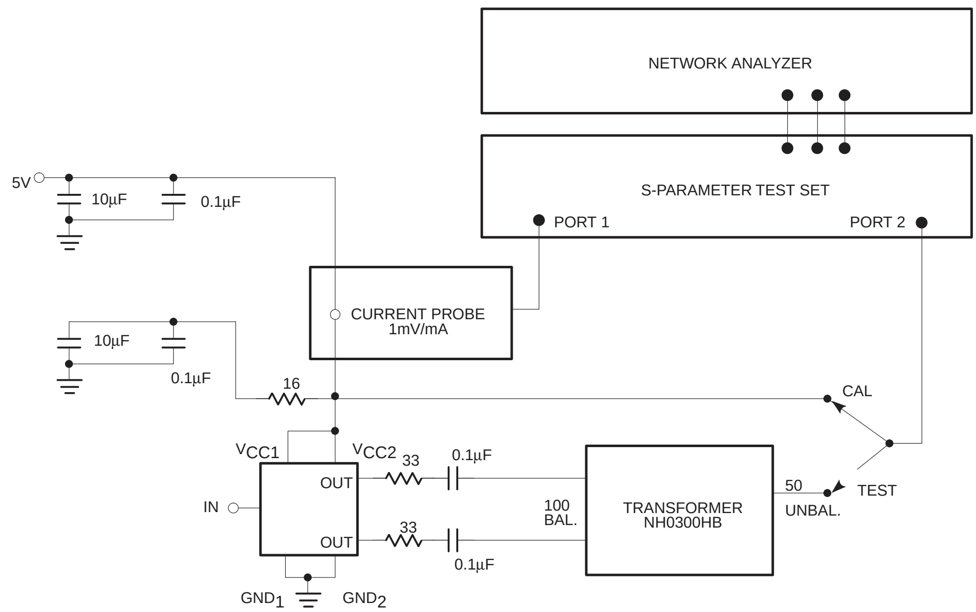
Test Circuit 1



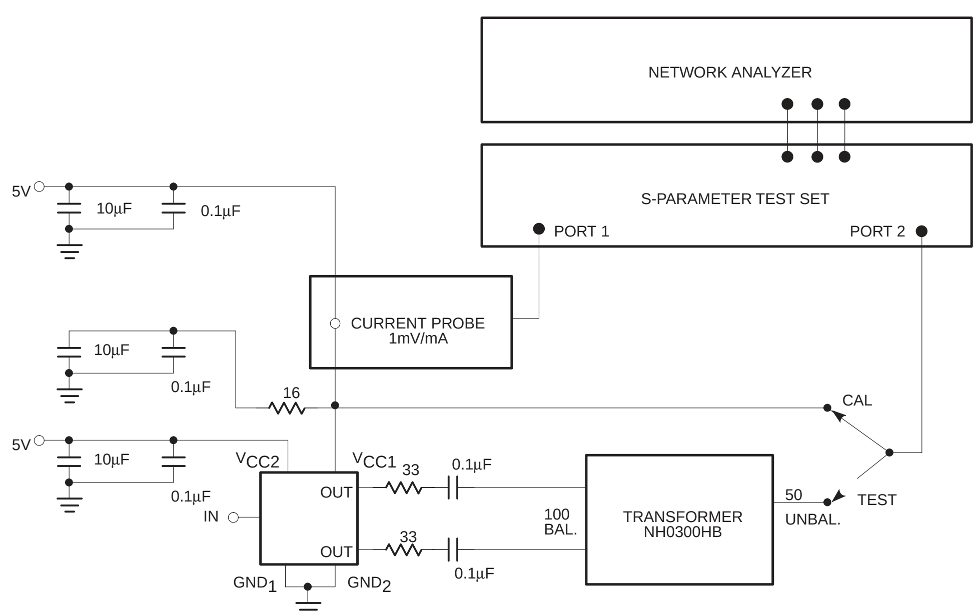
Test Circuit 2

SD00319

Fig 2. Test circuits 1 and 2.



Test Circuit 3



Test Circuit 4

SD00320

Fig 3. Test circuits 3 and 4.

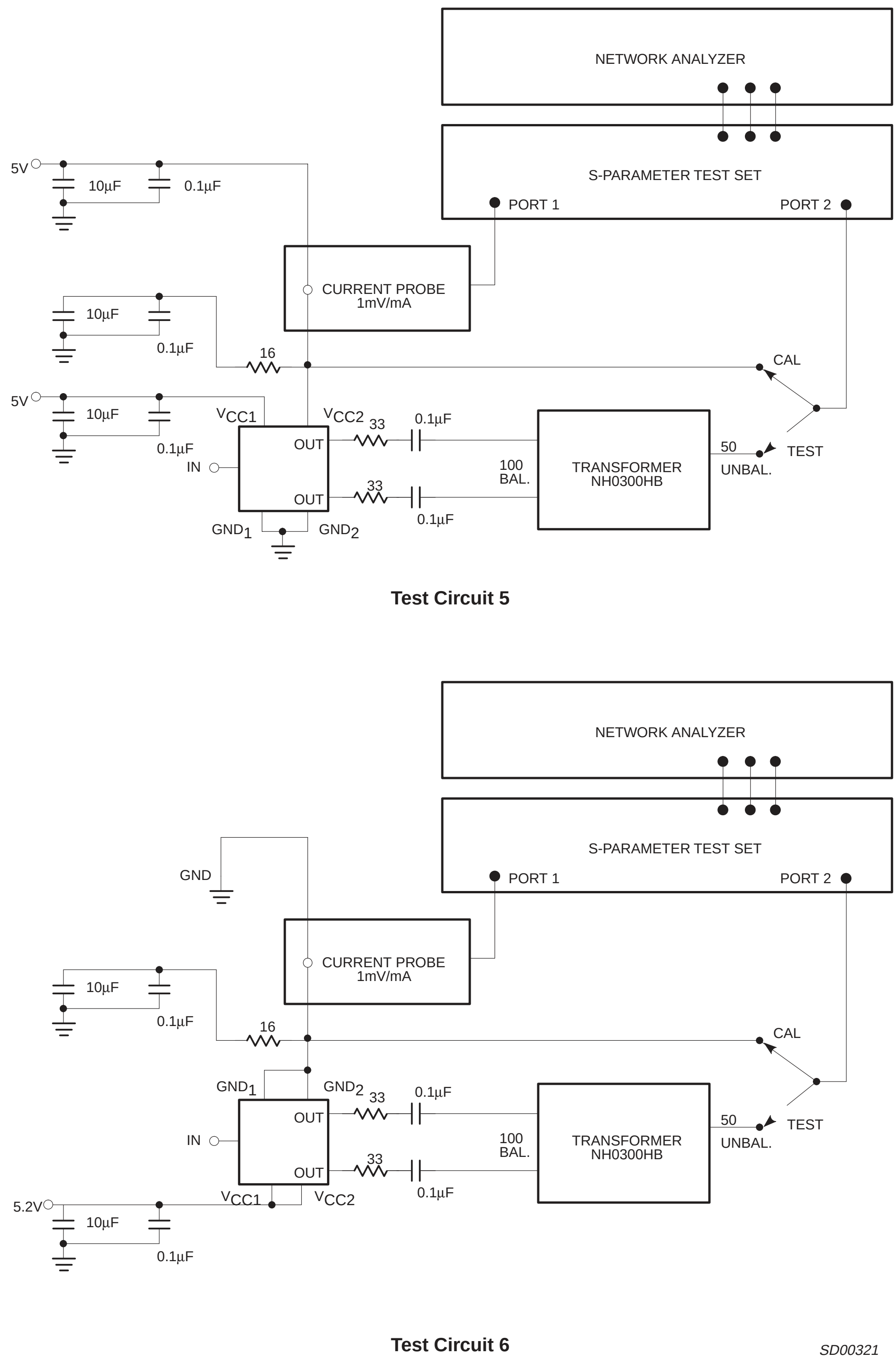


Fig 4. Test circuits 5 and 6.

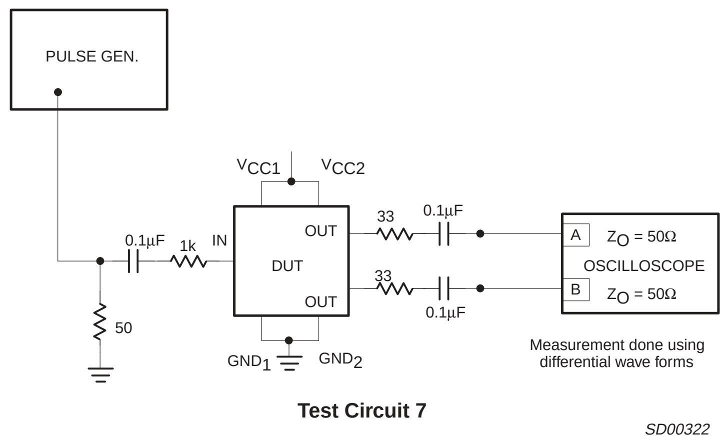
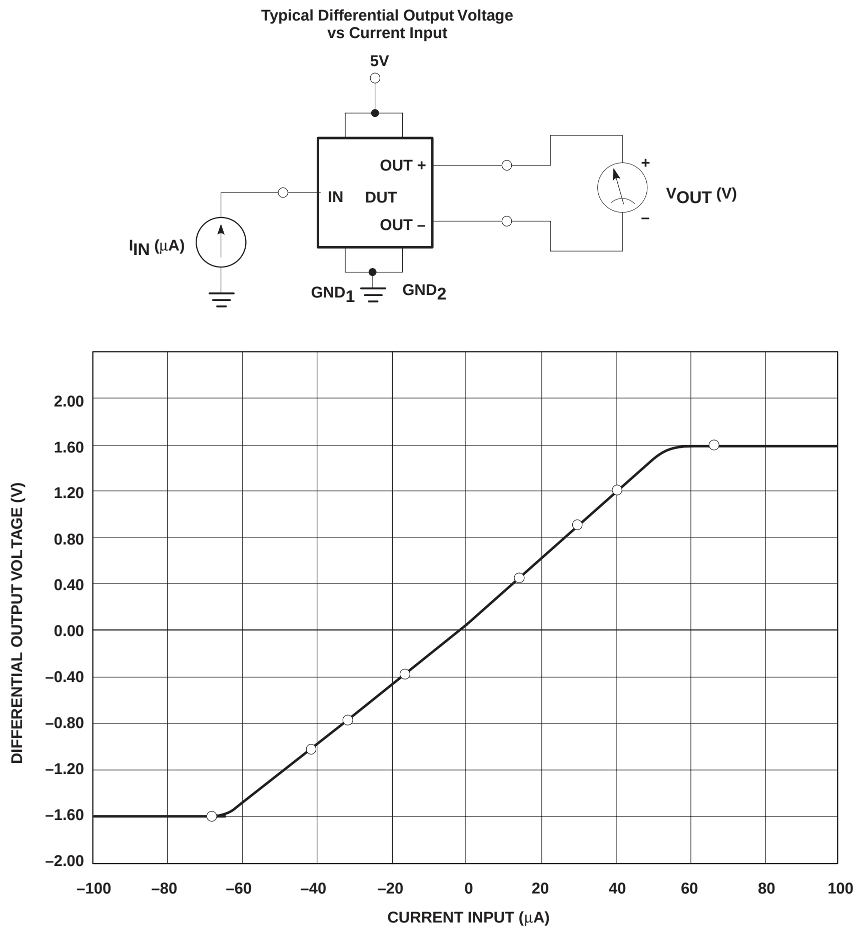


Fig 5. Test circuit 7.



NE5211 TEST CONDITIONS

Procedure 1	R_T measured at 15µA $R_T = (V_{O1} – V_{O2})/(+15µA – (–15µA))$ Where: V_{O1} Measured at I_{IN} = +15µA V_{O2} Measured at I_{IN} = –15µA
Procedure 2	Linearity = 1 – ABS(($V_{OA} – V_{OB}$) / ($V_{O3} – V_{O4}$)) Where: V_{O3} Measured at I_{IN} = +30µA V_{O4} Measured at I_{IN} = –30µA $V_{OA} = R_T \times (+ 30µA) + V_{OB}$ $V_{OB} = R_T \times (– 30µA) + V_{OB}$
Procedure 3	$V_{OMAX} = V_{O7} – V_{O8}$ Where: V_{O7} Measured at I_{IN} = +65µA V_{O8} Measured at I_{IN} = –65µA
Procedure 4	I_{IN} Test Pass Conditions: $V_{O7} – V_{O5}$ > 20mV and $V_{06} – V_{O5}$ > 50mV Where: V_{O5} Measured at I_{IN} = +40µA V_{O6} Measured at I_{IN} = –400µA V_{O7} Measured at I_{IN} = +65µA V_{O8} Measured at I_{IN} = –65µA

Test Circuit 8

SD00331

Fig 6. Test circuit 8.

10. Typical performance characteristics

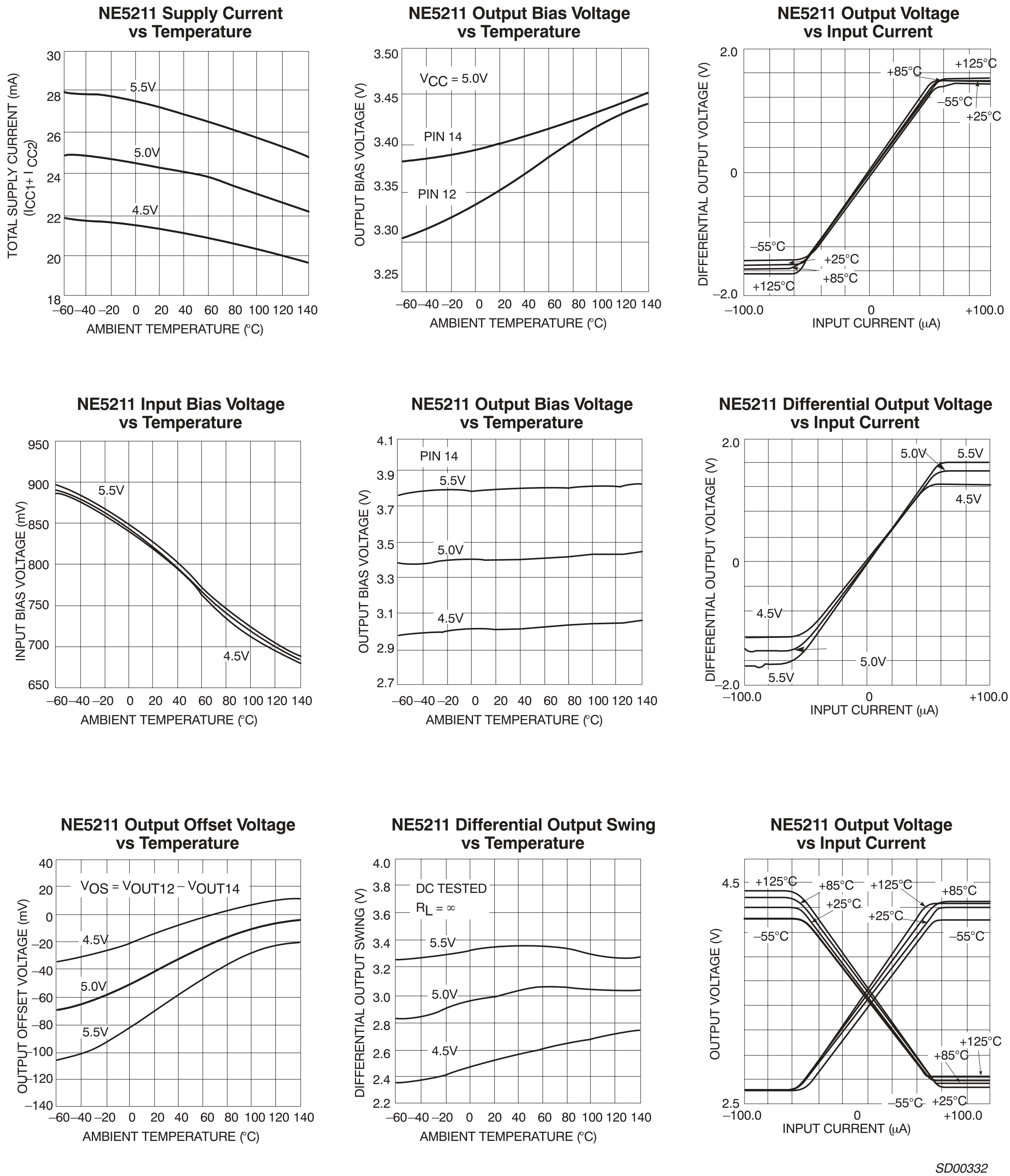


Fig 7. Typical performance characteristics.

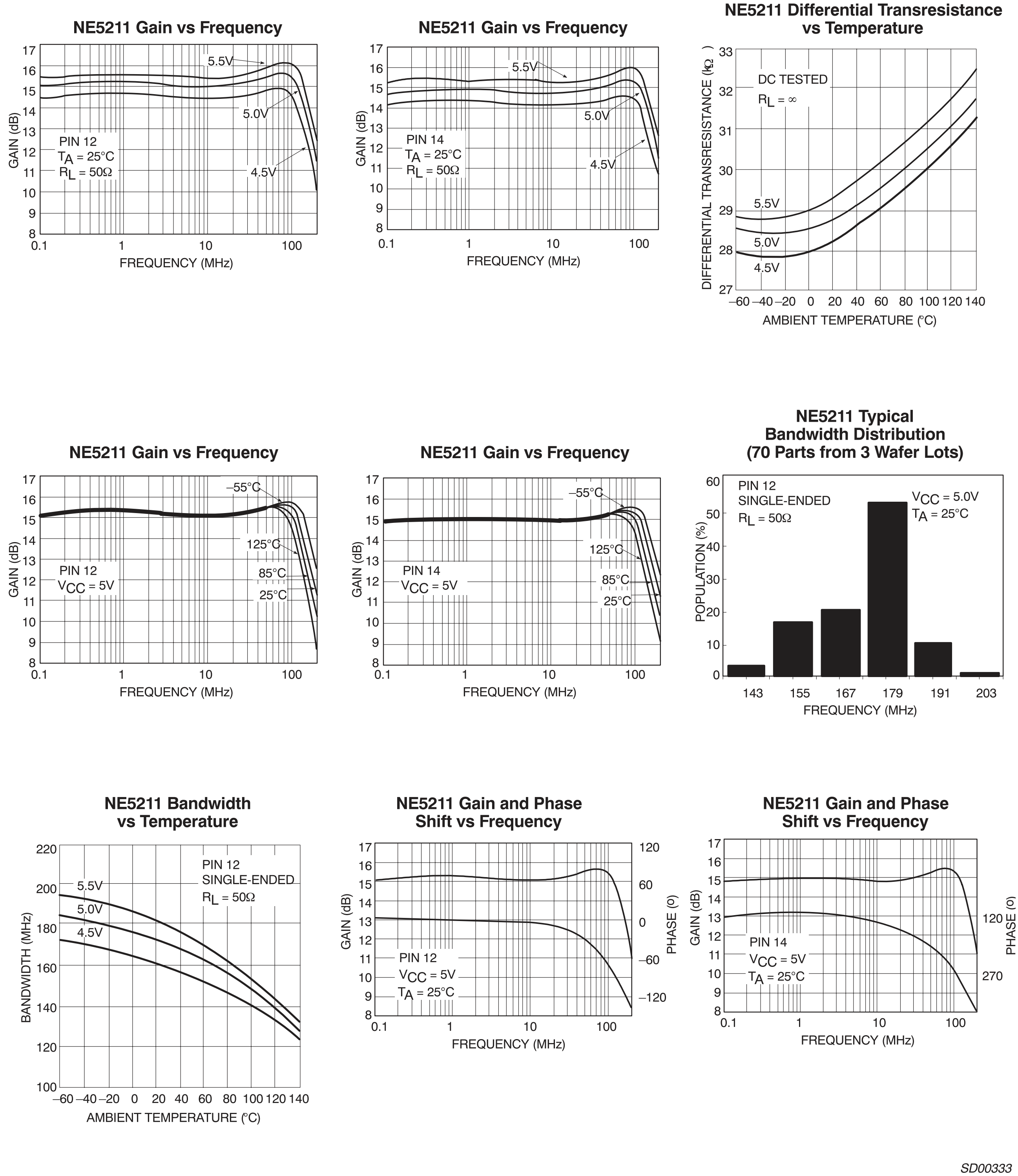


Fig 8. Typical performance characteristics. (cont.)

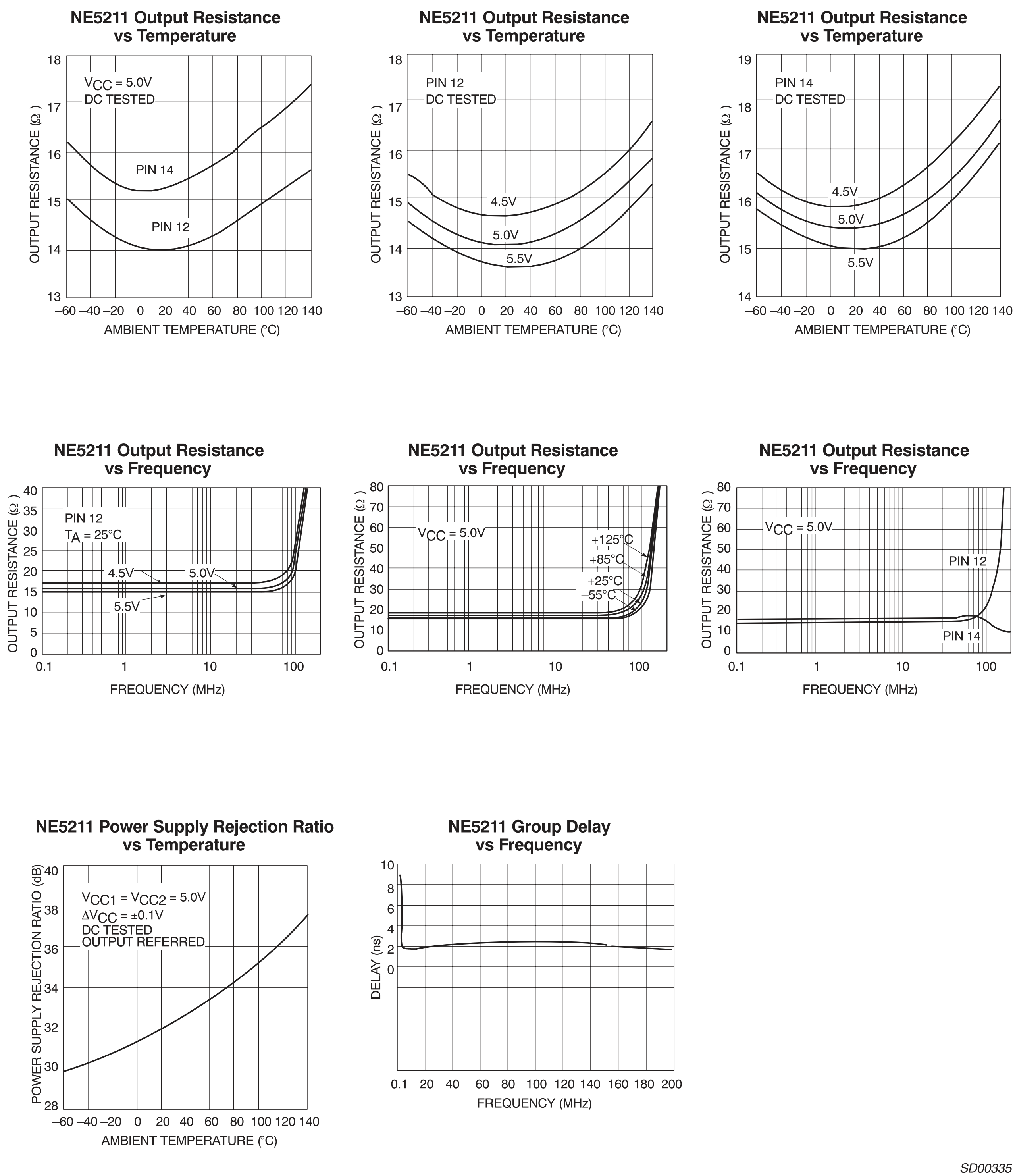


Fig 9. Typical performance characteristics. (cont.)

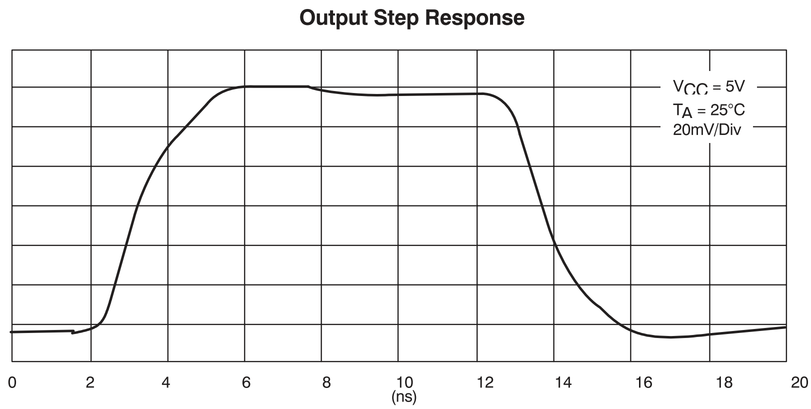


Fig 10. Typical performance characteristics. (cont.)

11. Theory of operation

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The SA5211 is a wide bandwidth (typically 180 MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 50µA. The SA5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 11. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F = 14.4 kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2\,R_F = 2(14.4\text{ K}) = 28.8\text{ k}\Omega \quad (1)$$

The single-ended transresistance of the amplifier is typically 14.4 kΩ.

The simplified schematic in Figure 12 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15} – Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers

Q_{11} – Q_{12} which are biased by constant current sources. The collectors of Q_{11} – Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

12. Bandwidth calculations

The input stage, shown in Figure 13, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 4 pF (typical), assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4\ k\Omega}{71} = 203\Omega \quad (2)$$

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3db} = \frac{1}{2\pi R_{IN} C_{IN}} \quad (3)$$

Assuming typical values for R_F = 14.4 kΩ, R_{IN} = 200 Ω, C_{IN} = 4 pF

$$f_{-3db} = \frac{1}{2\pi\ \ 4\ \text{pF}\ 200\ \Omega} = 200\ \text{MHz} \quad (4)$$

The operating point of Q1, Figure 12, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1 pF, input stage voltage gain of 70, R_{IN} = 60 Ω then the total input capacitance, C_{IN} = (1 + 4) pF which will lead to only a 20% bandwidth reduction.

13. Noise

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 1.8 pA/$\sqrt{\text{Hz}}$ (typical). The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 41 nA RMS in a 200 MHz bandwidth.

14. Dynamic range calculations

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200 MHz bandwidth assuming I_{INMAX} = 60 µA and a wideband noise of I_{EQ} = 41 nA_{RMS} for an external source capacitance of C_S = 1 pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}} \quad (5)$$

$$D_E\ (\text{dB}) = 20\log\frac{(60 \times 10^{-6})}{(\sqrt{2}\ 41\ 10^{-9})} \quad (6)$$

$$D_E(\text{dB}) = 20\log\frac{(60\ \mu\text{A})}{(58\ \text{nA})} = 60\text{db} \quad (7)$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 m/sec

c / λ = optical frequency

No. of incident photons/sec = $\frac{P}{\frac{hc}{\lambda}}$ where P = optical incident power

No. of generated electrons/sec = $\eta \times \frac{P}{\frac{hc}{\lambda}}$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \times \frac{P}{\frac{hc}{\lambda}} \times e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \times e}{\frac{hc}{\lambda}} \text{ Amp/watt}$$

$$I = P \times R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200 MHz), the noise parameter Z_n may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{41 \times 10^{-9}}{(1.6 \times 10^{-19})(200 \times 10^{6})} = 1281 \quad (8)$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}BZ = 12 \times 2.3 \times 10^{-19}$$

$$200 \times 10^{6}(1281) = 719 \text{ nW} = -31.5 \text{ dBm} = 1139 \text{ nW} = -29.4 \text{ dBm} \quad (9)$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the SA5211, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}\frac{1}{\text{Joule}} \times \frac{\text{Joule}}{\text{sec}} \times q = l = \frac{707 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}} = 500 \text{ nA} \quad (10)$$

Choosing the maximum peak overload current of I_{avMAX} = 60 μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}}60 \times 10 \ \mu\text{A} = 86 \ \mu\text{W or} - 10.6 \text{ dBm (optical)} \quad (11)$$

Thus the optical dynamic range, D_O is:

$$D_O = P_{avMAX} - P_{avMIN} = -4.6 - (-29.4) = 24.8 \text{ dB}$$

$$D_O = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6) \quad (12)$$

1. S.D. Personick, *Optical Fiber Transmission Systems,* Plenum Press, NY, 1981, Chapter 3.

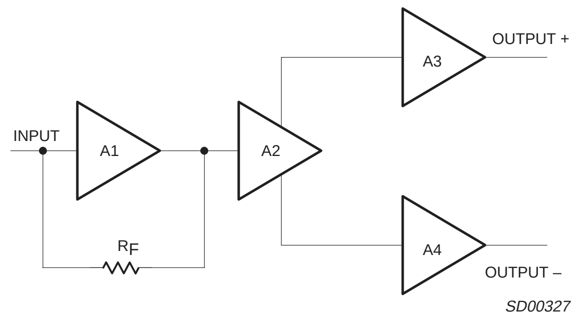


Fig 11. SA5211 – Block diagram.

This represents the maximum limit attainable with the SA5211 operating at 200 MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

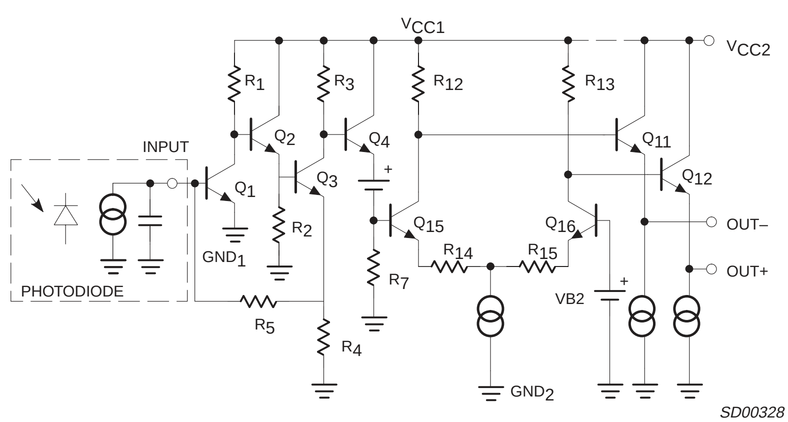


Fig 12. Transimpedance amplifier.

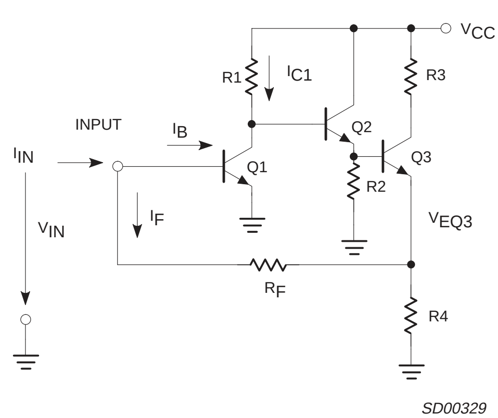


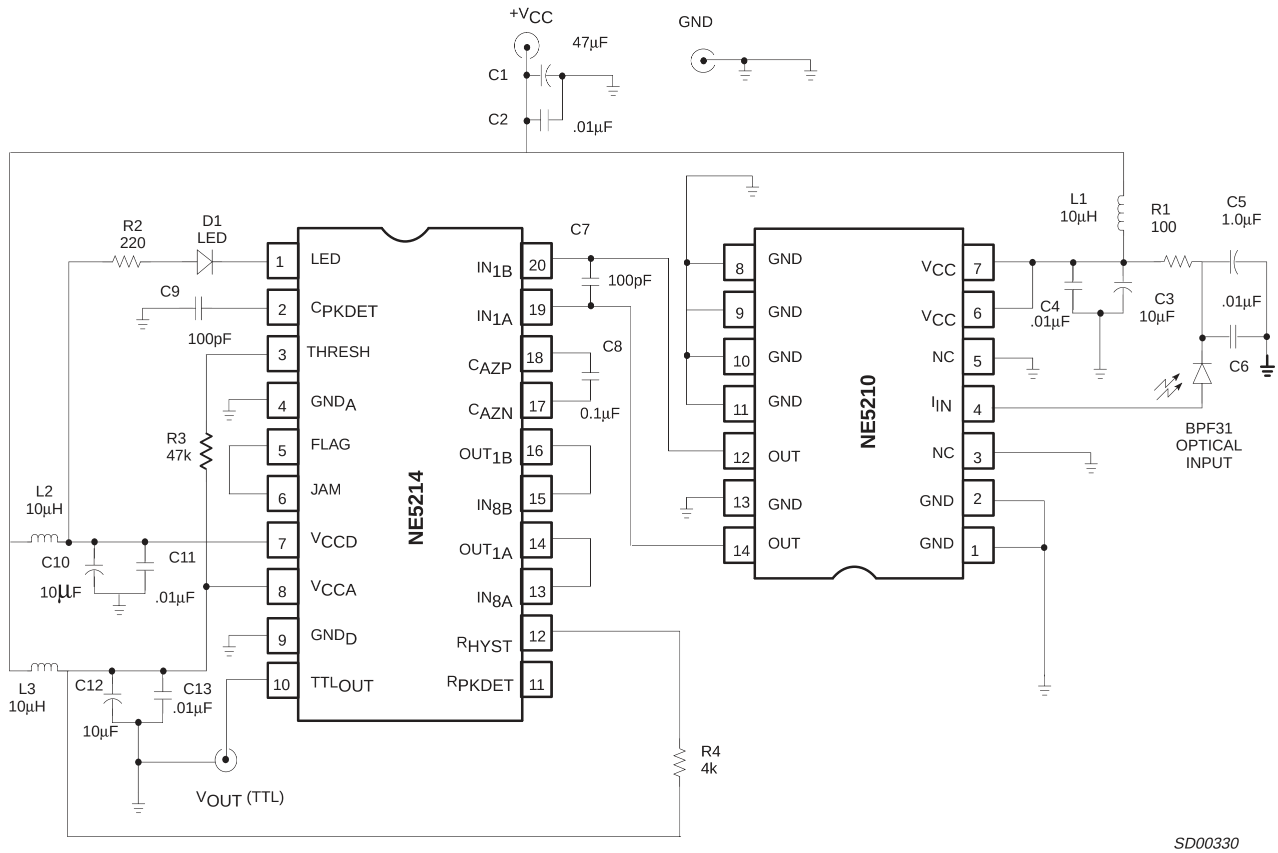
Fig 13. Shunt-series input stage.

15. Application information

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the SA5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8-11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800 MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3 V (for a 5 V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1 µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1 µF capacitors with 10 µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 14 depicts a 50 Mb/s TTL fiber-optic receiver using the BPF31, 850 nm LED, the SA5211 and the SA5214 post amplifier.



The NE5210/NE5217 combination can operate at data rates in excess of 100 Mb/s NRZ
The capacitor C7 decreases the NE5210 bandwidth to improve overall S/N ratio in the DC-50 MHz band, but does create extra high frequency noise on the NE5210 V_{CC} pin(s).

Fig 14. A 50Mb/s fiber optic receiver.

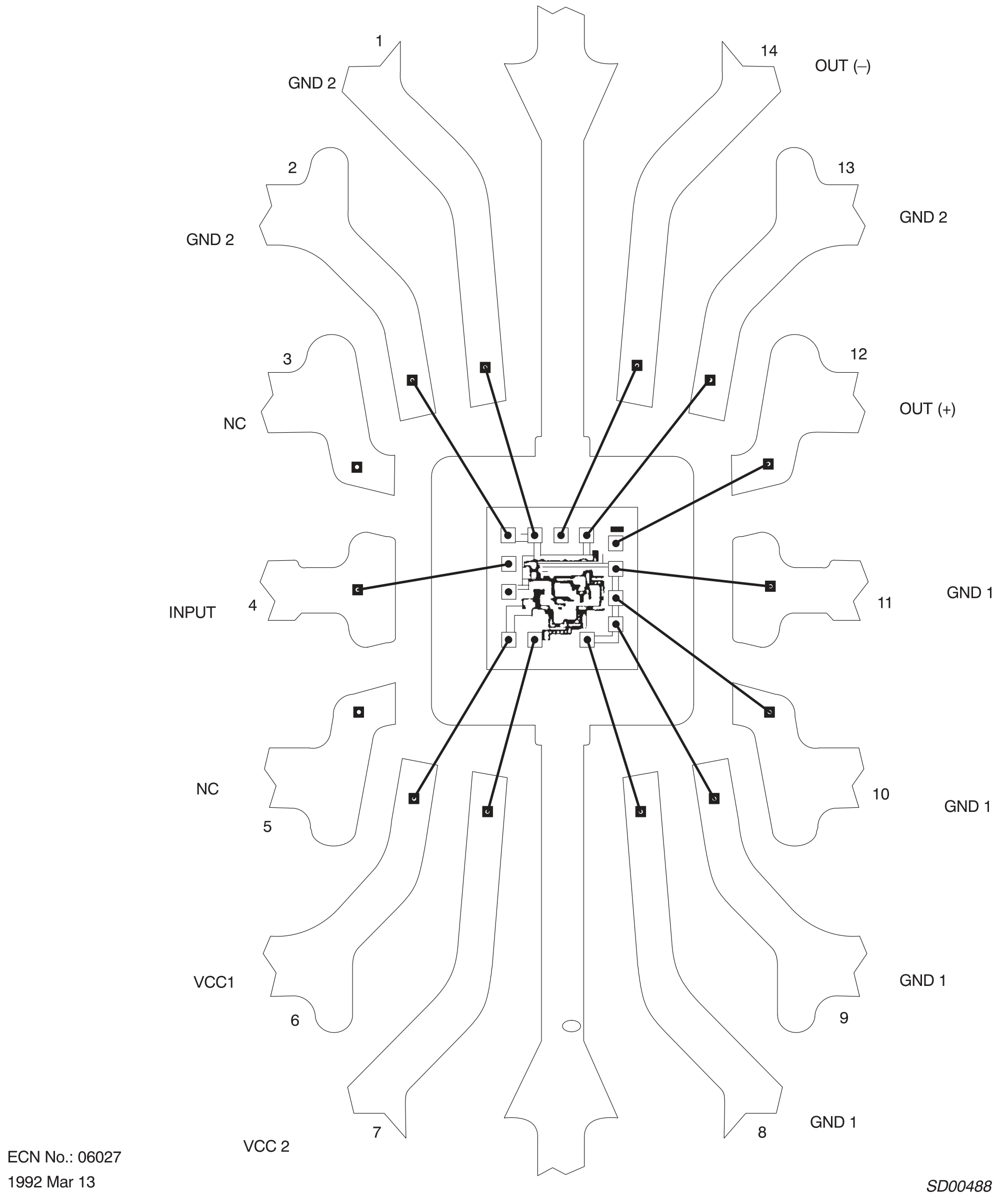


Fig 15. SA5211 Bonding diagram.

15.1 Die sales disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

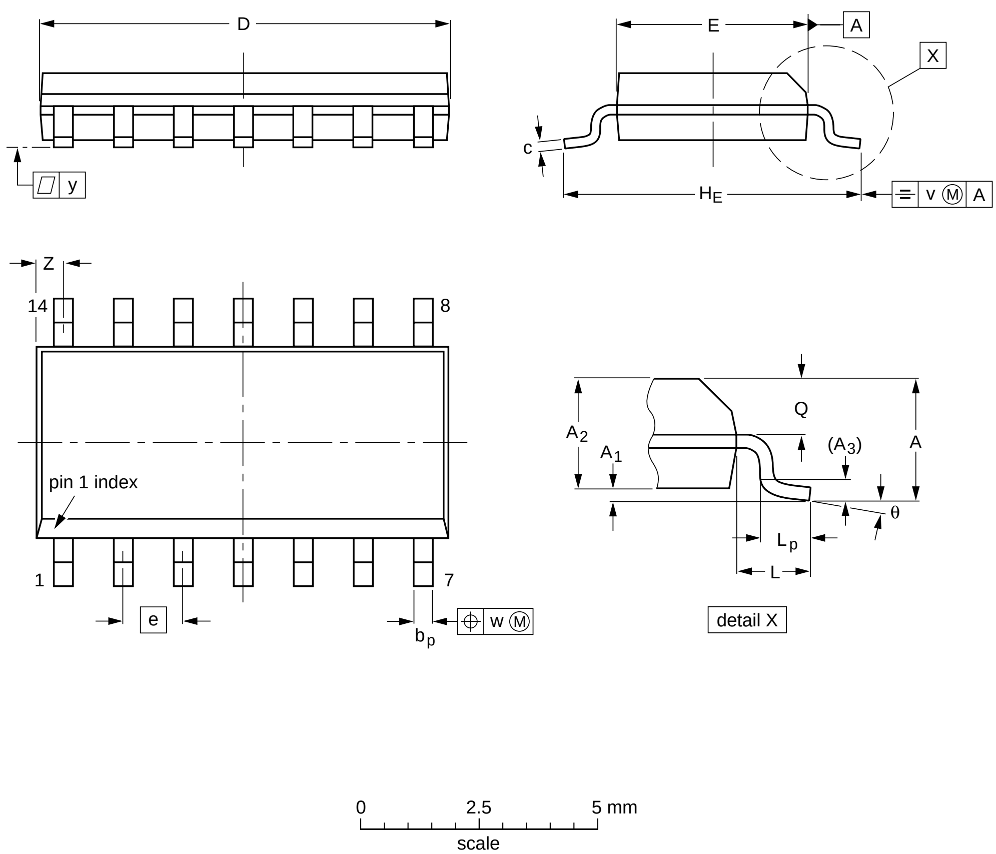
All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.

16. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

Fig 16. SOT108-1.

17. Soldering

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Package related soldering information

Table 6: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	**Reflow** [1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
03	19981007	853-1799 20142	**Product specification; third version; supersedes second version SA5211_2 of 1998 Oct 07 (9397 750 04624). Modifications:** The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard.
02	19981007	853-1799 20142	**Product specification; second version; supersedes first version SA5211_1 of 1995 Apr 26. Modifications:** Changed prefix from NE to SA.
01	19950426	853-1799 15170	**Product specification; initial version.**

19. Data sheet status

Data sheet status [1]	Product status [2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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