

IGBT Chip in NPT-technology

FEATURES:

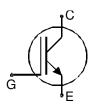
- 1200V NPT technology
- 180µm chip
- low turn-off losses
- positive temperature coefficient
- easy paralleling
- integrated gate resistor

This chip is used for:

• power module BSM100GD120DLC

Applications:

drives



Chip Type	V _{CE}	I Cn	Die Size	Package	Ordering Code
SIGC156T120R2CL	1200V	100A	12.59 X 12.59 mm ²	sawn on foil	Q67041- A4663-A003

MECHANICAL PARAMETER:

Raster size	12.59 X 12.59 mi				
Emitter pad size	8 x (3.98 x 2.38)				
Gate pad size	1.46 x 0.8				
Area total / active	158.5 / 132.6				
Thickness	180	μm			
Wafer size	150	mm			
Flat position	90	grd			
Max.possible chips per wafer	82 pcs				
Passivation frontside	Photoimide				
Emitter metallization	3200 nm Al Si 1%				
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding				
Die bond	electrically conductive glue or solder				
Wire bond	Al, <500μm				
Reject Ink Dot Size	Ø 0.65mm ; max 1.2mm				
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C				



MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Collector-emitter voltage, Tj=25 °C	V _{CE}	1200	V
DC collector current, limited by T _{jmax}	I _C	1)	А
Pulsed collector current, t_p limited by T_{jmax}	I _{cpuls}	300	А
Gate emitter voltage	V _{GE}	±20	V
Operating junction and storage temperature	T _j , T _{stg}	-55 +150	°C

¹⁾ depending on thermal properties of assembly

STATIC CHARACTERISTICS (tested on chip), T_j =25 °C, unless otherwise specified:

Parameter	Symbol	Conditions	Value			Unit
		Conditions	min.	typ.	max.	
Collector-emitter breakdown voltage	V _{(BR)CES}	V_{GE} =0V , I _C =5mA	1200			
Collector-emitter saturation voltage	V _{CE(sat)}	V _{GE} =15V, I _C =100A	1.8	2.2	2.6	V
Gate-emitter threshold voltage	$V_{\rm GE(th)}$	$I_C=4mA$, $V_{GE}=V_{CE}$	4.5	5.5	6.5	
Zero gate voltage collector current	I _{CES}	V_{CE} =1200V , V_{GE} =0V			12.2	μA
Gate-emitter leakage current	I _{GES}	V_{CE} =0V , V_{GE} =20V			600	nA
Integrated gate resistor	R _{Gint}			5		Ω

ELECTRICAL CHARACTERISTICS (tested at component):

Parameter	Symbol	Conditions	Value			Unit
Falameter	Symbol	Conditions	min.	typ.	max.	Unit
Input capacitance	Ciss	$V_{CE}=25V$,	-	6.5	-	nF
Output capacitance	Coss	$V_{\rm GE}=0V$,	-	-	-	
Reverse transfer capacitance	Crss	f=1MHz	-	0.42	-	

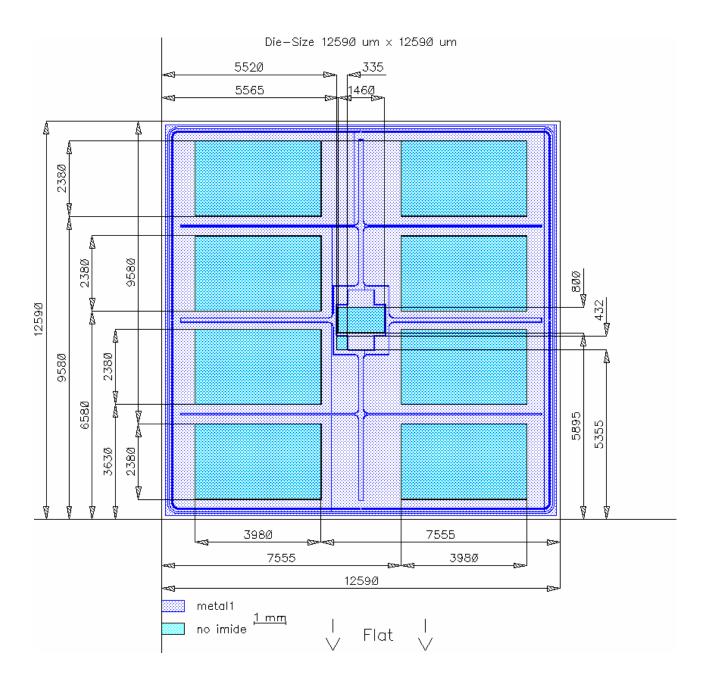
SWITCHING CHARACTERISTICS (tested at component), Inductive Load

Parameter	Symbol	Conditions ¹⁾	Value			Unit
	Cymbol	Conditions	min.	typ.	max.	onne
Turn-on delay time	t _{d(on)}	$T_{\rm j} = 125^{\circ}{\rm C}$	-	60	-	ns
Rise time	<i>t</i> r	V _{CC} =600V, / _C =100A,	-	50	-	
Turn-off delay time	$t_{d(off)}$	$V_{\text{GE}} = \pm 15 \text{V},$	-	400	-	
Fall time	t _f	$R_{\rm G}$ =5.6 Ω	-	80	-	

¹⁾ values also influenced by parasitic L- and C- in measurement and package.



CHIP DRAWING:





FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the
device data sheet

BSM100GD120DLC

Package Econopack 3

DESCRIPTION:

AQL 0,65 for visual inspection according to failure catalog

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

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