10 W (40 dBm), 0.01 GHz to 2.8 GHz, GaN Power Amplifier

Data Sheet **HMC8500PM5E**

FEATURES

- High small signal gain: 15.0 dB typical
- P_{OUT}: 40 dBm typical at P_{IN} = 30 dBm
- High PAE: 55% typical at P_{IN} = 30 dBm
- Frequency range: 0.01 GHz to 2.8 GHz across all frequencies
- V_{DD} = 28 V at quiescent current of 100 mA
- Internal prematching
  - Simple and compact external tuning for optimal performance
- 5 mm × 5 mm, 32-lead LFCSP package

APPLICATIONS

- Extended battery operation for public mobile radios
- Power amplifier stage for wireless infrastructures
- Test and measurement equipment
- Commercial and military radars
- General-purpose transmitter amplification

FUNCTIONAL BLOCK DIAGRAM

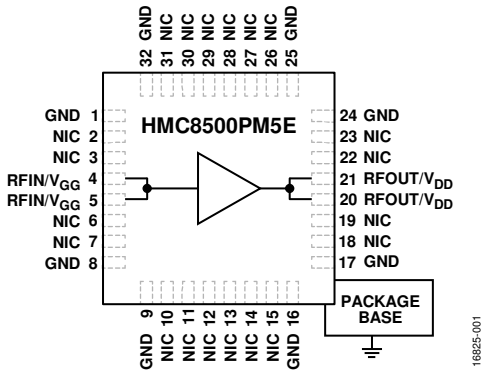

Figure 1.

GENERAL DESCRIPTION

The HMC8500PM5E is a gallium nitride (GaN), broadband power amplifier delivering 10 W (40 dBm), typical, with up to 55% power added efficiency (PAE) across an instantaneous bandwidth of 0.01 GHz to 2.8 GHz, at an input power of 30 dBm. The typical gain flatness is 3 dB at small signal levels.

The HMC8500PM5E is ideal for pulsed or continuous wave (CW) applications, such as wireless infrastructure, radars, public mobile radios, and general-purpose amplification.

The HMC8500PM5E amplifier is externally tuned using low cost, surface-mount components and is available in a compact LFCSP package.

Note that, throughout this data sheet, multifunction pins, such as RFIN/V_{GG}, are referred to either by the entire pin name or by a single function of the pin, for example, RFIN, when only that function is relevant.

Rev. A

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REVISION HISTORY

9/2018—Rev. 0 to Rev. A

Changes to Storage Temperature Range Parameter, Table 4 5

7/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, supply voltage (V_{DD}) = 28 V, quiescent current (I_{DDQ}) = 100 mA, and frequency range = 0.01 GHz to 1.3 GHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		1.3	GHz	
GAIN						
Small Signal Gain		14.0	20.0		dB	
Gain Flatness			6		dB	
RETURN LOSS						
Input			7		dB	
Output			7		dB	
POWER						
Output Power	P_{OUT}		40		dBm	Input power (P_{IN}) = 28 dBm
			40		dBm	P_{IN} = 30 dBm
Power Added Efficiency	PAE		55		%	P_{IN} = 28 dBm
			55		%	P_{IN} = 30 dBm
OUTPUT THIRD-ORDER INTERCEPT	OIP3		47		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE	NF		7		dB	
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust the gate bias control voltage (V_{GG}) from −8 V to 0 V to achieve I_{DDQ} = 100 mA, V_{GG} = −2.65 V typical to achieve I_{DDQ} = 100 mA
SUPPLY VOLTAGE	V_{DD}	24	28	32	V	

T_A = 25°C, V_{DD} = 28 V, I_{DDQ} = 100 mA, and frequency range = 1.3 GHz to 2.8 GHz.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		1.3		2.8	GHz	
GAIN						
Small Signal Gain		12.0	15.0		dB	
Gain Flatness			3		dB	
RETURN LOSS						
Input			9		dB	
Output			9		dB	
POWER						
Output Power	P_{OUT}		39		dBm	P_{IN} = 28 dBm
			40		dBm	P_{IN} = 30 dBm
Power Added Efficiency	PAE		40		%	P_{IN} = 28 dBm
			47		%	P_{IN} = 30 dBm
OUTPUT THIRD-ORDER INTERCEPT	OIP3		47		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE	NF		4.5		dB	
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust the gate bias control voltage (V_{GG}) from −8 V to 0 V to achieve I_{DDQ} = 100 mA, V_{GG} = −2.65 V typical to achieve I_{DDQ} = 100 mA
SUPPLY VOLTAGE	V_{DD}	24	28	32	V	

TOTAL SUPPLY CURRENT BY V_{DD}

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
QUIESCENT CURRENT	I_{DDQ}					Adjust the gate bias control voltage (V_{GG}) between −8 V and 0 V to achieve I_{DDQ} = 100 mA typical
			100		mA	V_{DD} = 24 V
			100		mA	V_{DD} = 28 V
			100		mA	V_{DD} = 32 V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Supply Bias Voltage (V_{DD})	35 V
Gate Bias Voltage (V_{GG})	−8 V to 0 V dc
Radio Frequency (RF) Input Power (RFIN)	33 dBm
Maximum Voltage Standing Wave Ratio (VSWR)[2]	6:1
Channel Temperature	225°C
Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3 (MSL3))[3]	260°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 147.0 mW/°C Above 85°C)	20.6 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model	Class 1B, passed 500 V

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the absolute maximum rating is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] Restricted by maximum power dissipation.
[3] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CG-32-2[1]	6.8	°C/W

[1] Thermal resistance (θ_{JC}) determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground pad to the PCB. The ground pad is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

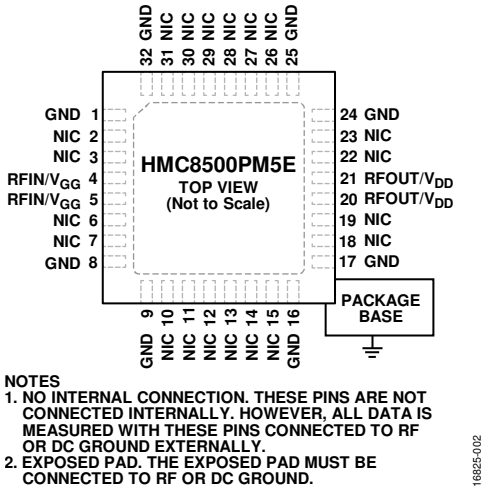

Figure 2. Pin Configuration

Table 6. Pad Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. These pins must be connected to RF or dc ground. See Figure 3 for the GND interface schematic.
2, 3, 6, 7, 10 to 15, 18, 19, 22, 23, 26 to 31	NIC	No Internal Connection. These pins are not connected internally. However, all data is measured with these pins connected to RF or dc ground externally.
4, 5	RFIN/V_{GG}	RF Input/Gate Bias Control Voltage. This pin is a multifunction pin. The RFIN/V_{GG} pin is dc-coupled with internal prematching and requires external matching to 50 Ω, as shown in Figure 44. See Figure 4 for the RFIN/V_{GG} interface schematic.
20, 21	RFOUT/V_{DD}	RF Output/Drain Bias Voltage. This is a multifunction pin. The RFOUT/V_{DD} pin is dc-coupled and requires external matching to 50 Ω, as shown in Figure 44. See Figure 4 for the RFOUT/V_{DD} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

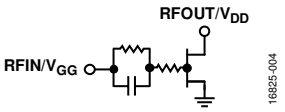

Figure 4. RFIN/V_{GG} and RFOUT/V_{DD} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

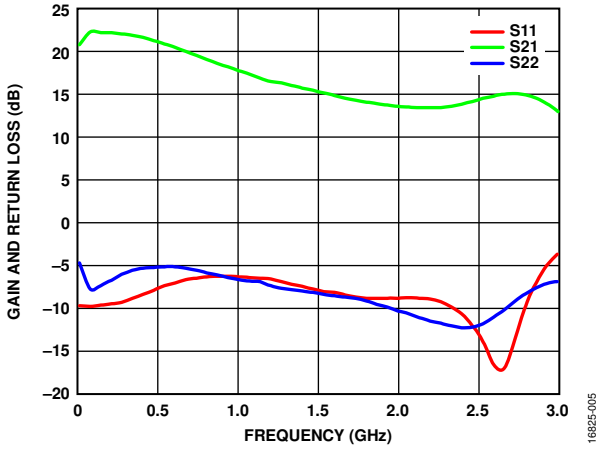

Figure 5. Gain and Return Loss vs. Frequency

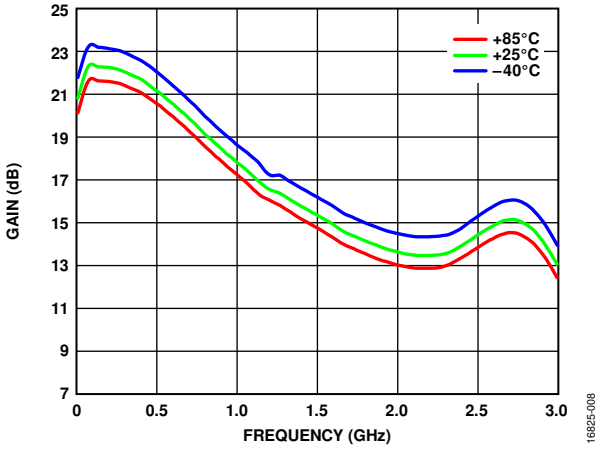

Figure 8. Gain vs. Frequency at Various Temperatures

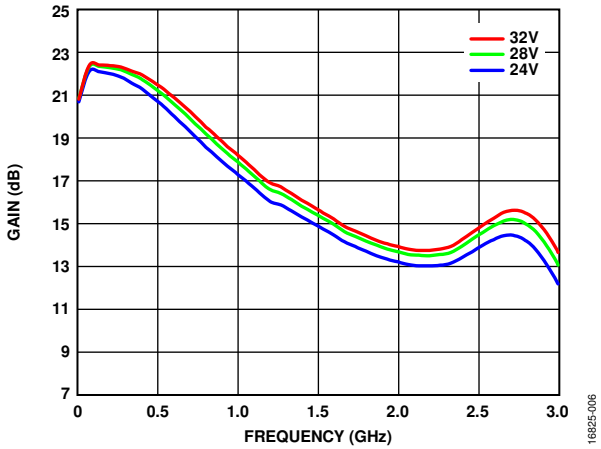

Figure 6. Gain vs. Frequency at Various Supply Voltages

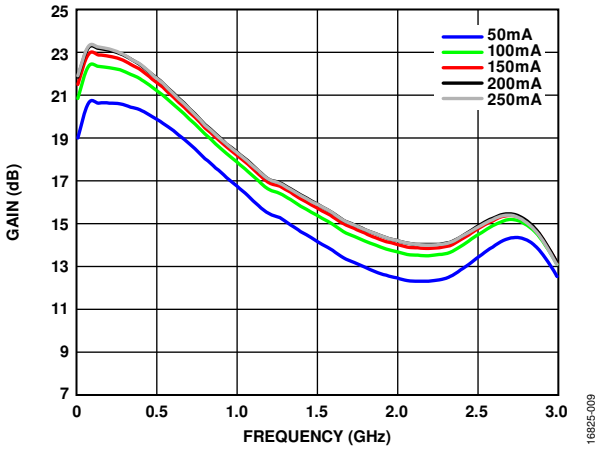

Figure 9. Gain vs. Frequency at Various Quiescent Currents

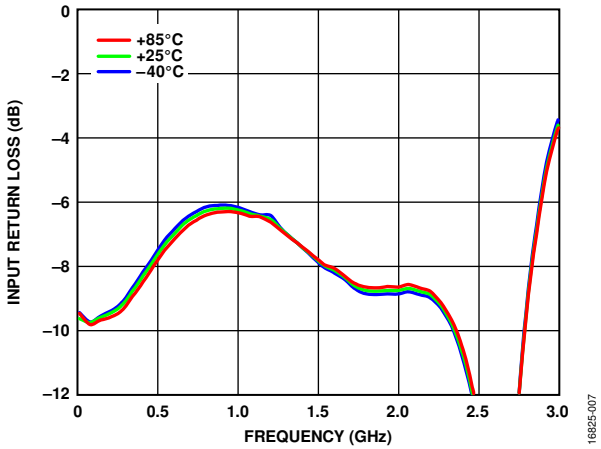

Figure 7. Input Return Loss vs. Frequency at Various Temperatures

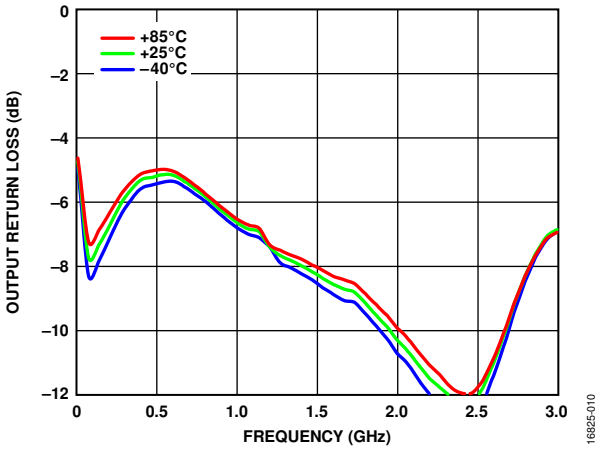

Figure 10. Output Return Loss vs. Frequency at Various Temperatures

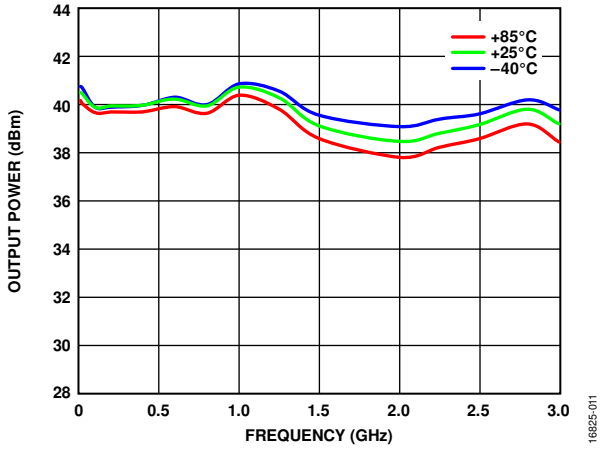

Figure 11. Output Power vs. Frequency at Various Temperatures, Input Power = 28 dBm

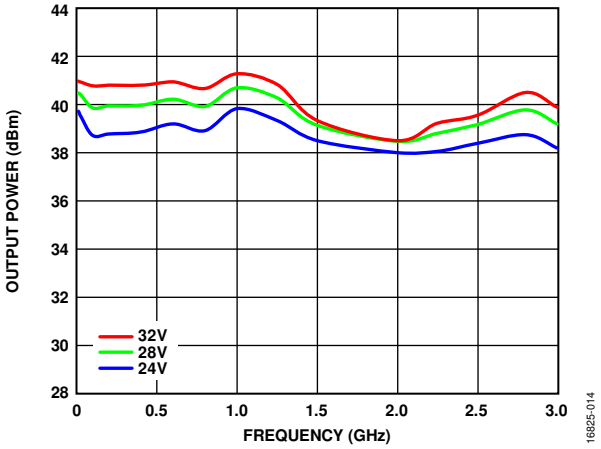

Figure 14. Output Power vs. Frequency at Various Supply Voltages, Input Power = 28 dBm

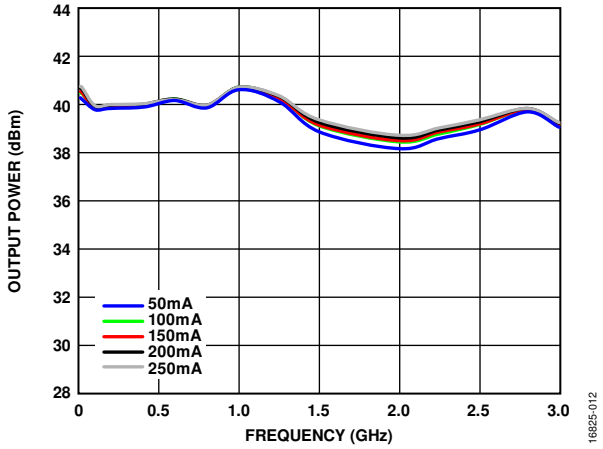

Figure 12. Output Power vs. Frequency at Various Quiescent Currents, Input Power = 28 dBm

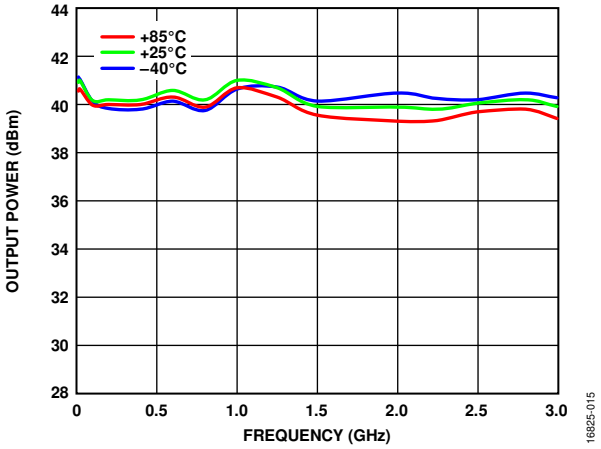

Figure 15. Output Power vs. Frequency at Various Temperatures, Input Power = 30 dBm

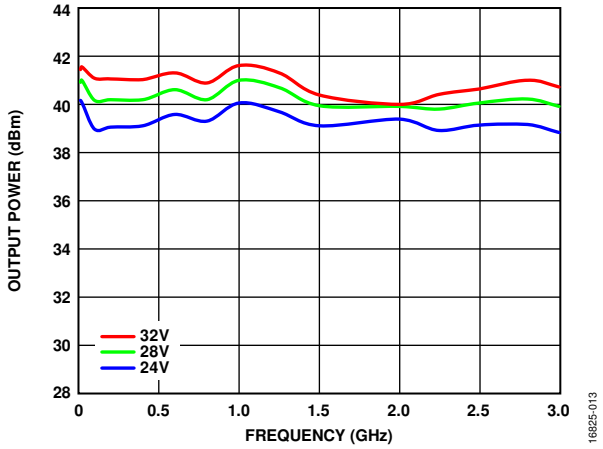

Figure 13. Output Power vs. Frequency at Various Supply Voltages, Input Power = 30 dBm

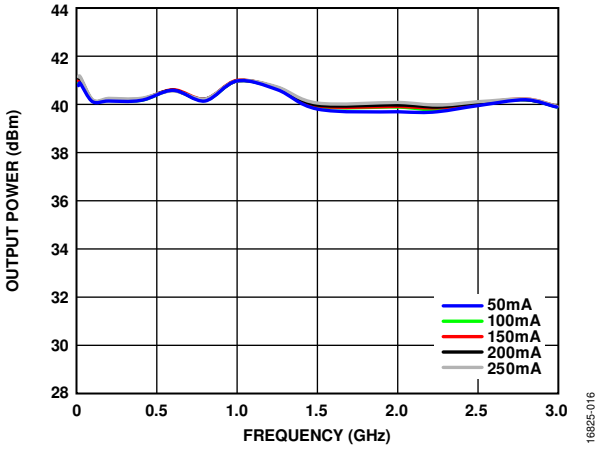

Figure 16. Output Power vs. Frequency at Various Quiescent Currents, Input Power = 30 dBm

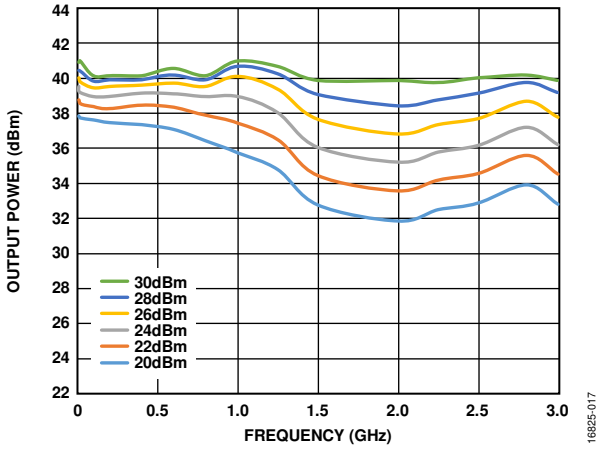

Figure 17. Output Power vs. Frequency at Various Input Powers

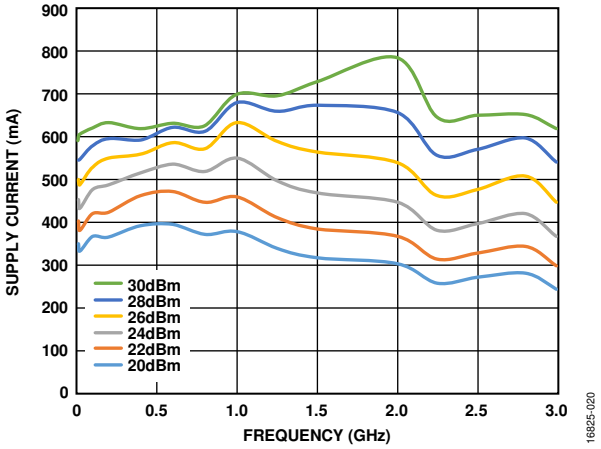

Figure 20. Supply Current vs. Frequency at Various Input Powers

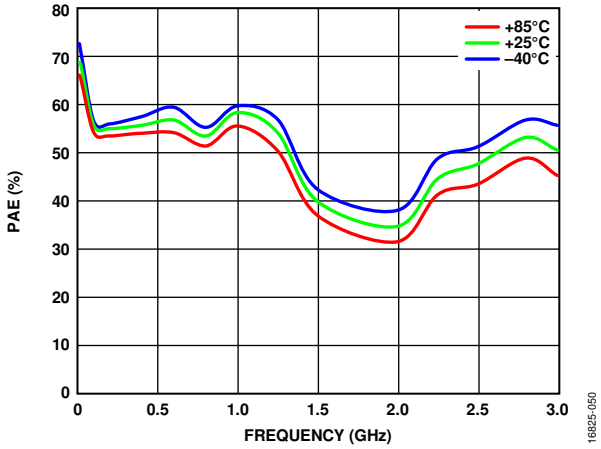

Figure 18. PAE vs. Frequency at Various Temperatures, Input Power = 28 dBm

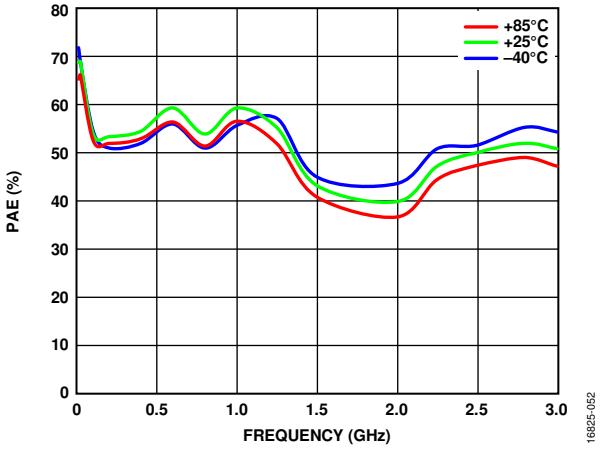

Figure 21. PAE vs. Frequency at Various Temperatures, Input Power = 30 dBm

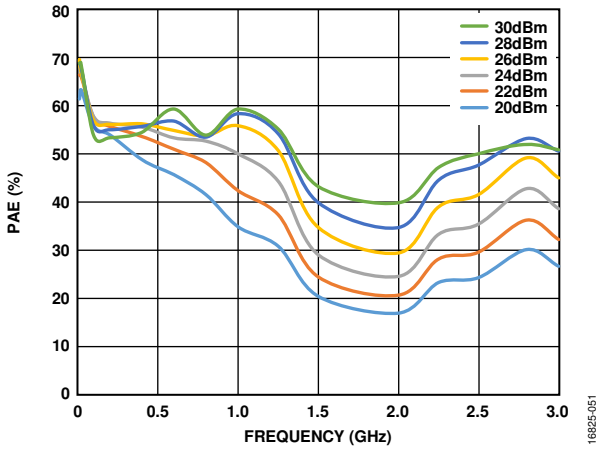

Figure 19. PAE vs. Frequency at Various Input Powers

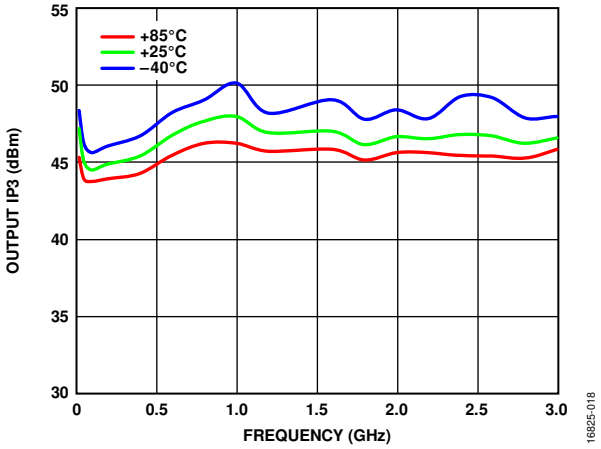

Figure 22. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 30 dBm

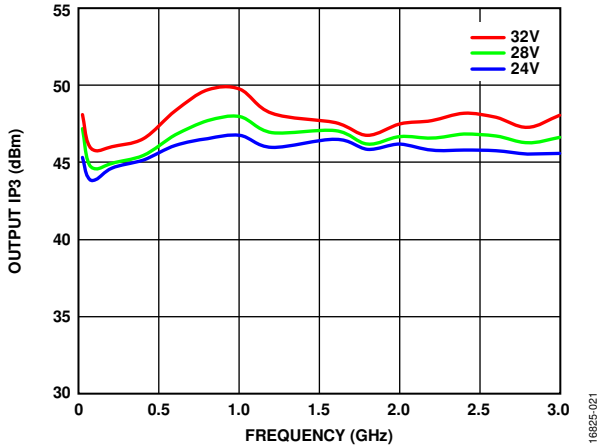

Figure 23. Output IP3 vs. Frequency at Various Supply Voltages, P_{OUT} per Tone = 30 dBm

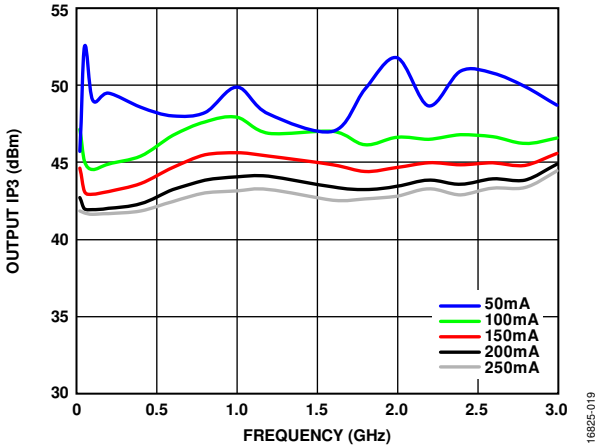

Figure 26. Output IP3 vs. Frequency at Various Quiescent Currents, P_{OUT} per Tone = 30 dBm

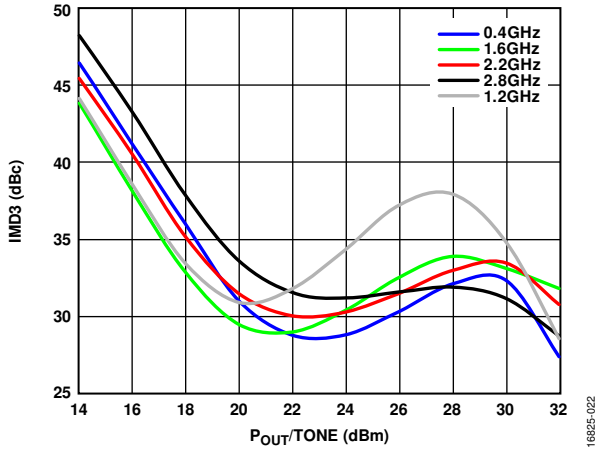

Figure 24. Output Third-Order Intermodulation (IMD3) vs. P_{OUT} per Tone, V_{DD} = 24 V

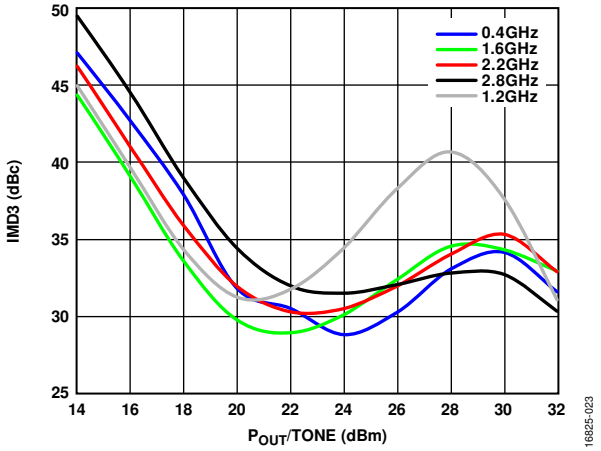

Figure 27. IMD3 vs. P_{OUT} per Tone, V_{DD} = 28 V

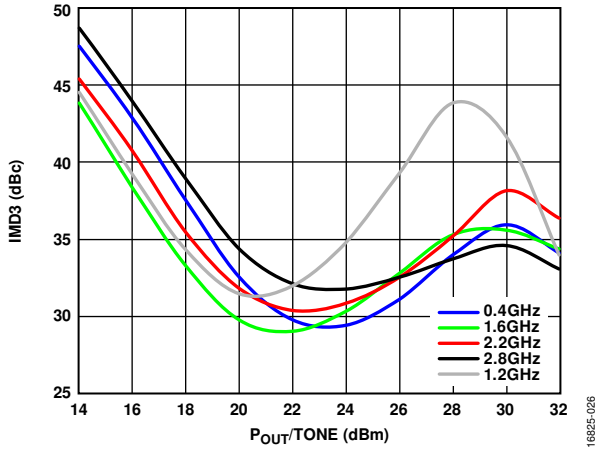

Figure 25. IMD3 vs. P_{OUT} per Tone, V_{DD} = 32 V

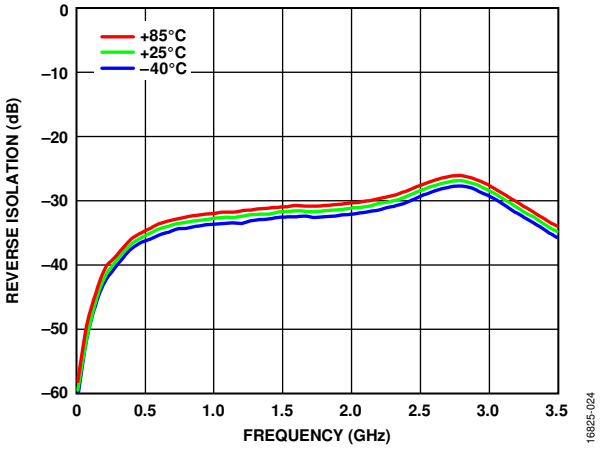

Figure 28. Reverse Isolation vs. Frequency at Various Temperatures

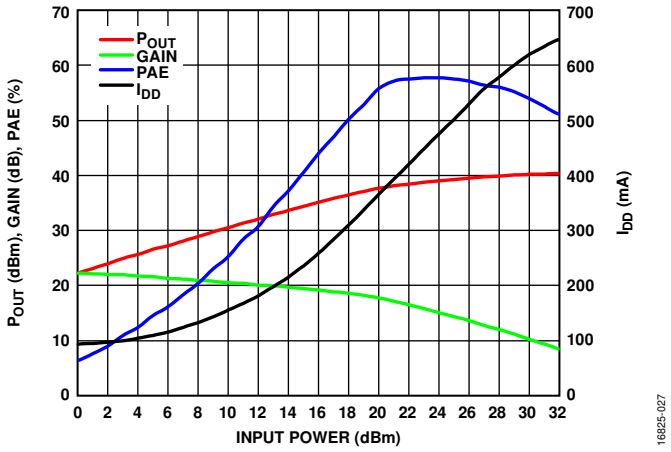

Figure 29. P_{OUT}, Gain, PAE, and Total Supply Current (I_{DD}) vs. Input Power at 0.1 GHz

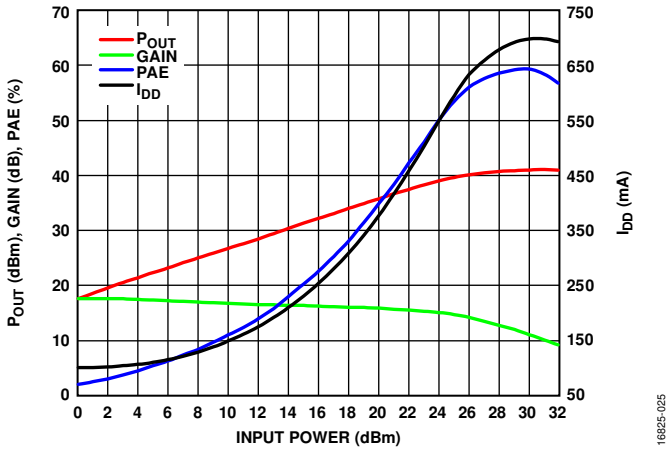

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 1 GHz

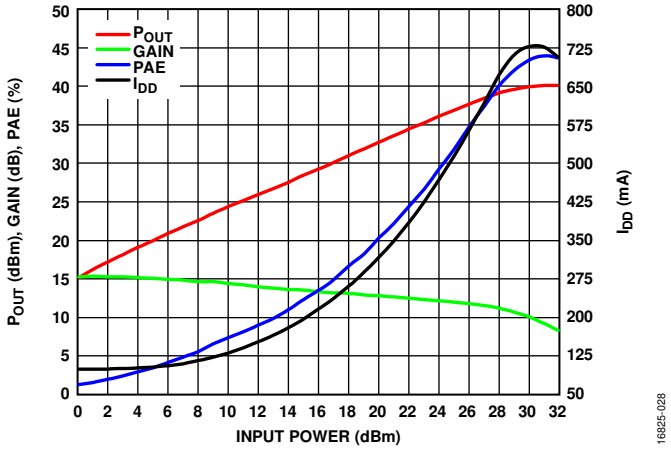

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 1.5 GHz

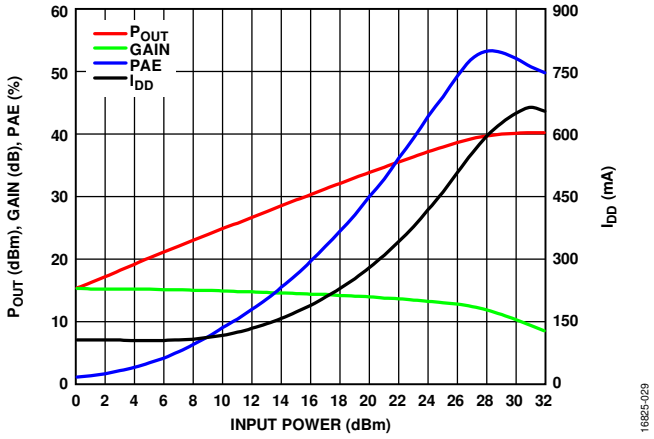

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 2.8 GHz

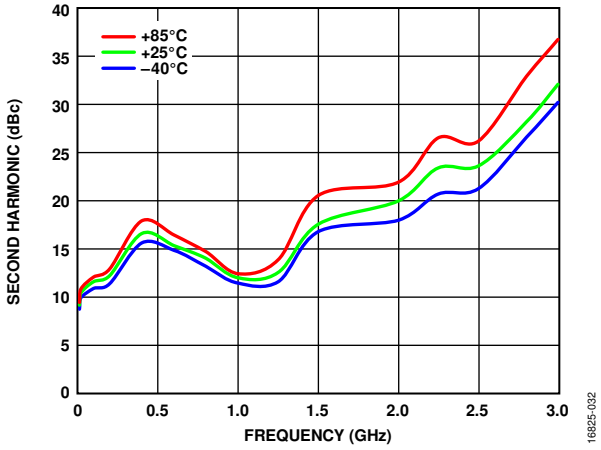

Figure 31. Second Harmonic vs. Frequency at Various Temperatures, Input Power = 15 dBm

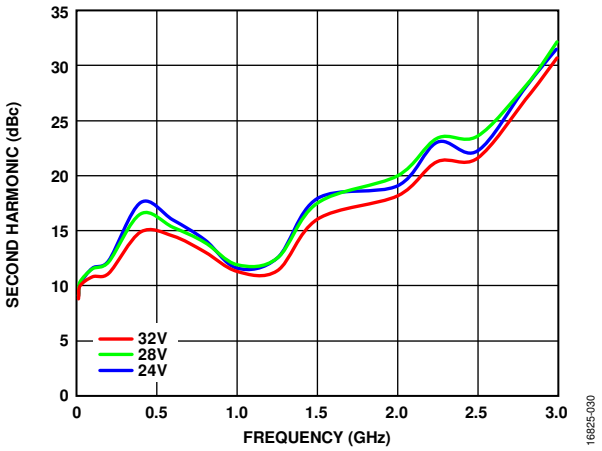

Figure 34. Second Harmonic vs. Frequency at Various Supply Voltages, Input Power = 15 dBm

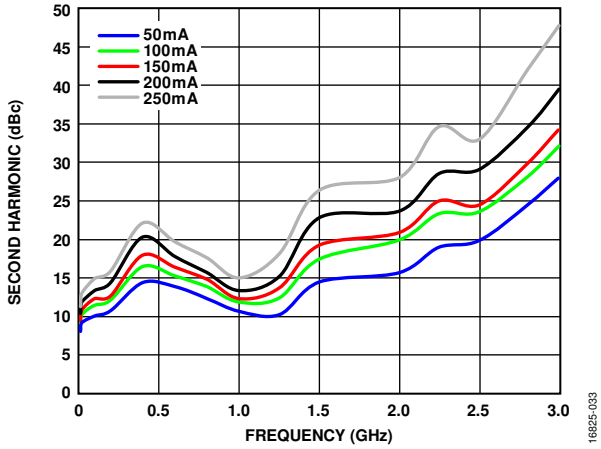

Figure 35. Second Harmonic vs. Frequency at Various Quiescent Currents, Input Power = 15 dBm

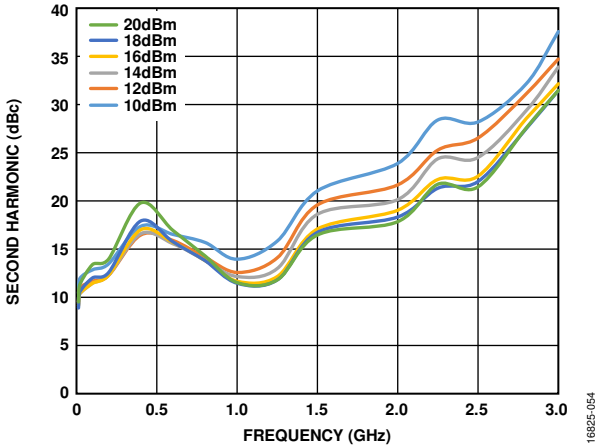

Figure 38. Second Harmonic vs. Frequency at Various Input Powers, 10 dBm to 20 dBm

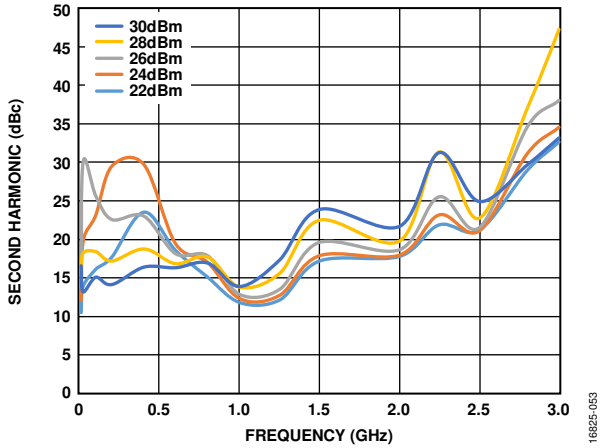

Figure 36. Second Harmonic vs. Frequency at Various Input Powers, 22 dBm to 30 dBm

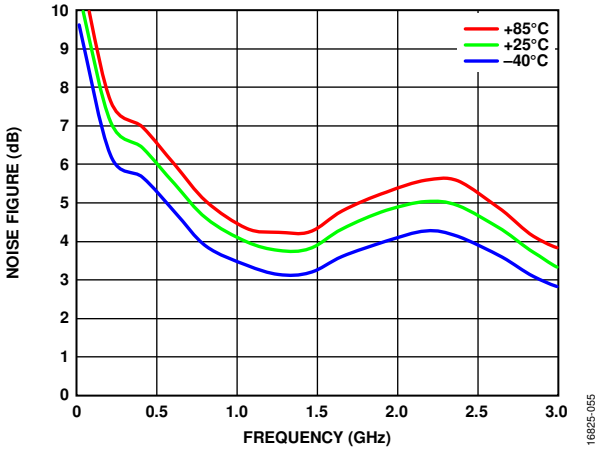

Figure 39. Noise Figure vs. Frequency at Various Temperatures

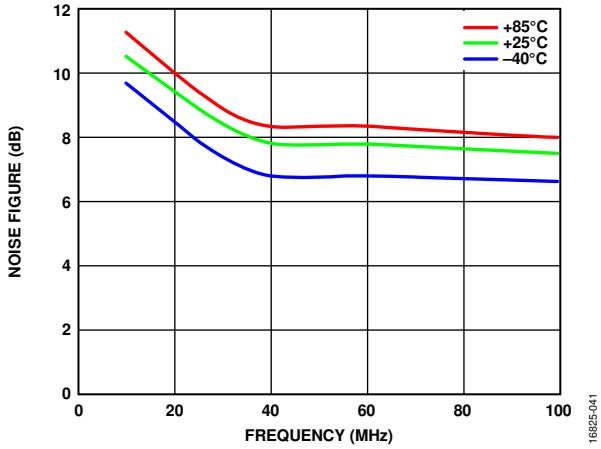

Figure 37. Noise Figure vs. Frequency at Various Temperatures, Low Frequency

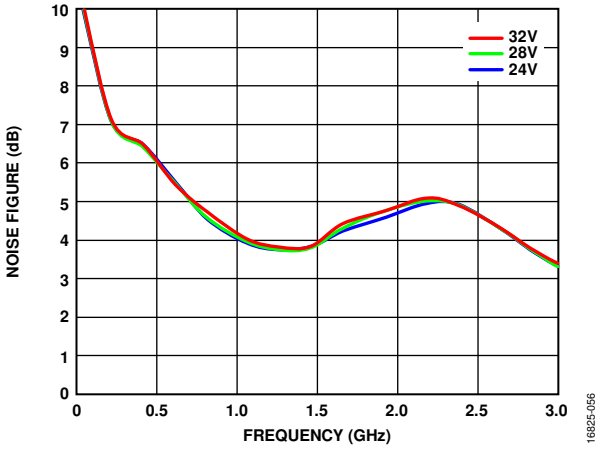

Figure 40. Noise Figure vs. Frequency at Various Supply Voltages

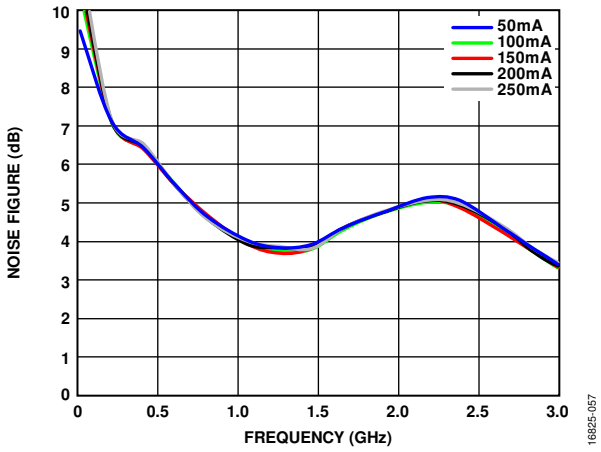

Figure 41. Noise Figure vs. Frequency at Various Quiescent Currents

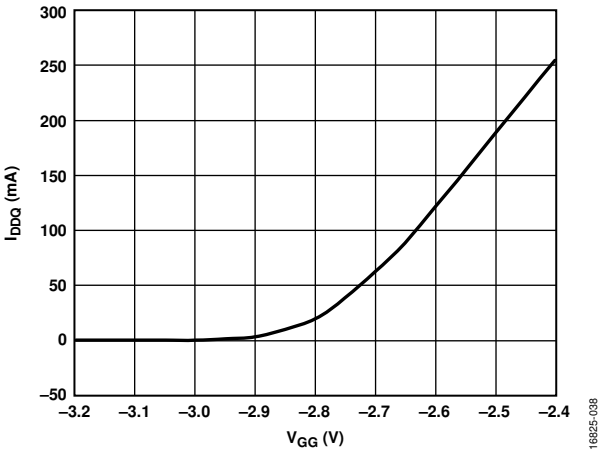

Figure 43. I_{DDQ} vs. V_{GG} at V_{DD} = 28 V, Representative of a Typical Device

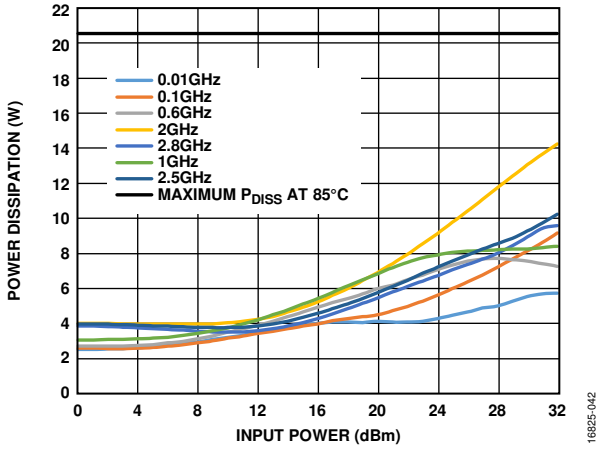

Figure 42. Power Dissipation vs. Input Power at Various Frequencies, T_A = 85°C

THEORY OF OPERATION

The HMC8500PM5E is a 10 W (40 dBm), gallium nitride (GaN), power amplifier that consists of a single gain stage that operates like a single field effect transistor (FET). The device is internally prematched so that simple, external matching networks at the RF input and RF output ports optimize the performance across the entire operating frequency range. The recommended dc bias conditions place the device in Class AB operation, resulting in high output power (40 dBm typical at P_{IN} = 30 dBm) at improved levels of power efficiency (55% typical at P_{IN} = 30 dBm).

APPLICATIONS INFORMATION

The drain bias voltage is applied through the RFOUT/V_{DD} pin, and the gate bias voltage is applied through the RFIN/V_{GG} pin. For operation of a single application circuit across the entire frequency range, it is recommended to use the external matching components specified in the typical application circuit (L1, C1, C8, C11, and R2) shown in Figure 44. If operation is only required across a narrower frequency range, performance can be optimized additionally through the implementation of alternate matching networks. Capacitive bypassing of V_{DD} and V_{GG} is recommended.

The recommended power-up bias sequence is as follows:

1. Connect the power supply ground to circuit ground.
2. Set V_{GG} to −8 V to pinch off the drain current. Set V_{DD} to 28 V (drain current is pinched off). Adjust V_{GG} between −3 V and −2.5 V until a quiescent current of I_{DDQ} = 100 mA is obtained.
3. Apply the RF signal.

The recommended power-down bias sequence is as follows:

1. Turn off the RF signal.
2. Set V_{GG} to −8 V to pinch off the drain current.
3. Set V_{DD} to 0 V.
4. Set V_{GG} to 0 V.

All measurements for this device were taken using the typical application circuit, configured as shown in the assembly diagram (see Figure 44). The bias conditions shown in the electrical specifications tables (see Table 1 and Table 2) are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC8500PM5E under other bias conditions may cause performance that differs from that shown in the Typical Performance Characteristics section.

The evaluation PCB provides the HMC8500PM5E in the typical application circuit, allowing easy operation using standard dc power supplies and 50 Ω RF test equipment.

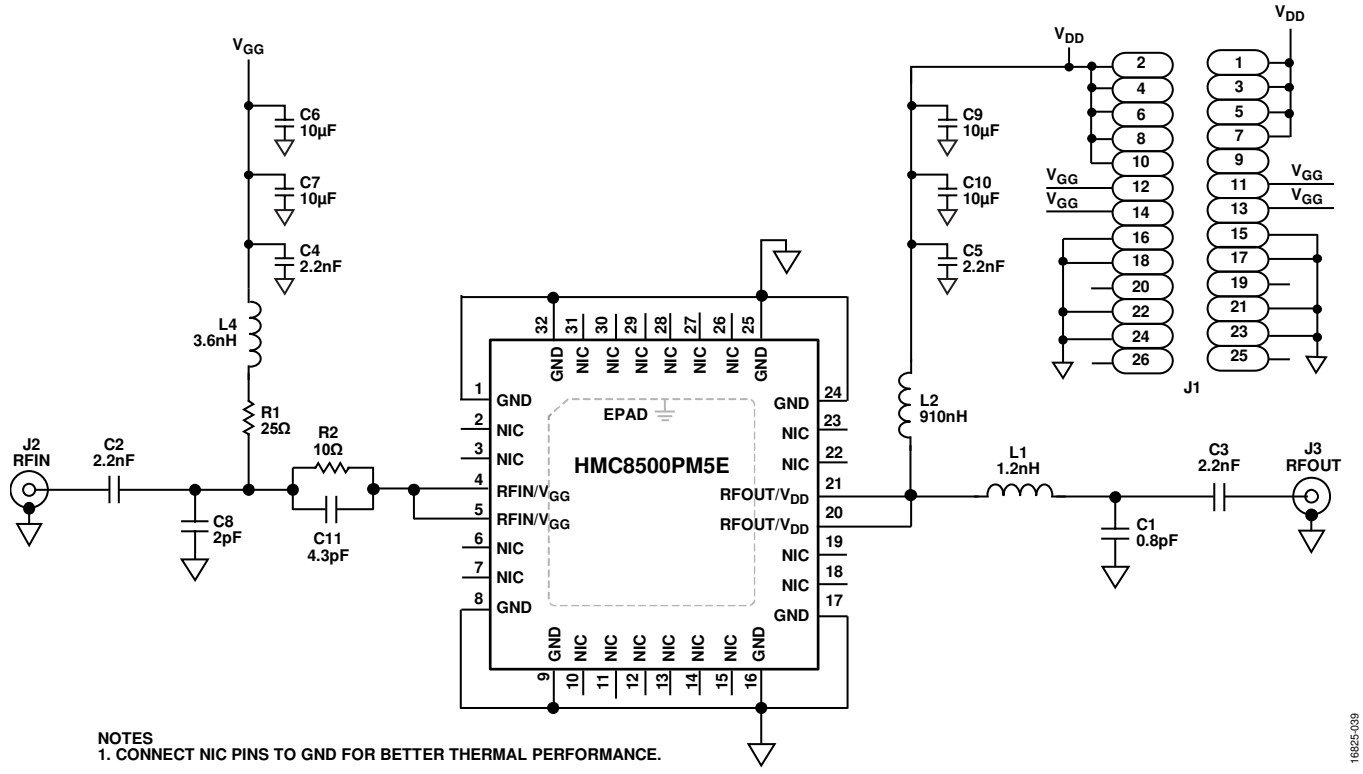

Figure 44. Typical Application Circuit

EVALUATION BOARD

The HMC8500PM5E evaluation board is a 2-layer board fabricated with Rogers 4350 material and using layout techniques recommended for high frequency RF designs. The RF input and RF output traces have a 50 Ω characteristic impedance. The board is attached to a heat sink using an electrically and thermally conductive epoxy, providing a low thermal and low dc resistance path. Components are mounted using SN63 solder, allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation board and populated components are designed to operate over the ambient temperature range of −40°C to +85°C. During operation, attach the evaluation board to a temperature controlled plate to control the temperature of the HMC8500PM5E during operation. For the proper bias sequence, see the Applications Information section.

A fully populated and tested evaluation board, shown in Figure 45, is available from Analog Devices, Inc., upon request.

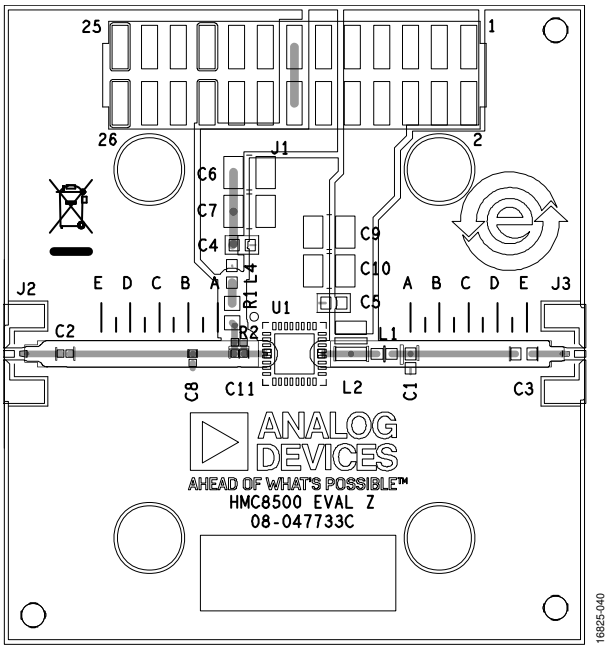

Figure 45. Evaluation PCB

Table 7. Bill of Materials for Evaluation PCB EV1HMC8500PM5

Item	Description	Manufacturer/Part Number
J2, J3	K connectors	SRI/25-146-1000-92
J1	Preform surface terminal strip	SAMTEC/TSM-113-01-L-DV
C1	0.8 pF capacitor, 0402 package	Murata/GRM1555C1HR80BA01D
C2	2.2 nF capacitor, 0402 package	Samsung/CL05B222KB5NNNC
C3, C4, C5	2.2 nF capacitors, 0603 package	TDK/C1608C0G1H222J
C6, C7, C9, C10	10 µF capacitors, 1210-2 package	TDK/C3225X7S1H106K250AB
C8	2 pF capacitor, 0402 package	AVX/04023U2R0BAT2A
C11	4.3 pF capacitor, 0402 package	Murata/GJM1552C1H4R3BB01C
L1	1.2 nH inductor, 0402 package	TDK/MHQ1005P1N2CT000
L2	910 nH inductor, 1008CS package	Coilcraft/1008CS-911XGLB
L4	3.6 nH inductor, 0603 package	Coilcraft/0603CS-3N6XGLU
R1	25 Ω high precision resistor, 0603 package	Vishay/P0603E25R0BNT
R2	10 Ω resistor, 0402 package	Panasonic/ERJ-2RKF10R0X
Heat Sink	Used for thermal transfer from the HMC8500PM5E amplifier	Not applicable
U1	HMC8500PM5E amplifier	Analog Devices/HMC8500PM5E
PCB	EV1HMC8500PM5 circuit board material: Rogers 4350	Analog Devices/EV1HMC8500PM5

OUTLINE DIMENSIONS

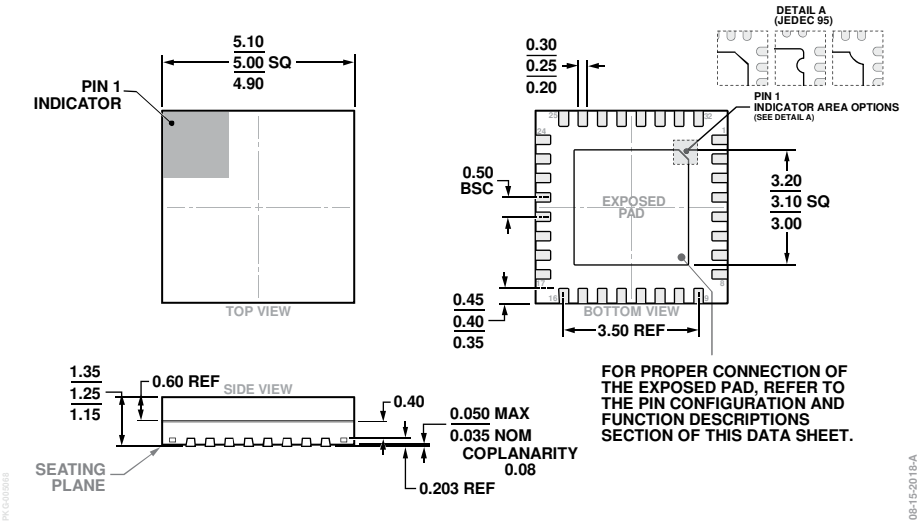

Figure 46. 32-Lead Lead Frame Chip Scale Package [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description[4]	Package Option
HMC8500PM5E	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP_CAV]	CG-32-2
HMC8500PM5ETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP_CAV]	CG-32-2
EV1HMC8500PM5			Evaluation Board	

[1] All models are RoHS compliant.
[2] When ordering the evaluation board, use the reference model number, EV1HMC8500PM5.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC8500PM5E and the HMC8500PM5ETR is nickel palladium gold (NiPdAu).