MP3437

16V$_{OUT}$, 9.5A, High-Efficiency, Fully Integrated, Synchronous Boost Converter

DESCRIPTION

The MP3437 is a 600kHz, fixed-frequency, highly integrated, synchronous boost converter with a wide input range. The MP3437's input voltage starts as low as 2.7V and supports up to 20W of load power from a 1-cell battery with integrated low $R_{DS(ON)}$ power MOSFETs.

The MP3437 utilizes a constant-off-time (COT) control topology, which provides fast transient response. The QFN package has a MODE pin that supports the selection of pulse-skip mode (PSM), forced continuous conduction mode (FCCM), and ultrasonic mode (USM) under light-load conditions. The cycle-by-cycle current limit on the low-side MOSFET (LS-FET) prevents current runaway, and the high-side MOSFET (HS-FET) eliminates the need for an external Schottky diode.

The MP3437 supports automatic pass-through mode when the input voltage (V_{IN}) is greater than the set output voltage (V_{OUT_SET}) in PSM. Full protection features include programmable input under-voltage lockout (UVLO) protection and over-temperature protection (OTP).

The MP3437 is available in a QFN-10 (2mmx2.5mm) package and a TSOT23-8 package.

FEATURES

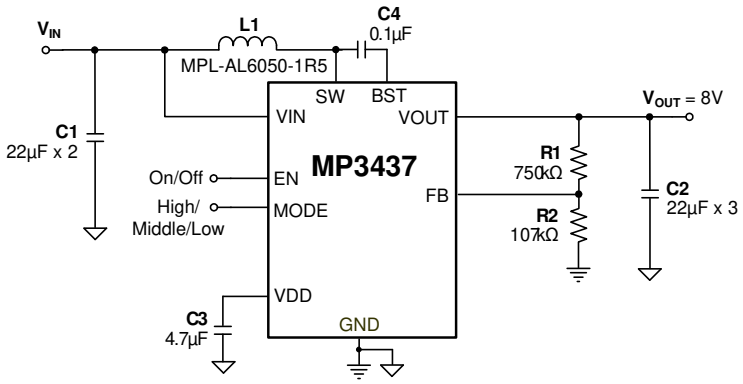
- 2.7V to 16V Start-Up Voltage
- 0.8V to 16V Operation Voltage
- Up to 16V Output Voltage
- Supports 20W Power Load from 3.3V
- 9.5A Internal Switch Current Limit
- Integrated 14mΩ and 21mΩ MOSFETs
- >90% Efficiency for 3.3V V_{IN} to 8V/2.5A
- Automatic Pass-Through Function in Pulse-Skip Mode (PSM)
- 600kHz Fixed Switching Frequency
- Adaptive Constant-Off-Time (COT) Control for Fast Transient Response
- Internal Soft Start (SS) and Compensation
- 150°C Over-Temperature Protection (OTP)
- Over-Voltage Protection (OVP)
- Available in QFN-10 (2mmx2.5mm) and TSOT23-8 Packages

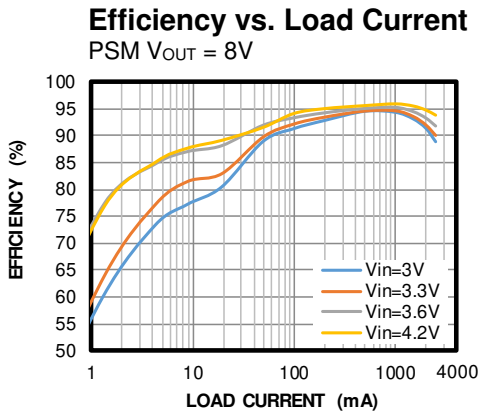
MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

APPLICATIONS

- Notebooks
- Artificial Intelligence (AI) Speakers
- Bluetooth Speakers
- Portable Point-of-Sale (POS) Systems
- Solid State Drive (SSD) VPP Rails
- Power Meters

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP3437GRP*	QFN-10 (2mmx2.5mm)	*See Below*	1
MP3437GJ**	TSOT23-8		

* For Tape & Reel, add suffix –Z (e.g. MP3437GRP–Z).
** For Tape & Reel, add suffix –Z (e.g. MP3437GJ–Z).

TOP MARKING (MP3437GRP)

JDY
LLL

JD: Product code
Y: Year code
LLL: Lot number

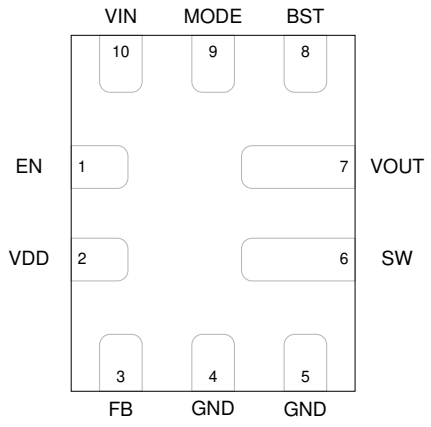
TOP MARKING (MP3437GJ)

BGZY

BGZ: Product code
Y: Year code

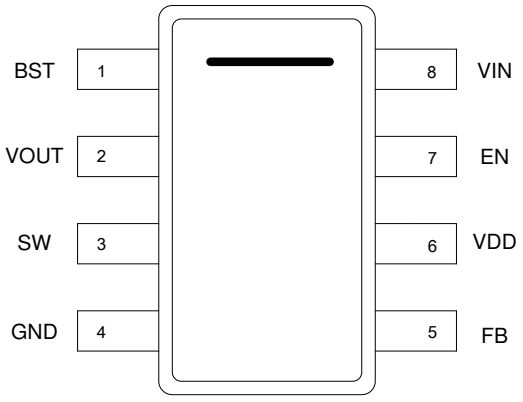
PACKAGE REFERENCE

TOP VIEW



QFN-10 (2mmx2.5mm)

TOP VIEW



TSOT23-8

PIN FUNCTIONS

QFN-10 Pin #	TSOT23-8 Pin #	Name	Description
1	7	EN	**Chip enable control.** Connect the EN pin to the VIN pin for automatic start-up. The EN pin programs VIN's under-voltage lockout (UVLO). Do not float the EN pin. This pin must be pulled up or down externally.
2	6	VDD	**Internal bias supply.** Decouple the VDD pin by placing a 4.7μF ceramic capacitor as close to this pin as possible. When V_{IN} is above 3.4V, VDD is powered by the VIN pin. Otherwise, VDD is powered by either V_{IN} or V_{OUT}, whichever voltage is greater. If the bias voltage connected to VDD is above 3.4V, the regulator from VIN to VOUT is disabled. If EN's voltage is high, the VDD regulator starts up when V_{IN} exceeds 0.95V. Supply the VIN pin with a power source above 2.7V during start-up to provide enough voltage to VDD.
3	5	FB	**Feedback input.** Connect a resistor divider from the VOUT pin to the FB pin.
4, 5	4	GND	**Power ground.** It is recommended to connect the analog signal close to GND pin-4.
6	3	SW	**Converter switch pin.** The SW pin is connected to the drain of the internal low-side power MOSFET (LS-FET) and the source of the internal synchronous high-side MOSFET (HS-FET). Connect the power inductor to SW.
7	2	VOUT	**Output pin.** The VOUT pin is connected to the drain of the HS-FET. This pin powers the VDD pin when V_{OUT} is above V_{IN} and V_{IN} is below 3.4V.
8	1	BST	**Bootstrap.** A capacitor between the BST and SW pins powers the synchronous HS-FET.
9	-	MODE	**MODE selection pin in QFN package.** The MP3437 works in pulse-skip mode (PSM) when the MODE pin is floating, and works in forced continuous conduction mode (FCCM) if the MODE pin is high.
10	8	VIN	**Input supply.** The VIN pin must be bypassed locally. Supply this pin with a power source greater than 2.7V during VIN start-up to provide enough voltage to VDD.

ABSOLUTE MAXIMUM RATINGS (1)

SW……..
-0.3V (-5V for <10ns) to +18V (22V for <10ns)
VIN, EN, MODE, VOUT..... -0.3V to +18V
BST……. -0.3V to V_{SW} + 4.5V
All other pins……..…… -0.3V to + 4.5V
HS-FET body diode inrush current…..... 15A (2)
Continuous power dissipation (T_A = 25°C) (3)
QFN-10 (2mmx2.5mm)…….. 2.8W (4)
TSOT23-8…… 2.4W (5)
Junction temperature…….. 150°C
Lead temperature…….... 260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM)……..... 2000V
Charged device model (CDM)..... 750V

Recommended Operating Conditions (6)

Start-up input voltage (V_{ST})……..... 2.7V to 16V (2)
Operation input voltage (V_{IN})……..... 0.8V to 16V
Startup input voltage with VDD bias (V_{ST2})……0.95V to 16V
Maximum external VDD bias voltage….. 3.6V (7)
Boost output voltage (V_{OUT})…… V_{IN} to 16V
Operating junction temp (T_J)… -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-10 (2mmx2.5mm)		
EV3437-RP-00A (4)	44	11 °C/W
JESD51-7 (8)	70	15 °C/W
TSOT23-8		
EVL3437-J-00A (5)	52	12 °C/W
JESD51-7 (8)	100	55 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) During input start-up, the inrush current through the high-side MOSFET (HS-FET) body diode should be below 15A. Avoid continuous current through the HS-FET body diode. See the Input Start-Up Inrush Current Control section on page 20 for further details.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on the EV3437-RP-00A, a 2-layer, 63mmx63mm, 2oz PCB.
5) Measured on the EVL3437-J-00A, a 2-layer, 63mmx63mm, 2oz PCB.
6) The device is not guaranteed to function outside of its operating conditions.
7) When the external VDD bias voltage is below its normal regulated voltage, the external power should prevent current from flowing out of the VDD pin.
8) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [9], typical values are tested at T_J = 25° C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage [10]	V_{ST}	No VDD bias	2.7		16	V
		VDD = 3V	0.95		16	V
Operating input voltage	V_{IN}		0.8		16	V
Operating VDD Voltage [11]	V_{DD}	V_{IN} = 2.7V, 0mA	2.3	2.6		V
		V_{IN} = 12V, 0mA - 10mA		3.4		V
VDD under-voltage lockout (UVLO) rising threshold [11]	VDD_{UVLO_R}	V_{DD} rising	2.2	2.4	2.6	V
VDD UVLO falling threshold	VDD_{UVLO_F}	V_{DD} falling	2	2.2	2.4	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	µA
Quiescent current	I_Q	V_{FB} = 1.05V, V_{IN} = 3V, V_{OUT} = 8V, no switching, measured on VIN		3	6	µA
		V_{FB} = 1.05V, V_{IN} = 3V, V_{OUT} = 8V, no switching, measured on VOUT		380	500	µA
		V_{FB} = 1.05V, V_{IN} = 9V, V_{OUT} floating, PSM, pass-through mode, measured on VIN		430	550	µA
Enable (EN) Control						
EN turn-on voltage threshold	V_{EN_ON}	V_{EN} rising (switching)	1.15	1.23	1.31	V
EN high voltage threshold	V_{EN_H}	V_{EN} rising (micro-power)			1.0	V
EN low voltage threshold	V_{EN_L}	V_{EN} falling (micro-power)	0.4			V
EN turn-on hysteresis	I_{EN_HYS}	1.0V < EN < V_{EN_ON}	3.5	5	6.5	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN is on, IC starts switching		220		µs
Frequency						
Switching frequency	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 8V	500	600	700	kHz
Low-side MOSFET (LS-FET) minimum on time [12]	t_{MIN_ON}			130		ns
LS-FET maximum on time	t_{MAX_ON}			7.5		µs
Loop Control						
Feedback (FB) reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.05V			50	nA
Soft-start (SS) time	t_{SS}	V_{FB} from 0V to 1V		4		ms
Mode Selection (QFN Package) [13]						
Ultrasonic mode (USM) MODE tri-state region	V_{MODE_TRI}		0		0.6	V_{DD}
Pulse-skip mode (PSM) MODE tri-state region			0.95		1.2	
Forced continuous conduction mode (FCCM) MODE tri-state region			1.6		VDD	
USM frequency	f_{USM}		23	33		kHz
HS-FET zero-current detection (ZCD)		PSM, V_{FB} = 1V, L = 1.5µH, V_{OUT} = 8V.	-200	0	+300	mA
HS-FET ZCD [12] [14]		V_{FB} = 1.05V, USM and FCCM			-2	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [9], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Switch						
LS-FET switch on resistance	R_{ON_L}			14		mΩ
High-side (HS) synchronous switch on resistance	R_{ON_H}			21		mΩ
LS-FET leakage current		V_{SW} = 16V, T_J = 25°C			0.1	μA
HS-FET leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.1	μA
Current Limit						
Switching current limit	I_{PK_LIMT}		8.5	9.5	11	A
Protection						
Output over-voltage protection (OVP) threshold			16	16.5		V
Output OVP hysteresis				0.5		V
FB OVP threshold [15]				110%		V_{REF}
FB OVP hysteresis [15]				3%		V_{REF}
Thermal Protection						
Thermal shutdown [12]	T_{SD}			150		°C
Thermal shutdown hysteresis [12]	T_{SD_HYS}			25		°C

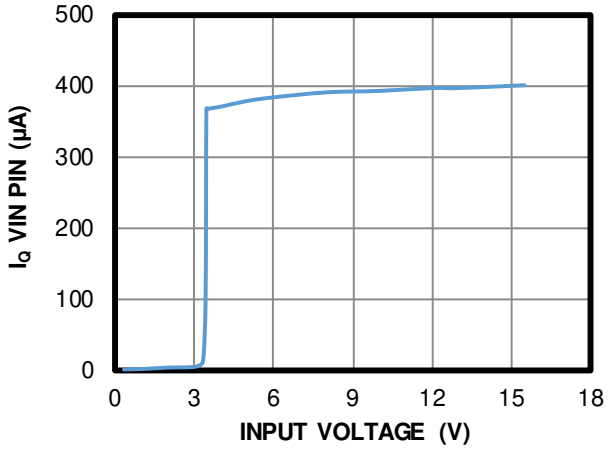
Notes:

9) Guaranteed by over-temperature (OT) correlation. Not tested in production.
10) During input start-up, the HS-FET body diode's inrush current should be below 15A. See the Input Start-Up Inrush Current Control section on page 20 for further details.
11) The VDD pin's regulation voltage from 2.7V_{IN} is greater than VDD_{UVLO_R} in each unit. This guarantees that the IC will start up at 2.7V_{IN}.
12) Guaranteed by sample characterization. Not tested in production.
13) The TSOT23-8 package does not have a MODE pin; the IC works in PSM mode.
14) HS-FET ZCD is below -2A in USM and FCCM.
15) FB OVP only works in PSM.

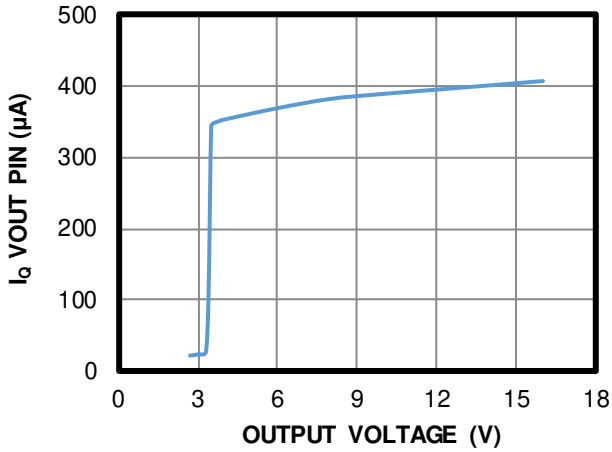
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

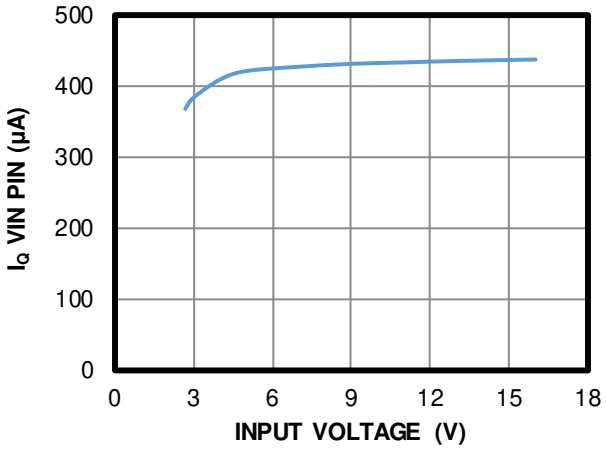
I_Q (VIN Pin) vs. V_{IN}
Boost mode, V_{OUT} = 16V



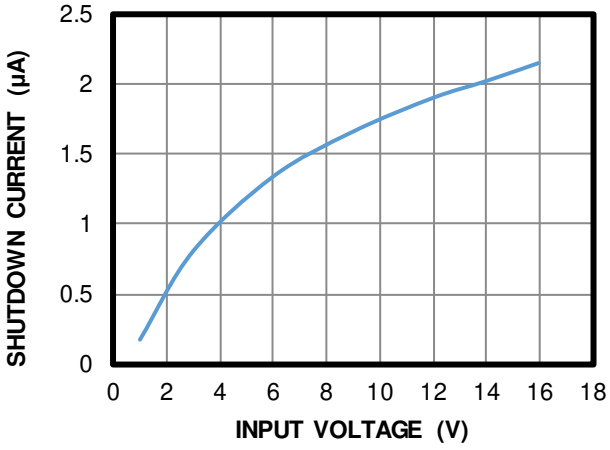
I_Q (VOUT Pin) vs. V_{OUT}
Boost mode



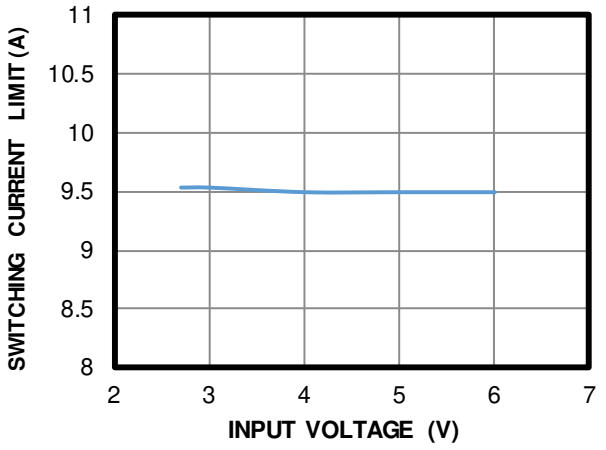
I_Q (VIN Pin) vs. V_{IN}
Pass-through mode



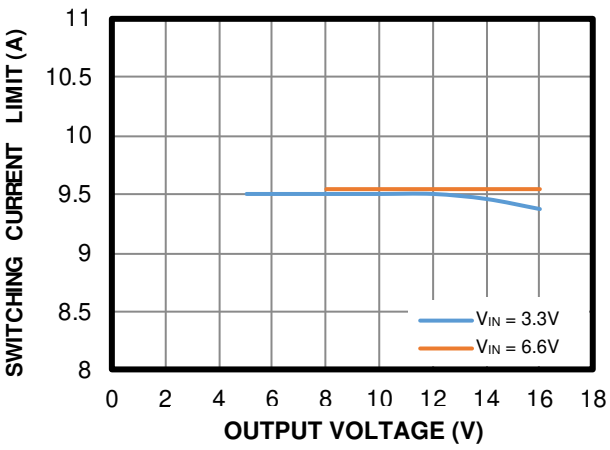
Shutdown Current vs. V_{IN}



Switching Current Limit vs. V_{IN}



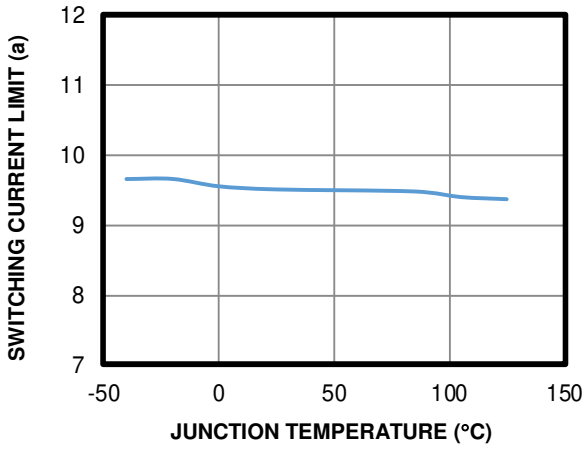
Switching Current Limit vs. V_{OUT}



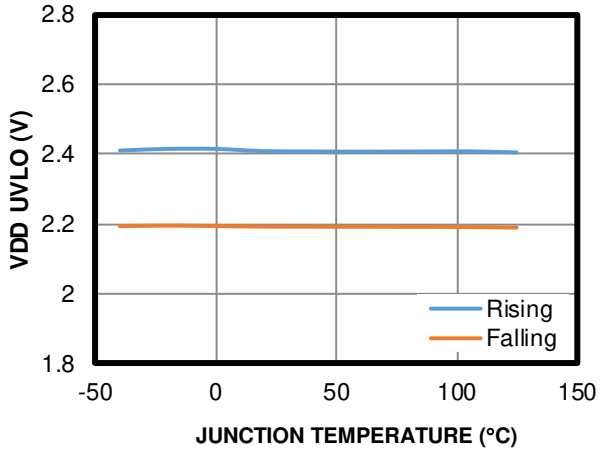
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Switching Current Limit vs. T_J

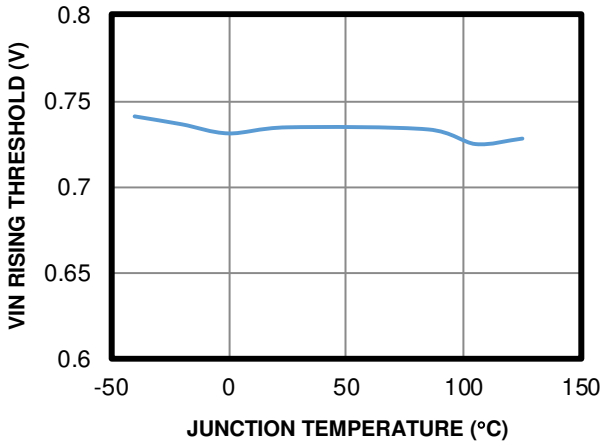


VDD UVLO vs. T_J



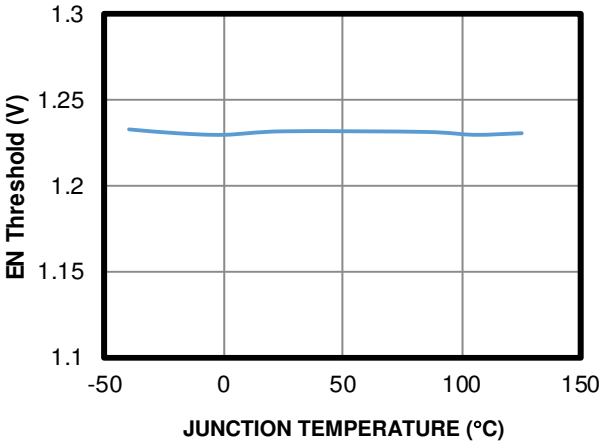
V_{IN} Rising Threshold vs. T_J

V_{DD} bias = 3V

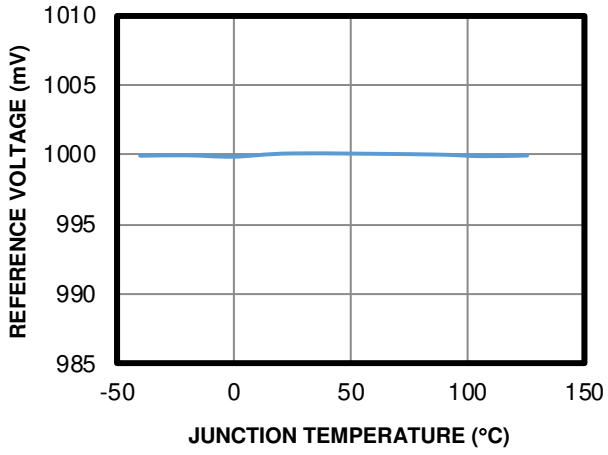


EN Threshold vs. T_J

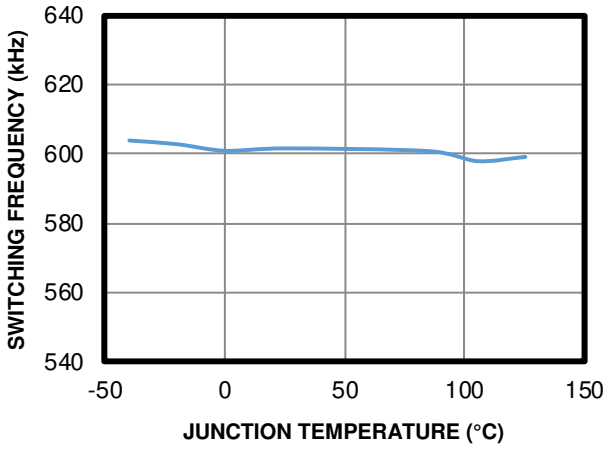
IC starts switching



Reference Voltage vs. T_J



Switching Frequency vs. T_J

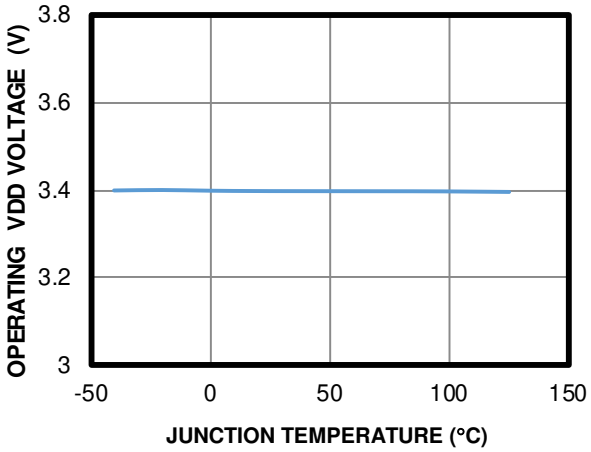


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Operating VDD Voltage vs. T_J

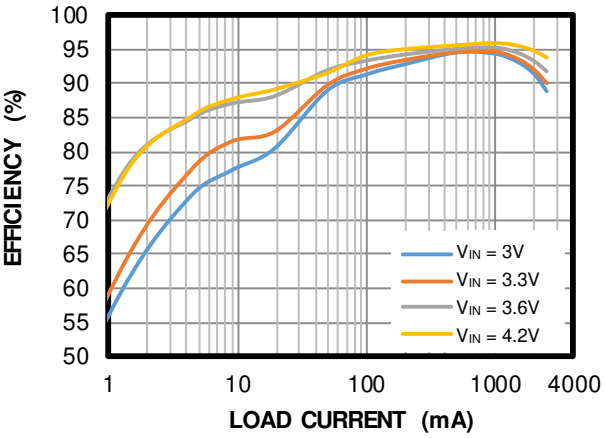
V_{IN} = 12V, 0mA



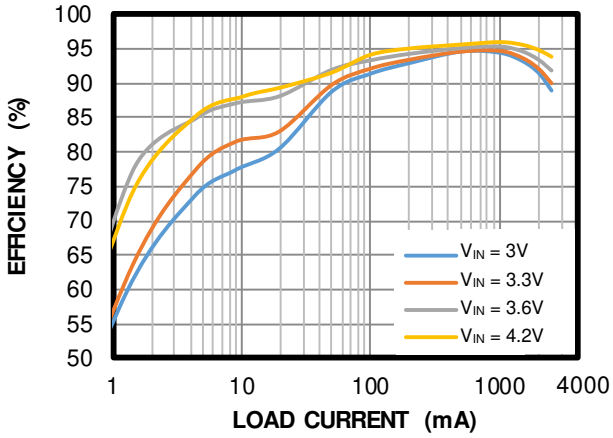
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 2.5A, PSM, T_A = 25°C, unless otherwise noted.

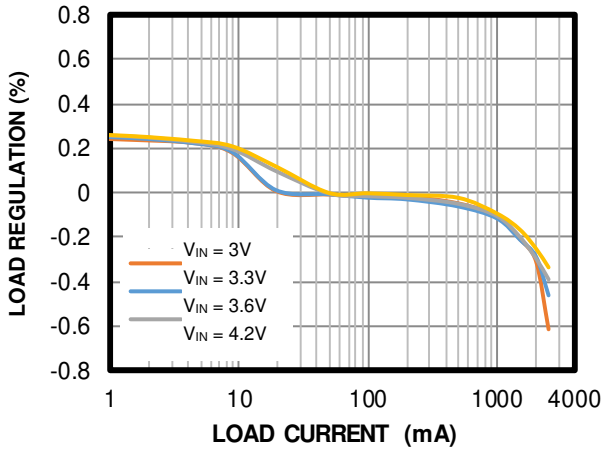
Efficiency vs. Load Current (16)
PSM



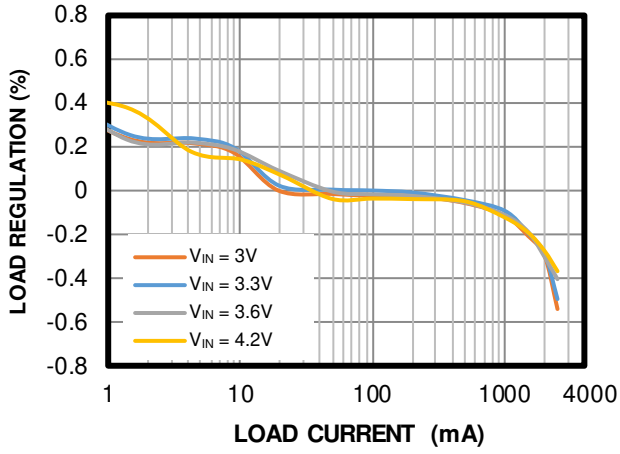
Efficiency vs. Load Current (16)
USM



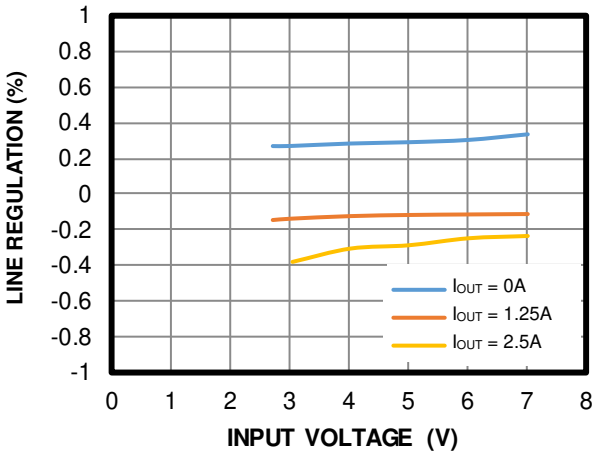
Load Regulation
PSM



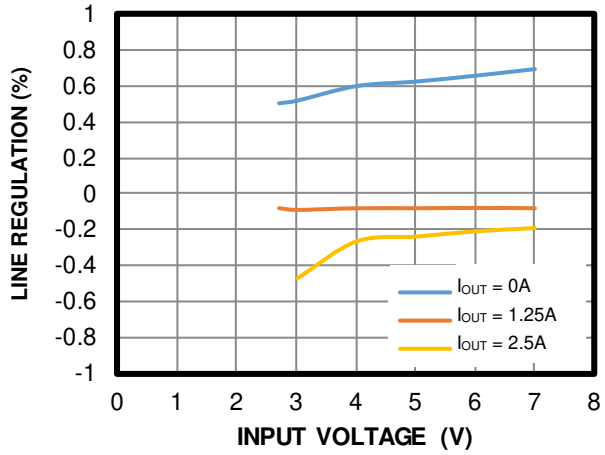
Load Regulation
USM



Line Regulation
PSM



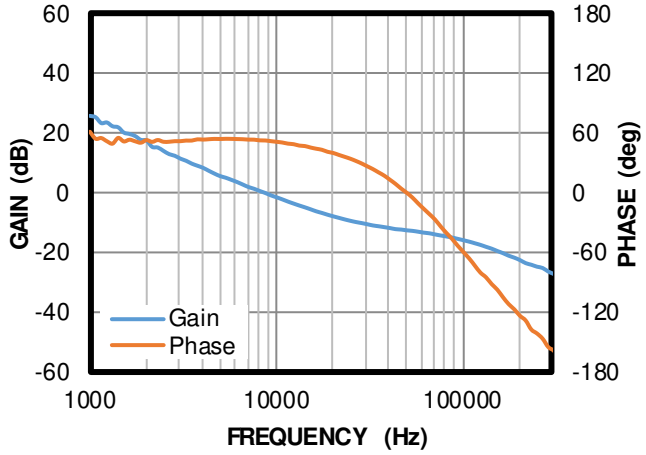
Line Regulation
USM



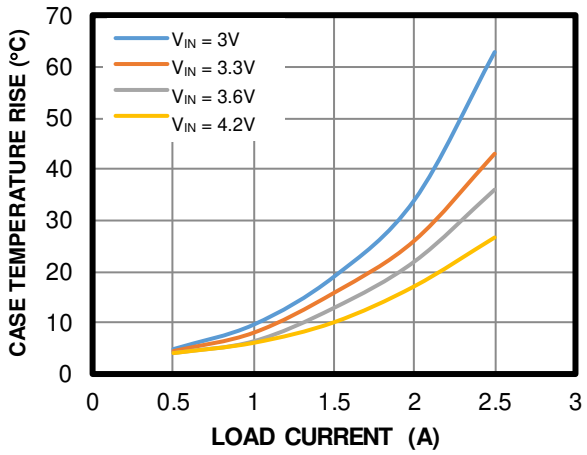
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 2.5A, PSM, T_A = 25°C, unless otherwise noted.

Bode Plot



Case Temperature Rise (16)



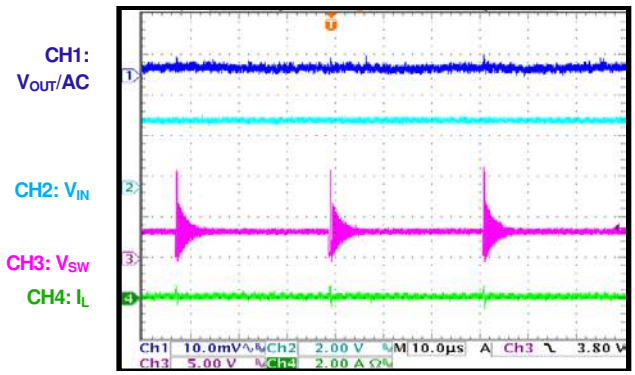
Note:

16) Tests performed with QFN package.

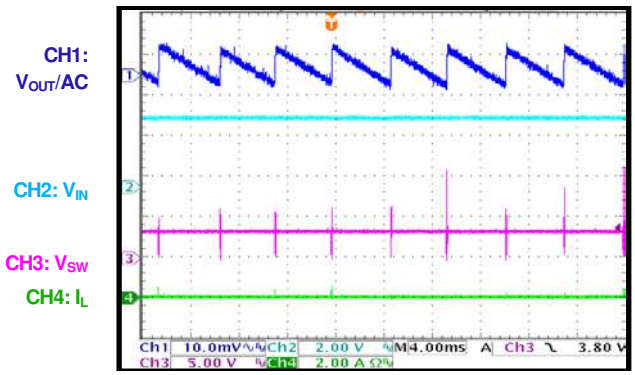
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 2.5A, PSM, T_A = 25°C, unless otherwise noted.

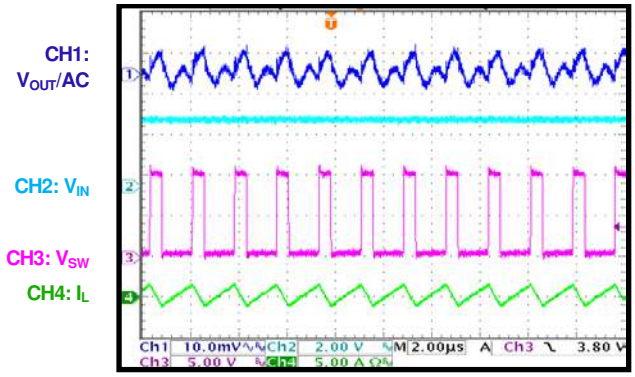
Steady State
I_{OUT} = 0A, USM



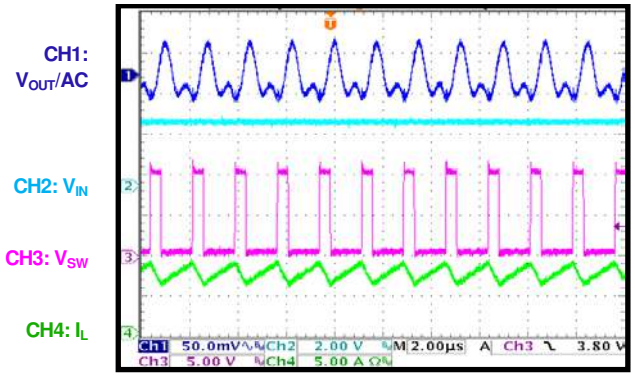
Steady State
I_{OUT} = 0A, PSM



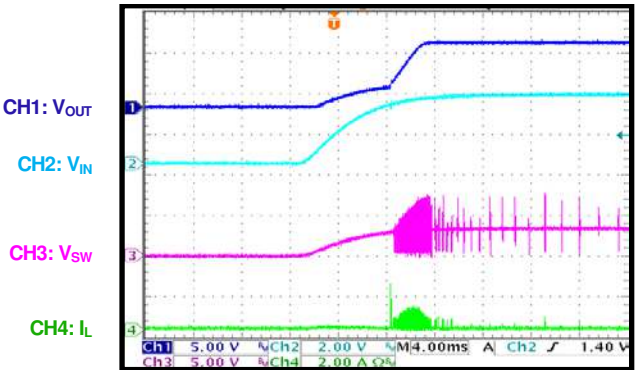
Steady State
I_{OUT} = 0A, FCCM



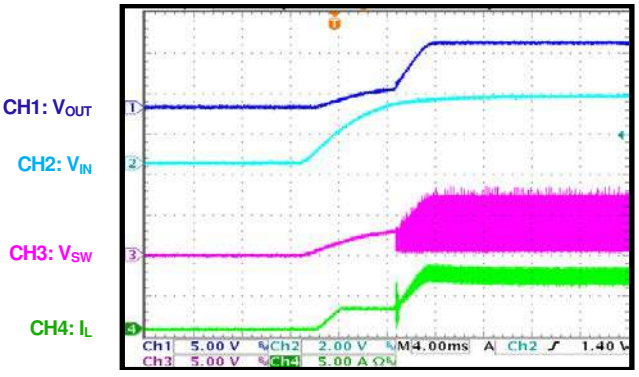
Steady State
I_{OUT} = 2.5A



Start-Up through VIN
I_{OUT} = 0A



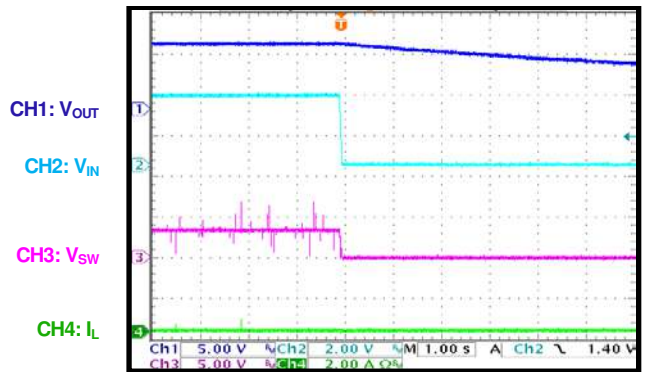
Start-Up through VIN
I_{OUT} = 2.5A



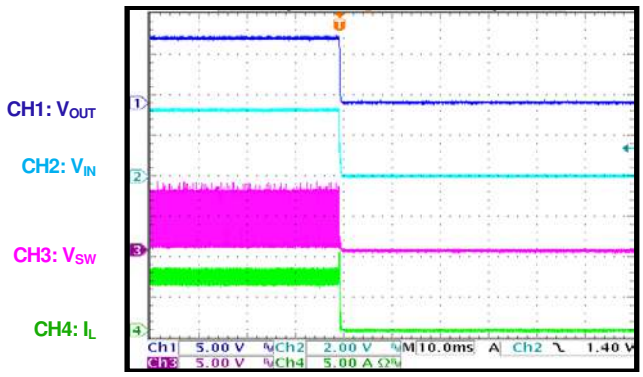
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 2.5A, PSM, T_A = 25°C, unless otherwise noted.

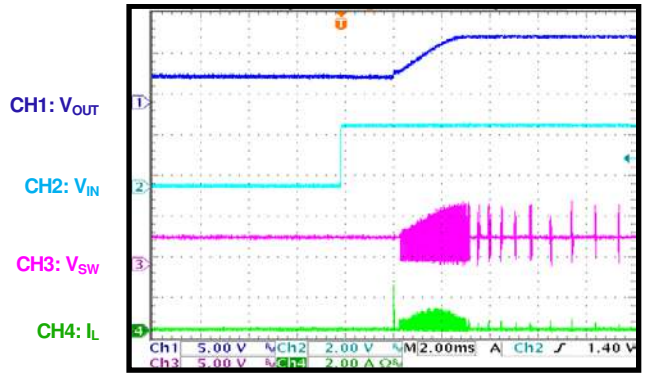
Shutdown through VIN
I_{OUT} = 0A



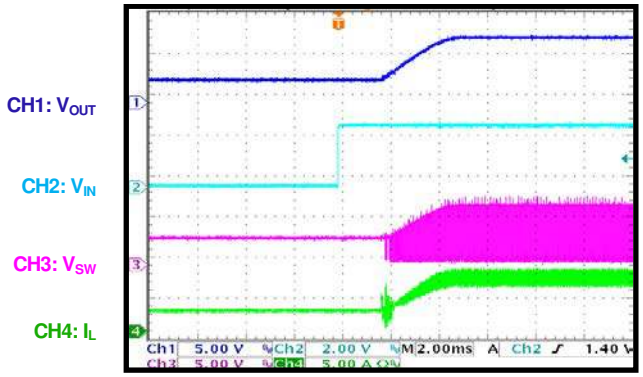
Shutdown through VIN
I_{OUT} = 2.5A



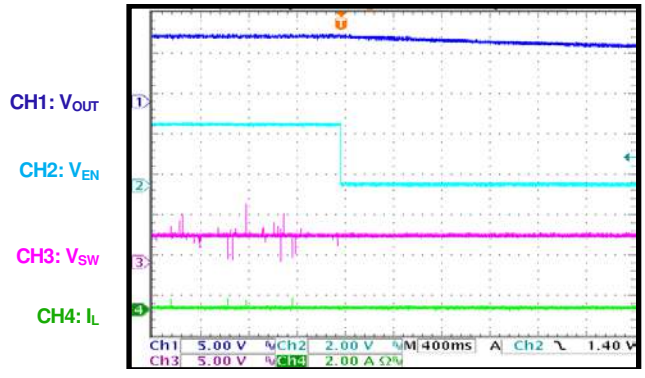
Start-Up through EN
I_{OUT} = 0A



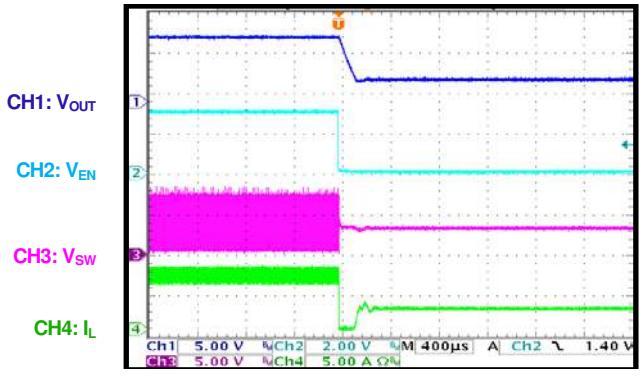
Start-Up through EN
I_{OUT} = 2.5A



Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 2.5A

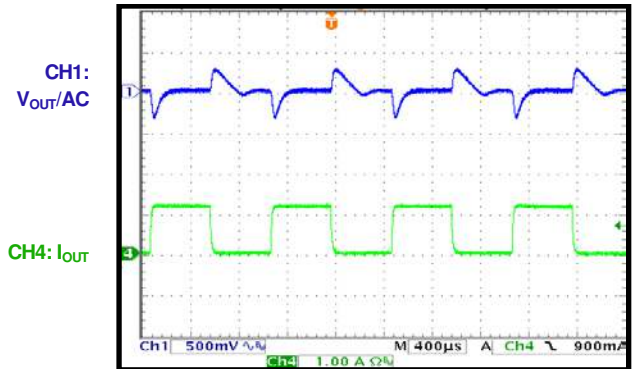


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 8V, L = 1.5µH, I_{OUT} = 2.5A, PSM, T_A = 25°C, unless otherwise noted.

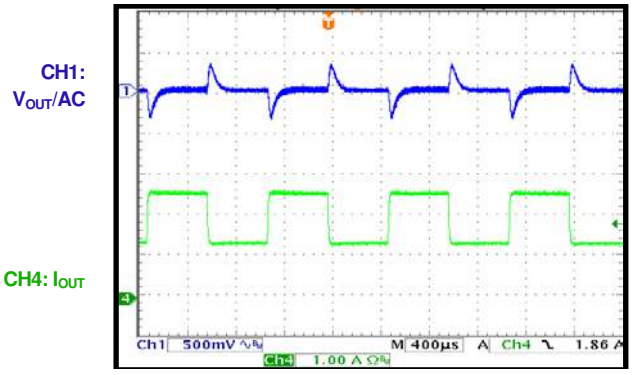
Load Transient

I_{OUT} = 0A to 1.25A, USM



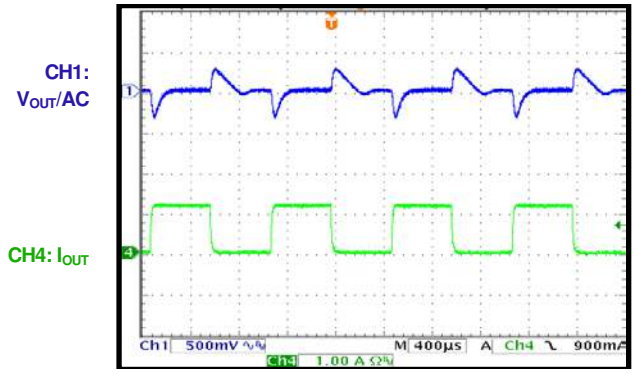
Load Transient

I_{OUT} = 1.25A to 2.5A



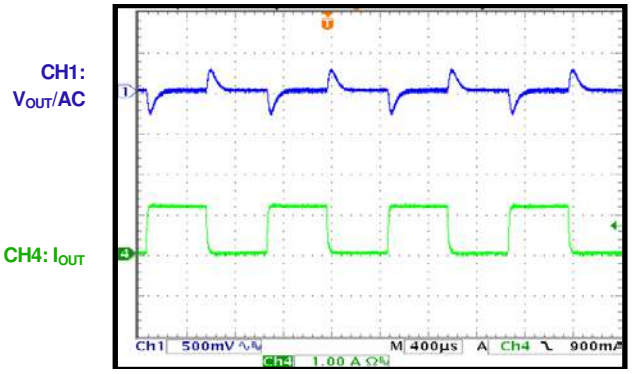
Load Transient

I_{OUT} = 0A to 1.25A, PSM



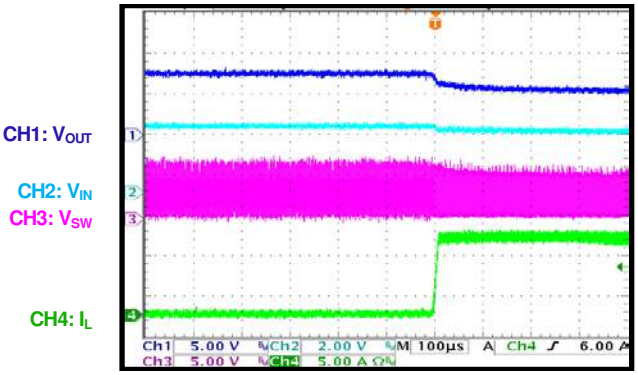
Load Transient

I_{OUT} = 0A to 1.25A, FCCM



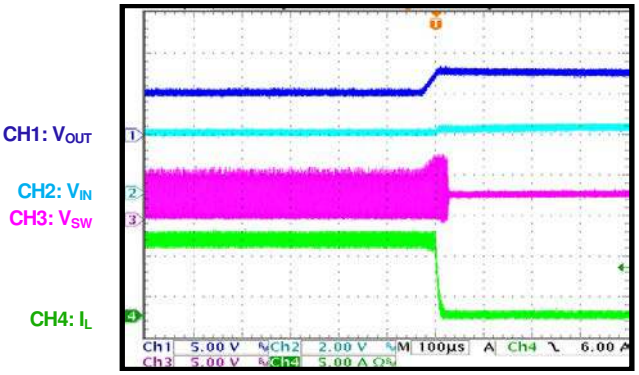
Over-Current Entry

Increased output current, 0A to 4.5A



Over-Current Recovery

Decreased output current, 4.5A to 0A



FUNCTIONAL BLOCK DIAGRAM

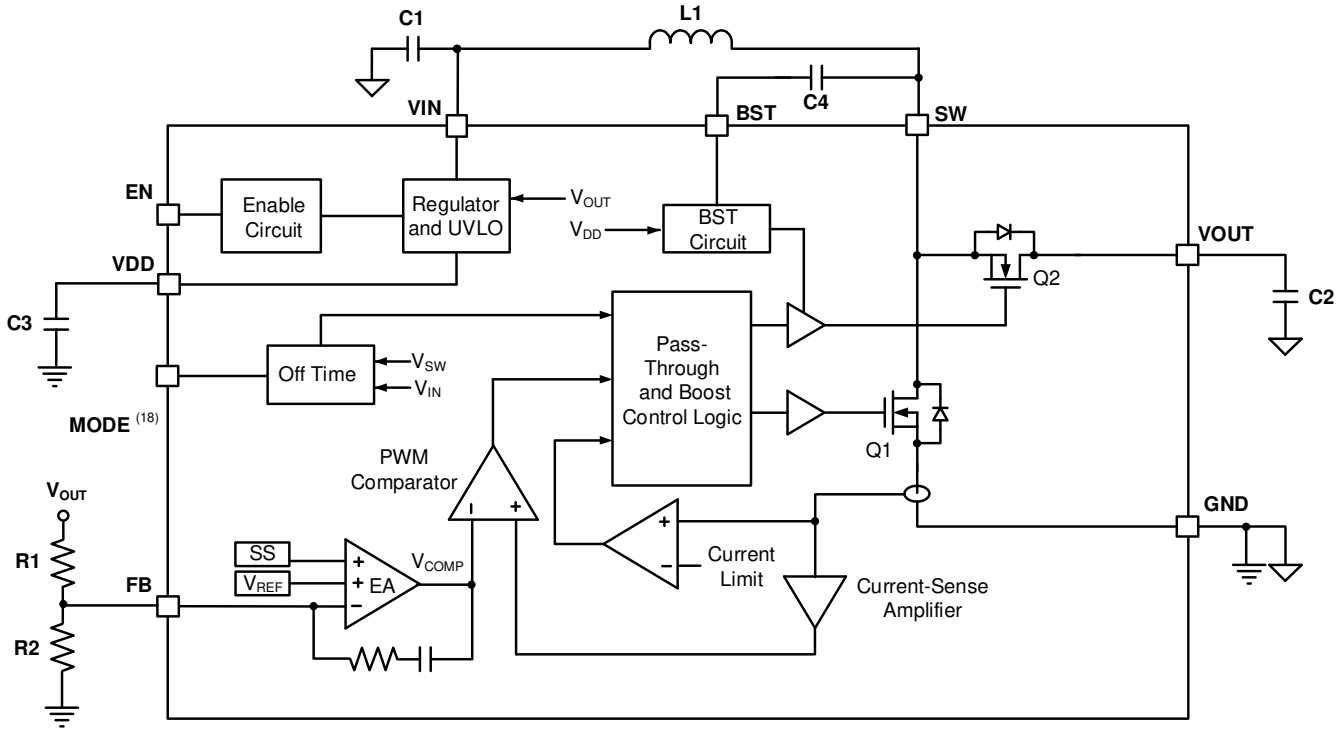


Figure 1: Functional Block Diagram

Note:

17) Only the MP3437GRP has a MODE pin.

OPERATION

The MP3437 is a 600kHz, fixed-frequency, high-efficiency boost converter with a wide input voltage range. Its fully integrated low $R_{DS(ON)}$ MOSFETs allow the IC to provide small size and high efficiency for high-power step-up applications. Constant-off-time (COT) control provides fast transient response, while MODE selection provides flexible light-load performance design.

Boost Operation

The MP3437 uses COT control to regulate the output voltage. At the beginning of each cycle, the N-channel low-side MOSFET (LS-FET) Q1 is turned on, forcing the inductor current to rise. The inductor current can be sensed through the LS-FET. If the current signal exceeds the comparator voltage (V_{COMP}), which is an amplifier output comparing the feedback voltage (V_{FB}) to the internal reference voltage, the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. Then the inductor current flows to the output capacitor through the high-side MOSFET (HS-FET), causing the inductor current to decrease. After a fixed off time, the LS-FET turns on again and the cycle repeats. In each cycle, the V_{IN} or V_{OUT} rate determines the LS-FET off time, and the V_{COMP} controls the on time. The inductor peak current is controlled by V_{COMP}, which is controlled by V_{OUT}. Therefore, the inductor current regulates V_{OUT}.

Operation Mode

The MP3437 works with a 600kHz frequency and PWM control under heavy-load conditions. In the QFN package, the MODE pin can set the part to work in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) under light-load conditions. In the TSOT package, the MP3437 works in PSM under light-load conditions.

Forced Continuous Conduction Mode (FCCM)

The MP3437 works in fixed-frequency PWM for any load condition if the MODE pin is high (>1.6V). In this circumstance, the off time is determined by the internal circuit to achieve the 600kHz frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current from V_{OUT} to V_{IN} may become negative during the off time (when the LS-FET is off and the HS-FET is on). This forces the inductor current to work in FCCM with a fixed frequency, producing a lower V_{OUT} ripple than in PSM.

Pulse-Skip Mode (PSM)

The MP3437 works in PSM mode under light-load conditions by floating the MODE pin or setting the voltage within the PSM range (0.95V < V_{MODE} < 1.2V). Once the inductor current drops to 0A, the HS-FET turns off to prevent current flow from V_{OUT} to V_{IN}, forcing the inductor current to work in discontinuous conduction mode (DCM). The internal off time becomes longer once the MP3437 enters DCM. The off time is inversely proportional to the HS-FET on period in each cycle. In deep DCM conditions, the MP3437 slows down the switching frequency and reduces power loss.

If V_{COMP} drops below the PSM threshold, the MP3437 stops switching to avoid further switching power loss. Switching resumes once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} under extreme light-load conditions. PSM is more efficient than FCCM during light-load conditions, but the V_{OUT} ripple may be higher, and the frequency may decrease and produce audible noise.

In DCM, the frequency is low, and the LS-FET does not turn on during the prolonged off time. If the load and V_{COMP} increase, the off time shortens and the MP3437 returns to its regular 600kHz fixed frequency so the loop can respond to the high load current.

Ultrasonic Mode (USM)

To prevent audible noise with a switching frequency below 20kHz in PSM, the MP3437 implements ultrasonic mode (USM) by setting V_{MODE} in the USM range (0V < V_{MODE} < 0.6V).

In USM, the inductor current works in DCM, and the frequency stretches as if in PSM when the load decreases to a moderate level. However, switching does not stop when V_{COMP} drops to the PSM threshold. V_{COMP} controls the LS-FET on time, even if V_{COMP} is below the PSM threshold, unless the LS-FET triggers the minimum on time.

The MP3437 continues to decrease the switching frequency as the load decreases.

Once the MP3437 detects that the LS-FET has been off for 30µs, it forces the LS-FET on. This limits the frequency to avoid audible noise under light-load or no-load conditions.

USM may convert more energy to the output than the required load because of the minimum 23kHz frequency that causes V_{OUT} to rise above the normal voltage setting. When V_{OUT} rises and V_{COMP} drops, the inductor peak current may drop. If V_{COMP} drops below one internal clamped level, the HS-FET ZCD threshold is gradually regulated to a negative level so the energy in the inductor can flow back to V_{IN} during each cycle. This keeps the set output voltage (V_{OUT_SET}) above 23kHz. The MP3437 also works with a 600kHz frequency if V_{COMP} rises again.

USM has the same efficiency as PSM if the frequency is greater than the typical 33kHz. USM has worse power loss than PSM if the frequency is clamped at the typical 33kHz. However, USM does not introduce audible noise, caused by the group pulse, as PSM does.

Automatic Pass-Through in PSM

If V_{IN} is above V_{OUT_SET} during PSM mode, the LS-FET remains off and the HS-FET remains on. The current goes through the inductor and the HS-FET to the output terminal; this operation is called automatic pass-through mode. The HS-FET turns on slowly to avoid inrush current between V_{IN} and V_{OUT}. The MP3437 returns to boost switching mode once V_{OUT} drops below 95% of V_{REF}, and V_{COMP} exceeds the PSM threshold.

When the HS-FET is on, the internal charge pump is enabled to drive the HS-FET gate. The charge pump is only enabled after the IC enters pass-through mode.

In USM, if V_{IN} is above the set V_{FB} value and COMP is pulled low, the MP3437 switches with a limited frequency even when V_{OUT} is above regulation. This keeps V_{OUT} slightly above V_{IN}.

In FCCM, the MP3437 switches with a 600kHz fixed frequency, even when V_{OUT} is above regulation (due to V_{IN} rising). Whether V_{OUT} is above or below V_{IN} is determined by the minimum on time of each period.

Table 1 shows the different work modes for when V_{IN} is greater than V_{OUT}.

Table 1: Work Mode when V_{IN} > V_{OUT} Regulation

MODE	V_{IN} > V_{OUT_SET} Work Mode	FB OVP
PSM	HS-FET pass-through	Yes
USM	Keep 33kHz switching	No
FCCM	Keep 600kHz switching	No

Minimum On Time and Minimum Off Time

The MP3437 blanks the LS-FET on state with 130ns during each cycle to enhance noise immunity. This 130ns minimum on time restricts applications with a high V_{IN} / V_{OUT} ratio. The MP3437 also blanks the LS-FET off state with a minimum off time during each cycle. The LS-FET cannot turn on during the minimum off time.

LS-FET Maximum On Time

If the inductor current cannot trigger V_{COMP} with an on time of 7.5µs, the MP3437 shuts down the LS-FET. After the LS-FET shuts down, the inductor current goes through the HS-FET and charges V_{OUT} in the off time period. This helps refresh V_{OUT} with a minimum frequency of about 133kHz under heavy load transient conditions.

VDD Power

The MP3437 internal circuit is powered by the VDD pin. It is recommended to place a minimum 4.7µF ceramic capacitor on VDD. When V_{IN} exceeds 3.4V, VDD is powered by the VIN pin. When V_{IN} is below 3.4V, VDD is powered by either the VIN or VOUT pin. In this case, the pin with the higher voltage powers VDD. This reduces power loss between VOUT and VDD in the event that V_{OUT} exceeds V_{IN}.

If VDD is powered by an external supply and the voltage is above 3.4V, the regulators from V_{IN} and V_{OUT} disable. In this circumstance, the MP3437 starts once the external VDD power supply exceeds VDD_{UVLO}, even if V_{IN} is as low as 0.95V. When VDD is powered by the external power supply, the MP3437 continues working, even if both V_{IN} and V_{OUT} are dropping (so long as they remain above 0.8V). The external VDD power source should be limited to 3.6V.

There is a reverse-blocking circuit to prevent current from flowing between V_{IN} and V_{OUT}. If the external VDD power is above the VDD regulation voltage, the current is supplied from the external power and there is no path for the current to flow from VDD to V_{IN} or V_{OUT}.

VDD is charged when V_{IN} is above about 0.95V and EN is above the micro-power threshold. If EN is low, VDD is disconnected from V_{IN} and

V_{OUT}. Supply V_{IN} with a power source greater than 2.7V during VIN start-up to provide enough VDD voltage.

Start-Up

When the MP3437 turns on, it starts charging the VDD pin from the VIN pin. Once VDD exceeds its under-voltage lockout (UVLO) threshold, the MP3437 starts switching with closed-loop control. If VDD is powered by an additional supply, the MP3437 starts switching once VDD exceeds its UVLO threshold.

After the IC is enabled, the MP3437 starts up with a soft start (SS). The SS signal is controlled by the internal signal rising from 0V, and is compared with the internal reference voltage (V_{REF}). The lower between V_{SS} and V_{REF} is fed to the error amplifier to control the output voltage. After V_{SS} exceeds V_{REF}, SS completes and the internal reference takes control of the feedback loop regulation.

During input start-up, the inrush current through the HS-FET body diode should be below 15A. See the Input Start-Up Inrush Current Control section on page 20 for further details.

If there is bias voltage on V_{OUT} during PSM, the MP3437 stops switching until V_{SS} exceeds V_{FB}, which is proportional to the V_{OUT} bias voltage. If the IC is in USM or FCCM, the MP3437 works with a frequency of about 33kHz or 600kHz respectively. Both USM and FCCM have a negative inductor current, so the energy may transfer from V_{OUT} to V_{IN} if the V_{OUT} bias is high.

Synchronous Rectifier and BST Function

The MP3437 integrates both an LS-FET Q1 and HS-FET Q2 to reduce external components. During switching, the rectifier switch Q2 is powered by the BST pin (typically 3.4V above V_{SW}). This 3.4V BST voltage is charged from VDD when the LS-FET turns on.

During pass-through mode, BST is regulated by the internal charge pump.

Switching Peak Current Limit

The MP3437 provides a fixed, cycle-by-cycle switching peak current limit function. During each cycle, the internal current-sense circuit monitors the LS-FET current signal. Once the sensed current reaches the set current limit (typically 9.5A), the LS-FET Q1 turns off. The LS-FET current signal is internally blanked for about 130ns to enhance noise immunity.

Enable (EN) and Programmable UVLO

The EN pin enables and disables the MP3437. When applying a voltage greater than EN's maximum threshold (1V), the MP3437 starts up some of the internal circuits (micro-power mode). If V_{EN} exceeds the turn-on threshold (1.23V), the MP3437 enables all functions and begins boost operation. Boost switching is disabled when V_{EN} falls below its turn-on threshold (1.23V). To completely shut down the MP3437, EN must have a low-level voltage of 0.4V or less. After shutdown, the MP3437 sinks the current from the input power (typically less than 2µA). EN is compatible with voltages up to 16V. For automatic start-up, connect EN directly to VIN.

The MP3437 features a programmable UVLO hysteresis. When powering up in micro-power mode, EN sinks a 5µA current from the R_{TOP} upper resistor (see Figure 2).

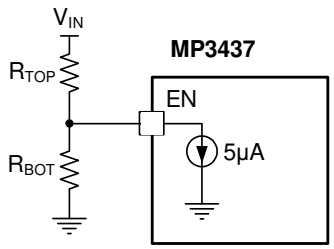


Figure 2: V_{IN} UVLO Program

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold can be calculated with Equation (1):

$$V_{IN\_ON} = V_{EN\_ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (1)$$

Where V_{EN_ON} is the EN voltage turn-on threshold (typically 1.23V).

Once V_{EN} reaches V_{EN_ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN}

falling threshold, which can be calculated with Equation (2):

$$V_{IN\_UVLO\_HYS} = 5\mu A \times R_{TOP} \quad (2)$$

Over-Voltage Protection (OVP)

If an over-voltage condition is detected on V_{OUT} (typically with a 16.5V threshold), the MP3437 stops switching immediately until the voltage drops to 16V. This prevents over-voltage on the output and internal power MOSFETs.

The MP3437 also supports OVP for the FB pin during PSM. Once V_{FB} exceeds 110% of V_{REF}, the MP3437 turns off, until V_{FB} drops below 107% of V_{REF}. In USM and FCCM, FB's OVP function is disabled.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. When the die temperature exceeds 150°C, the IC shuts down. Once the die temperature drops to about 125°C, normal operation resumes.

APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider is used to set the output voltage. The feedback resistor (R1) must count for both stability and dynamic response. It is recommended to choose an R1 value between 100kΩ and 800kΩ. R2 can be calculated with Equation (3):

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (3)$$

Where V_{REF} = 1V.

Input Start-Up Inrush Current Control

During input start-up, the inrush current through the HS-FET body diode should be below 15A. If the start-up inrush current is above 15A on the evaluation board, the system can be optimized by following the steps below:

1. Reduce the start-up V_{IN} voltage or slew rate.
2. Reduce the large output capacitor volume or add a MOSFET between the MP3437's output and the bulk capacitor to smoothly charge the bulk capacitor.

Under steady-state conditions, avoid having continuous current flow through the HS-FET body diode.

Selecting the Input Capacitor

The input capacitor (C1) is used to maintain the DC input voltage. Low-ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C1} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (4)$$

Where f_{SW} is the switching frequency, and L is the inductor value.

Selecting the Output Capacitor

The boost converter has a discontinuous output current, and therefore requires an output capacitor (C2) to supply AC current to the load. For the best performance, it is recommended to use low-ESR ceramic capacitors. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times R_L \times C2} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (5)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL6050 Series**

An inductor is required to transfer the energy between the input source and the output capacitors. An inductor with a larger value results in less ripple current and a lower peak inductor current, which reduces stress on the power MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance value can be calculated with Equation (6):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta I_L} \quad (6)$$

Where ΔI_L is the inductor ripple current.

The inductor ripple current should be approximately 20% to 50% of the maximum average current. Typically, a 1.5µH inductor is recommended. Ensure that the inductor does not saturate under worst-case conditions. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL6050-1R2	1.2µH	MPS
MPL-AL6050-1R5	1.5µH	MPS
MPL-AL6050-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

VDD Capacitor Selection

The MP3437 integrates the VDD power at about 3.4V, which typically powers the internal MOSFET gate driver and internal control circuit. A ceramic bypass capacitor (4.7µF or greater) is necessary for the internal regulator. Do not connect the external load to the VDD power.

Bootstrap (BST) Capacitor

The MP3437 uses one bootstrap (BST) circuit to power the output N-channel MOSFET. One external BST capacitor is necessary for the charge pump power. A 0.1µF ceramic capacitor placed between BST and SW is recommended.

Programmable UVLO

The MP3437 features a programmable under-voltage lockout (UVLO) hysteresis. When powering up, EN sinks a 5µA current from the R_{TOP} upper resistor (see Figure 2). V_{IN} must increase to overcome the current sink.

The V_{IN} start-up threshold can be calculated with Equation (7):

$$V_{IN\_ON} = V_{EN\_ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (7)$$

Where V_{EN_ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN_ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (8):

$$V_{IN\_UVLO\_HYS} = 5\mu A \times R_{TOP} \quad (8)$$

For automatic start-up, connect EN with a 30kΩ R_{TOP} resistor to operate with a 150mV hysteresis.

MODE Selection (QFN Package)

The MP3437 works in FCCM, PSM, or USM based on the MODE setting. Pull the MODE pin to the VDD pin for FCCM, float MODE for PSM, or pull V_{MODE} below 0.6V for USM.

Design Example

Table 3 shows a design example following the application guidelines for the provided specifications.

Table 3: Design Example

V_{IN}	3V to 4.2V
V_{OUT}	8V
I_{OUT}	2.5A

Figure 5 and Figure 6 show the detailed application schematics. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 10. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines [18]

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive electromagnetic interference (EMI), resistive loss, and system instability. For the best results, refer to Figure 3 and Figure 4 and follow the guidelines below, unless otherwise noted:

1. Place the output capacitor (C2A, C2B, and C2C) as close to V_{OUT} and GND as possible. Place a 0.1µF capacitor close to the IC (C2D) to reduce parasitic inductance (shown with the yellow components in Figure 3 and Figure 4).
2. For the QFN package, connect the SW pin underneath the IC using vias (shown with the red components in Figure 3). For the TSOT package, connect the SW pin on the top PCB layer using the copper that is under the IC (see Figure 4).
3. If V_{OUT_SET} is above 15V, it is recommended to connect the RC snubber to SW and GND (shown with R6 and C5 in Figure 3 and Figure 4).
4. Place the FB dividers (R1 and R2) as close to the FB pin as possible.
5. Keep the FB trace far away from noise sources, such as the SW node.
6. For the QFN package, connect the R2 GND trace close to GND pin-4.
7. Connect the VDD capacitor to GND with a short loop.
8. Keep the input loop (C1, L1, SW, and GND) as small as possible.
9. Place enough GND vias close to the MP3437 to ensure good thermal dissipation.

Note:

18) The recommended PCB layout is based on the typical application circuits (see Figure 5 and Figure 6 on page 23).

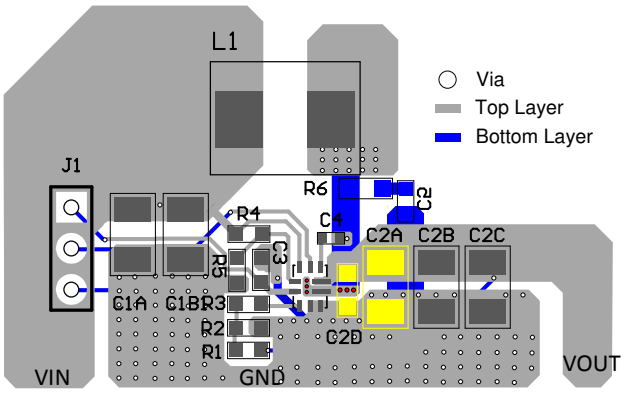


Figure 3: Recommended PCB Layout for QFN-10 Package

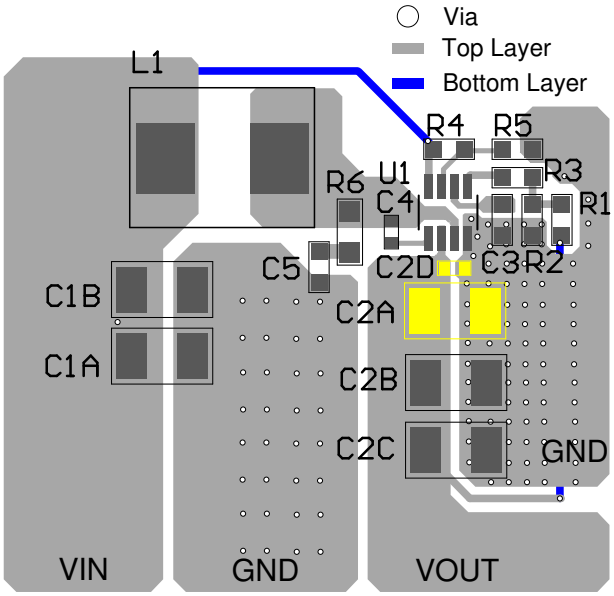


Figure 4: Recommended PCB Layout for TSOT23 Package

TYPICAL APPLICATION CIRCUITS

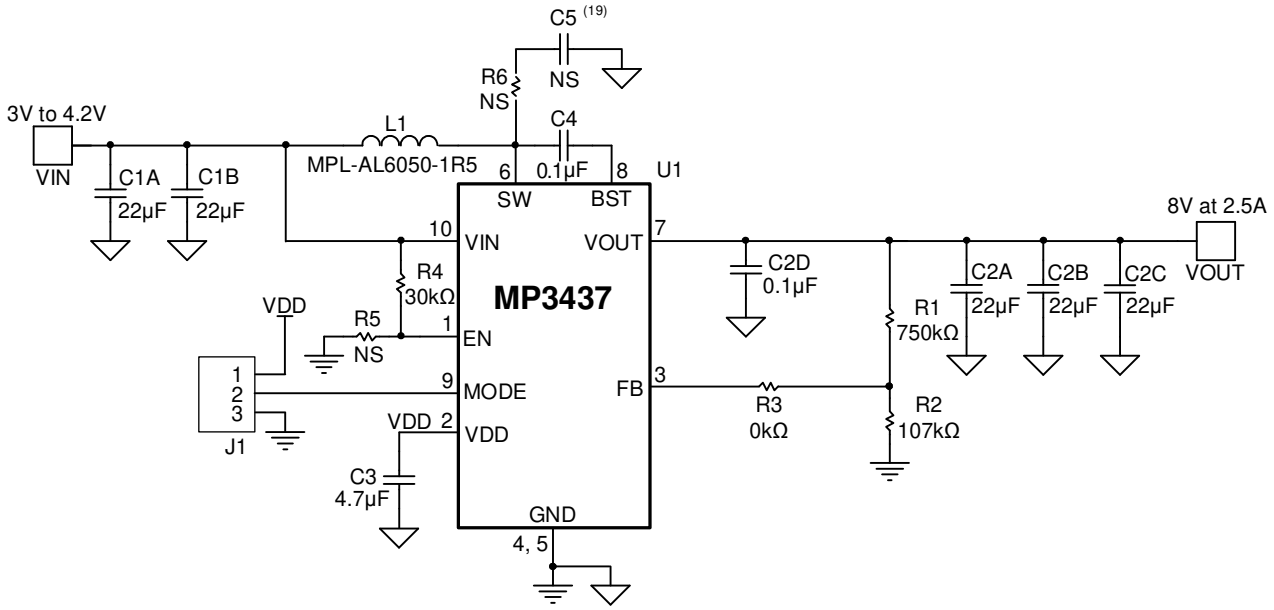


Figure 5: QFN Package Typical Application Circuit

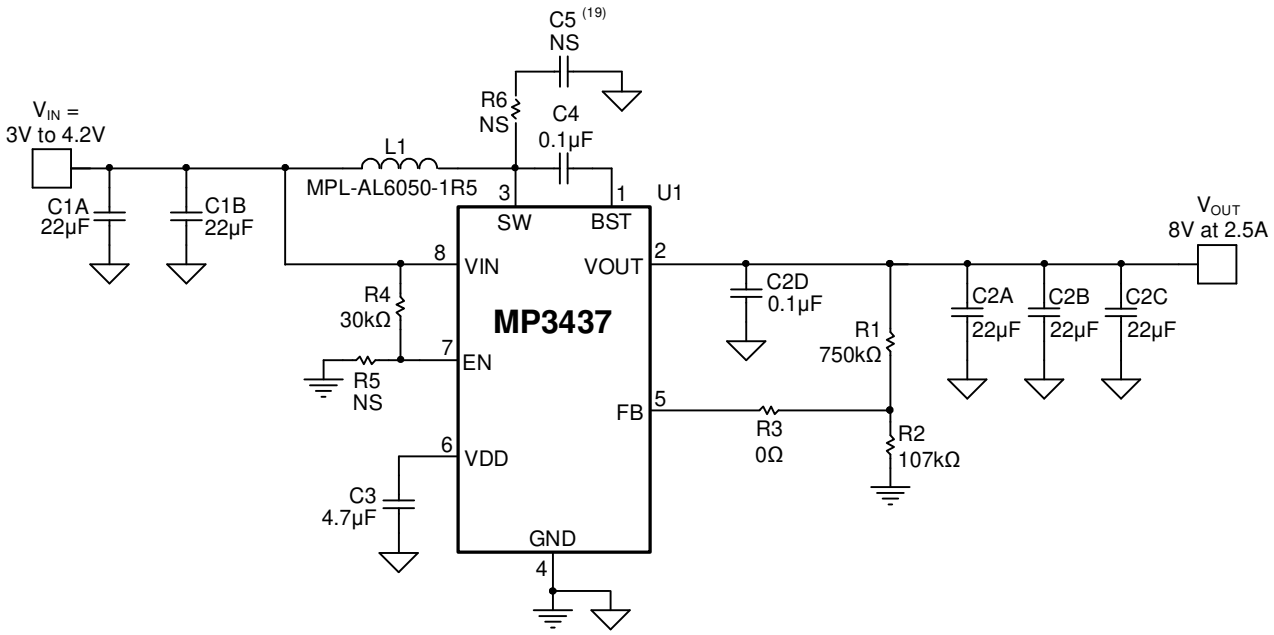


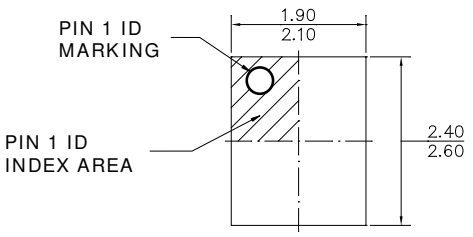
Figure 6: TSOT Package Typical Application Circuit

Note:

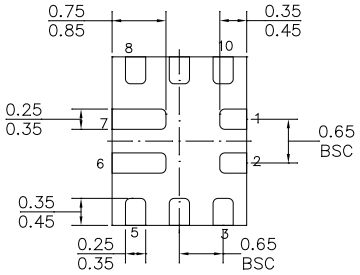
19) If V_{OUT_SET} > 15V, it is recommended to connect the RC snubber to SW and GND (e.g. R6 = 1Ω, C5 = 2.2nF).

PACKAGE INFORMATION

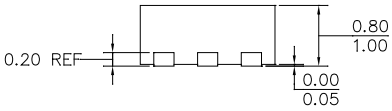
QFN-10 (2.0mmx2.5mm)



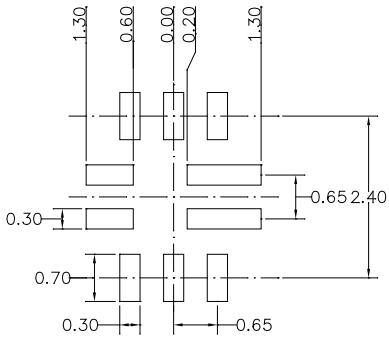
TOP VIEW



BOTTOM VIEW



SIDE VIEW



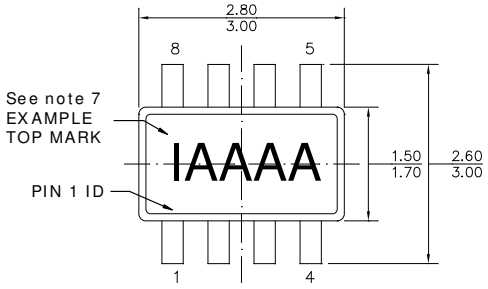
RECOMMENDED LAND PATTERN

NOTE:

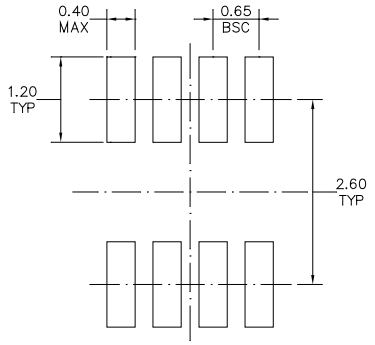
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

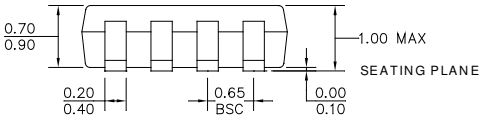
TSOT23-8



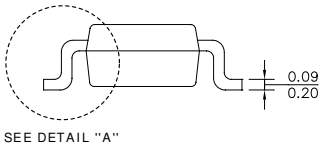
TOP VIEW



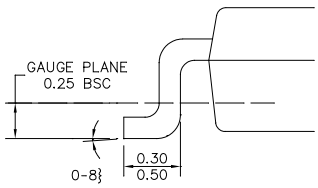
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



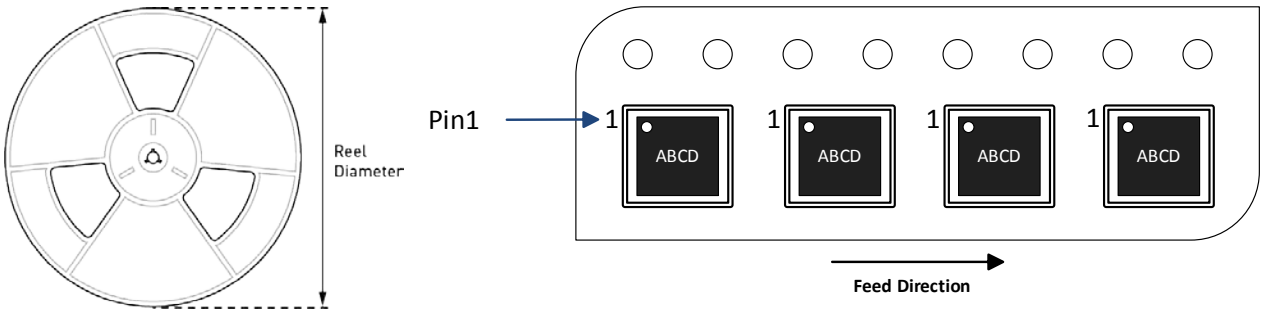
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARKING).

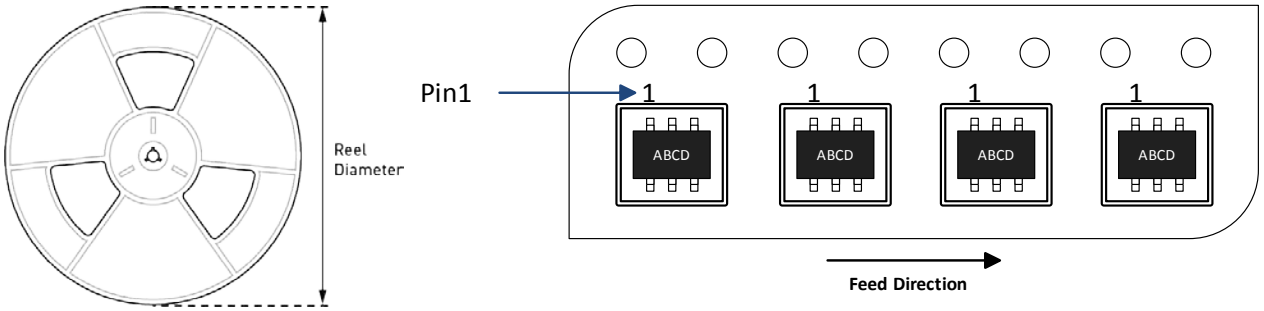
CARRIER INFORMATION

QFN-10 (2.0mmx2.5mm)



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3437GRP–Z	QFN-10 (2mmx2.5mm)	5000	N/A	N/A	13in	12mm	8mm

TSOT23-8



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3437GJ–Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/8/2021	Initial Release	-