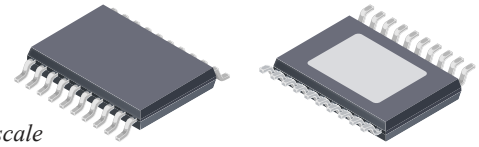
Low Input Voltage, Adjustable Frequency Dual Synchronous 2 A / 2 A Buck Regulator with Synchronization, 2× EN, and 2× NPOR

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Operating voltage range: 2.5 to 5.5 V
- UVLO stop threshold: 2.25 V (max)
- Dual outputs with up to 2 A output current per regulator
- Adjustable output voltage as low as 0.8 V
- Internal 80 mΩ high-side switching MOSFET
- Internal 55 mΩ low-side switching MOSFET
- Adjustable oscillator frequency (f_{OSC}): 0.35 to 2.2 MHz
- Synchronizes to external clock: 1.2× to 1.5× f_{OSC}
- 180° phase shift between switching regulators
- Sleep mode supply current less than 5 µA
- Soft-start time externally set via the SS pin
- Pre-biased startup capable
- Externally adjustable compensation
- Stable with ceramic output capacitors
- Independent enable inputs and NPOR output pins
- NPOR delay of 7.5 ms (A8651) or 120 µs (A8651-1)
- Adjustable current limiting (OCP) for each regulator
- Hiccup mode short-circuit protection (HIC)
- Overvoltage and overtemperature protection
- Open-circuit and adjacent pin short-circuit tolerant
- Short-to-ground tolerant at every pin

PACKAGE: 20-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

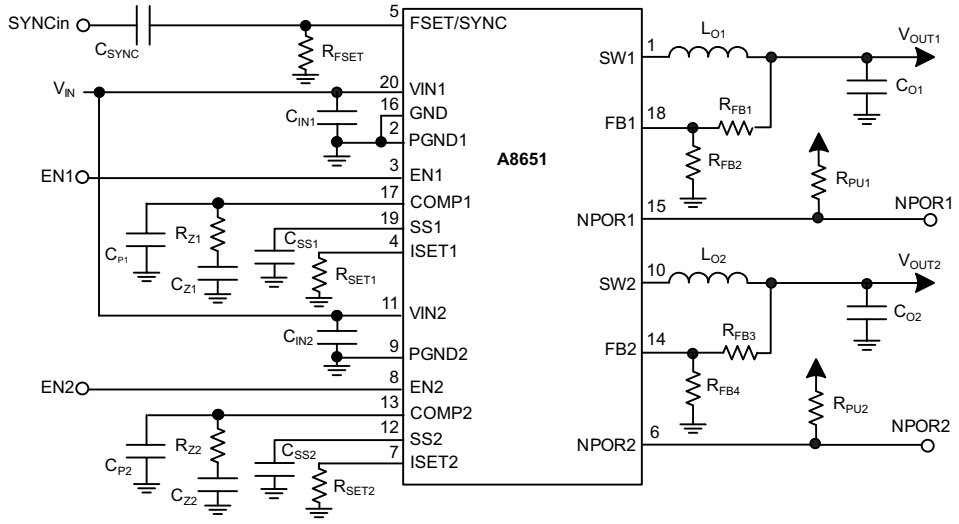
The A8651 is an adjustable frequency, high output current, PWM regulator that integrates a high-side, P-channel MOSFET and a low-side, N-channel MOSFET. The A8651 incorporates current-mode control to provide simple compensation, excellent loop stability, and fast transient response. The A8651 uses external compensation to accommodate a wide range of power components to optimize transient response without sacrificing stability. The A8651 regulates input voltages from 2.5 to 5.5 V, down to output voltages as low as 0.8 V and is able to supply up to 2 A of load current per regulator.

The A8651 features include an externally adjustable and synchronizable switching frequency, an externally set soft-start time to minimize inrush currents, independent EN inputs, and independent NPOR outputs with either 7.5 ms (A8651) or 120 µs (A8651-1) delay. The sleep mode current of the A8651 control circuitry is less than 5 µA. Protection features include VIN undervoltage lockout (UVLO), pulse-by-pulse overcurrent protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8651 provides open-circuit, adjacent pin short-circuit, and short-to-ground protection at every pin to satisfy the most demanding automotive applications.

Continued on the next page…

APPLICATIONS:

- GPS/infotainment
- Automotive audio
- Home audio
- Network and telecom



Typical Application Diagram

DESCRIPTION (CONTINUED)

The A8651 device is available in a 20-pin TSSOP package with exposed thermal pad for enhanced thermal dissipation (suffix LP). It is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A, (°C)	Package	Packing [1]	Leadframe Plating
~~A8651KLPTR-T~~ [2]	–40 to 125	20-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel	100% matte tin
A8651KLPTR-T-1				

[1] Contact Allegro™ for additional packing options.
[2] Part variant discontinued. Date of status change: September 1, 2016. Suggested replacement: A8651KLPTR-T-1.

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN1 and VIN2 to GND	V_{IN}		–0.3 to 6.0	V
SW1 and SW2 to GND[2]	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0 to V_{IN} +2.0	V
All Other Pins	–		–0.3 to 6.0	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[2] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

[2] SW1 and SW2 have internal clamp diodes to GND and V_{IN}. Applications that forward bias these diodes should take care not to exceed the A8651 package power dissipation limits.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	32	°C/W

[1]Additional thermal information available on the Allegro website.

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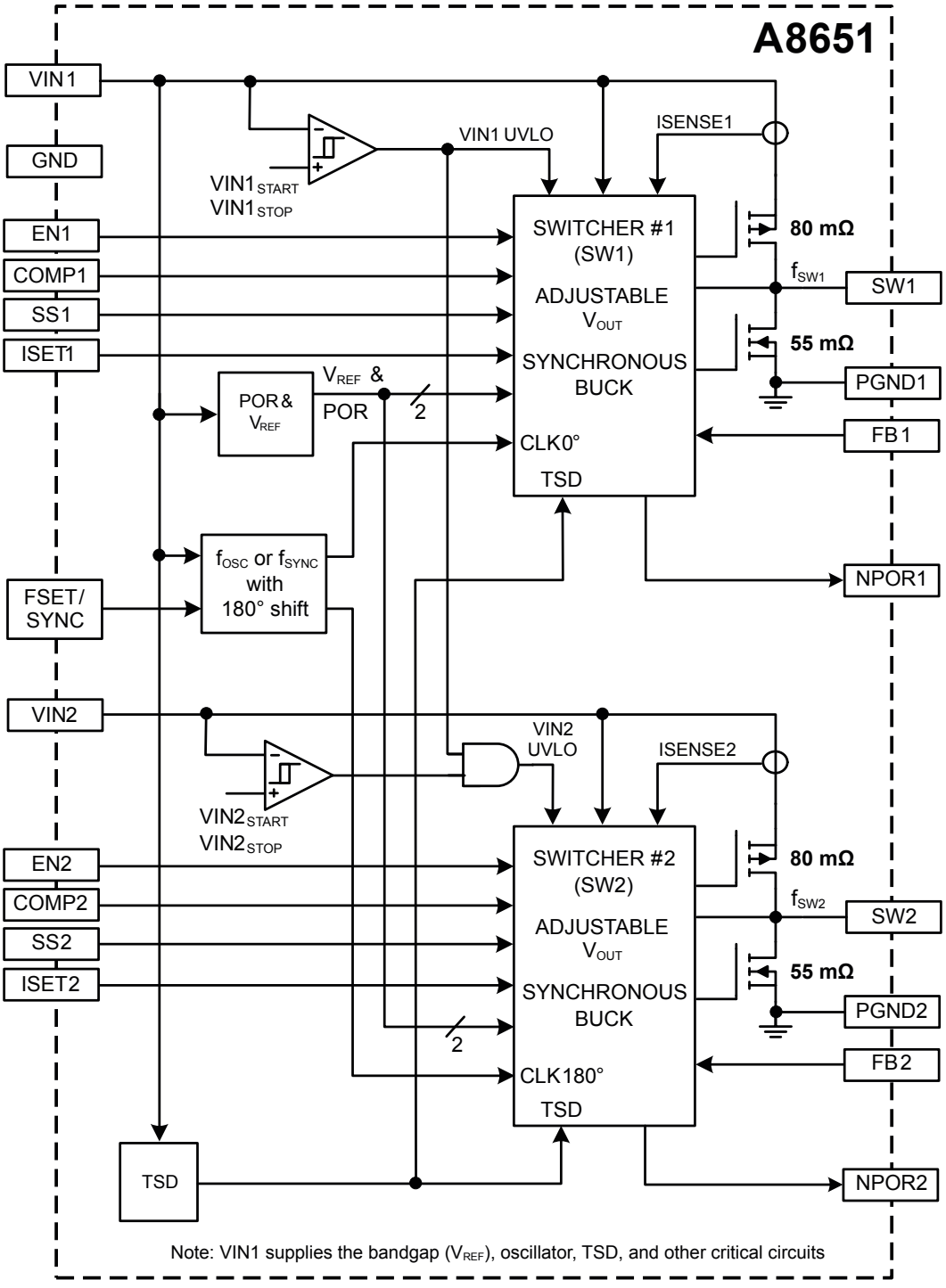

Top-Level Functional Block Diagram

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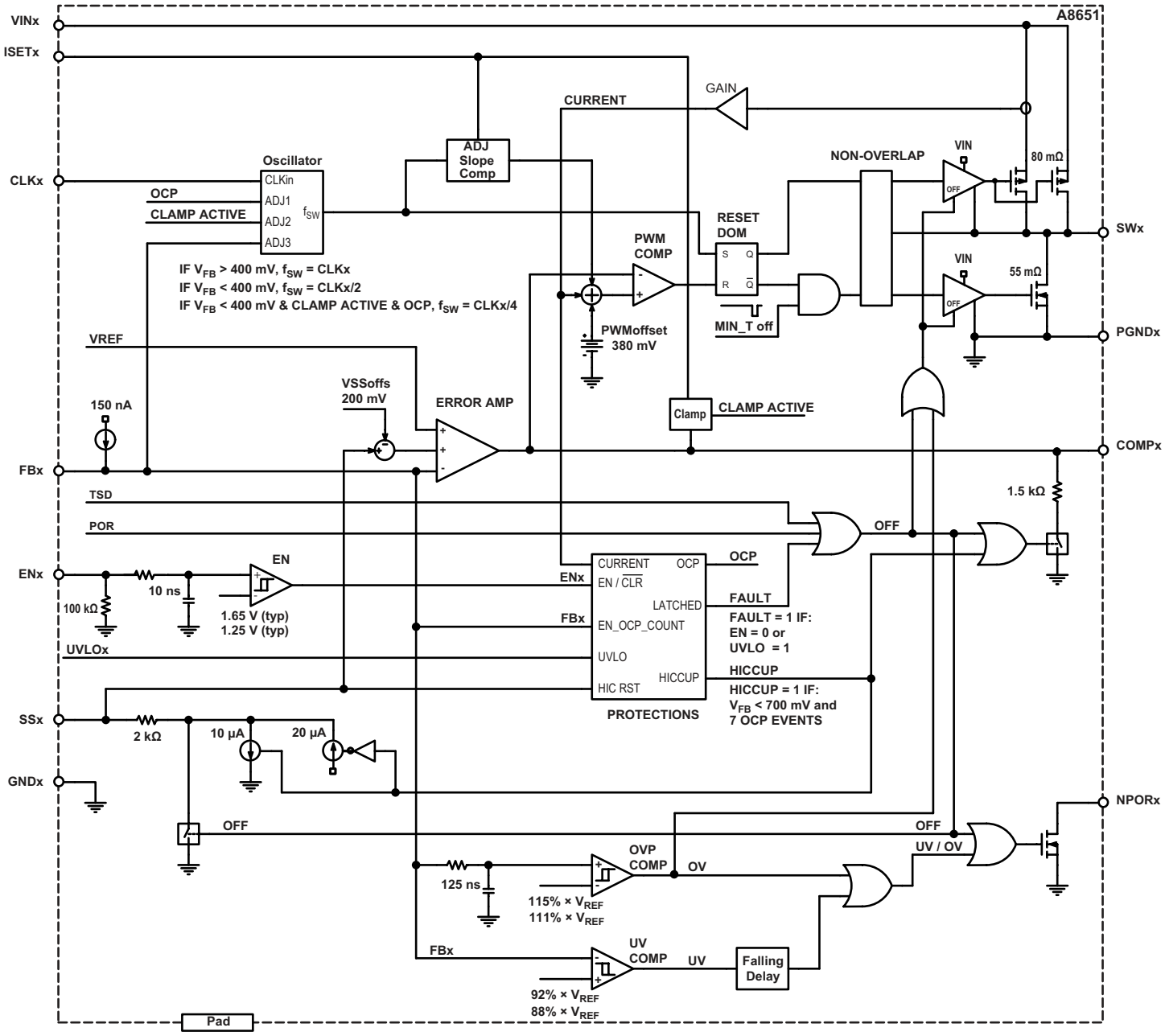

1 of 2 regulators shown

Detailed Functional Block Diagram

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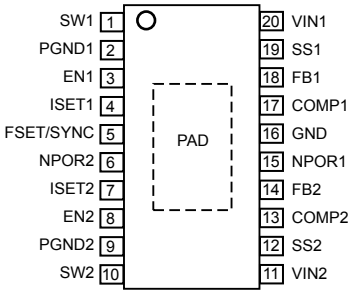
Pinout Diagram and Thermal Characteristics



Package LP, 20-Pin TSSOP with Exposed Thermal Pad Pinout Diagram

Terminal List Table

Number	Name	Function
1, 10	SW1, SW2	The drains of the internal high-side P-channel MOSFETs. The output inductors should be connected to these pins. The output inductors should be placed as close as possible to these pins and be connected with relatively wide traces.
2, 9	PGND1, PGND2	Power ground pins for switcher 1 and switcher 2.
3, 8	EN1, EN2	Inputs to enable switcher 1 and/or enable switcher 2.
4, 7	ISET1, ISET2	Pulse–by-pulse current limit setting pins.
5	FSET/SYNC	A resistor, R_{FSET}, from this pin to GND sets the base PWM switching frequency (f_{OSC}). If an external clock is AC-coupled to this pin by a 22 pF capacitor, the switching frequency of the regulator can be increased higher than f_{OSC}.
6, 15	NPOR2, NPOR1	Active low, open-drain fault indication outputs, with fixed delay.
11, 20	VIN2, VIN1	Power inputs for the control circuits and the sources of the internal high-side P-channel MOSFETs. VIN1 is the primary supply and must be present for the A8651 to operate. At least one high quality ceramic capacitor must be placed very close to these pins.
12, 19	SS2, SS1	Soft-start pins. Connect a capacitor, from these pins to GND to set the soft-start time. These capacitors also determine the hiccup period during an overcurrent condition.
13, 17	COMP2, COMP1	Outputs of the error amplifiers and compensation nodes for the current mode control loops. Connect a series RC network from these pins to GND for loop compensation. See the Design and Component Selection section of this datasheet for further details.
14, 18	FB2, FB1	Feedback (negative) inputs to the error amplifiers. Connect a resistor divider from the converter output nodes to these pins to program the output voltages.
16	GND	Ground.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.

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ELECTRICAL CHARACTERISTICS: Valid at $V_{IN1} = V_{IN2} = 5$ V, –40°C ≤ $T_A = T_J$ ≤ 125°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS						
Operating Input Voltage Range	V_{IN}		2.5	–	5.5	V
Undervoltage Lockout (UVLO) Start Threshold	$V_{INSTART}$	$V_{IN1} = V_{IN2}$, rising	2.00	2.22	2.45	V
Undervoltage Lockout (UVLO) Stop Threshold	V_{INSTOP}	$V_{IN1} = V_{IN2}$, falling	1.80	2.02	2.25	V
Undervoltage Lockout (UVLO) Hysteresis	$V_{UVLO(HYS)}$		–	200	–	mV
INPUT CURRENTS						
Input Quiescent Current	I_Q	$V_{EN1} = V_{EN2} = 5$ V, $V_{FB1} = V_{FB2} = 1$ V, no PWM switching	–	3	6	mA
Input Sleep Supply Current	I_{QSLEEP}	$V_{INx} = V_{SWx} = 5$ V, $V_{EN1} = V_{EN2} \le 0.4$ V	–	0.2	5	µA
REFERENCE VOLTAGE						
Reference (Feedback) Voltage	V_{REF}	2.5 V < $V_{IN1} = V_{IN2}$ < 5.5 V, $V_{FBx} = V_{COMPx}$	792	800	808	mV
ERROR AMPLIFIER						
Feedback Input Bias Current [1]	I_{FB}	$V_{COMPx} = 1.5$ V, V_{FBx} regulated so that $I_{COMPx} = 0$ A	–	–150	–300	nA
Open Loop Voltage Gain [2]	A_{VOL}		–	65	–	dB
Transconductance	g_m	$I_{COMPx} = 0$ µA, $V_{SSx} > 500$ mV	550	750	950	µA/V
		0 V < V_{SSx} < 500 mV	–	250	–	µA/V
Source Current	$I_{EA(SRC)}$	$V_{FBx} < 0.8$ V, $V_{COMPx} = 1.5$ V	–	–50	–	µA
Sink Current	$I_{EA(SINK)}$	$V_{FBx} > 0.8$ V, $V_{COMPx} = 1.5$ V	–	+50	–	µA
Maximum Output Voltage	$V_{EAVO(max)}$		1.00	1.25	1.50	V
COMP Pulldown Resistance	R_{COMP}	FAULT = 1, HICCUP = 1 or $V_{EN1} = V_{EN2} \le 0.4$ V	–	1.5	–	kΩ
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET}$	V_{COMPx} for 0% duty cycle	–	380	–	mV
High-Side MOSFET Minimum Controllable On-Time	$t_{ON(MIN)}$		–	65	105	ns
Low-Side MOSFET Minimum On-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, 2 × t_{OFF}	–	50	100	ns
Gate Driver Non-Overlap Time [2]	t_{OFF}		–	15	–	ns
COMP to SW Current Gain	g_{mPOWER}		–	4.5	–	A/V
Slope Compensation [2]	S_E	$R_{SETx} = 41.2$ kΩ, $f_{SW} = 2.0$ MHz	2.1	2.5	2.9	A/µs
		$R_{SETx} = 41.2$ kΩ, $f_{SW} = 0.35$ MHz	0.36	0.44	0.51	A/µs
		$R_{SETx} = 30.9$ kΩ, $f_{SW} = 2.0$ MHz	1.0	1.4	1.9	A/µs
		$R_{SETx} = 30.9$ kΩ, $f_{SW} = 0.35$ MHz	0.17	0.25	0.35	A/µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at $V_{IN1} = V_{IN2} = 5$ V, $-40°C \le T_A = T_J \le 125°C$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET PARAMETERS						
High-Side MOSFET On-Resistance	$R_{DS(on)HS}$	I_{DSx} = 100 mA	–	80	–	mΩ
SW Node Rise Time [2]	$t_{r(SW)}$		–	12	–	ns
High-Side MOSFET Leakage Current	$I_{DSS(HS)}$	$V_{ENx} \le 0.4$ V, $V_{SWx} = 0$ V, $V_{INx} = 5$ V, $-40°C < T_A = T_J < 85°C$ [3]	–	–	4	µA
		$V_{ENx} \le 0.4$ V, $V_{SWx} = 0$ V, $V_{INx} = 5$ V, $T_A = T_J = 125°C$	–	–	25	µA
Low-Side MOSFET ON Resistance	$R_{DS(on)LS}$	I_{DSx} = 100 mA	–	55	–	mΩ
Low-Side MOSFET Leakage Current	$I_{DSS(LS)}$	$V_{ENx} \le 0.4$ V, $V_{SWx} = 5$ V, $-40°C < T_A = T_J < 85°C$ [3]	–	–	1	µA
		$V_{ENx} \le 0.4$ V, $V_{SWx} = 5$ V, $T_A = T_J = 125°C$	–	–	10	µA
OSCILLATOR FREQUENCY						
Oscillator Frequency	f_{OSC}	R_{FSET} = 10.2 kΩ	1.98	2.20	2.45	MHz
		R_{FSET} = 24.9 kΩ	0.90	1.00	1.10	MHz
		R_{FSET} = 82.5 kΩ	325	375	425	kHz
SW1 to SW2 Phase Delay [2]	$\Phi_{1,2}$		–	180	–	degrees
FSET/SYNC INPUT						
FSET/SYNC High Threshold	$V_{FSETSYNC(H)}$		–	–	1.8	V
FSET/SYNC Low Threshold	$V_{FSETSYNC(L)}$		0.4	–	–	V
FSET/SYNC Pin Voltage	$V_{FSETSYNC}$	Without external SYNCin signal	–	0.8	–	V
FSET/SYNC Pin Current	$I_{FSETSYNC}$	Without external SYNCin signal	9	–	90	µA
Maximum SYNC Frequency	f_{SYNCM}		–	–	2.5	MHz
SYNC Frequency Range [2]	f_{SYNC}		1.2 × f_{OSC}	–	1.5 × f_{OSC}	–
SYNC Duty Cycle [2]	D_{SYNC}		50	60	70	%
Synchronization Minimum On-Time	t_{ONSYNC}		150	–	–	ns
Synchronization Minimum Off-Time	$t_{OFFSYNC}$		150	–	–	ns
ENABLE INPUTS						
EN High Threshold	V_{ENIH}	V_{ENx} rising	–	–	1.8	V
EN Low Threshold	V_{ENIL}	V_{ENx} falling	0.8	–	–	V
EN Hysteresis	V_{ENHYS}	$V_{ENIH} - V_{ENIL}$	–	200	–	mV
EN Input Resistance	R_{EN}		50	100	–	kΩ
EN Shutdown Delay [2]	$t_{dEN(SD)}$	From EN_X transitioning low to SWx switching stops	0	5	10	µs

[2] Ensured by design and characterization; not production tested.
[3] Specifications at 25°C or 85°C are ensured by design and characterization, not production tested at these temperatures.

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ELECTRICAL CHARACTERISTICS (continued): valid at $V_{IN1} = V_{IN2} = 5$ V, –40°C ≤ $T_A = T_J \leq 125$°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OVERCURRENT PROTECTION (OCP) AND HICCUP MODE						
Pulse-by-Pulse Current Limit	I_{LIM}	R_{SET} = 41.2 kΩ, duty cycle = 5%	3.5	4.1	4.7	A
		R_{SET} = 41.2 kΩ, duty cycle = 90% [2]	2.2	3.0	3.8	A
		R_{SET} = 30.9 kΩ, duty cycle = 5%	1.9	2.4	2.9	A
		R_{SET} = 30.9 kΩ, duty cycle = 90% [2]	1.1	1.8	2.3	A
Hiccup Disable Threshold	V_{HICDIS}	V_{FBx} rising	–	740	–	mV
Hiccup Enable Threshold	V_{HICEN}	V_{FBx} falling	–	700	–	mV
OCP / HICCUP Count Limit [2]	OCP_{LIMIT}	HICCUP enabled (see Functional Block diagram), OCP pulses	–	7	–	counts
SOFT-START (SS PIN)						
Soft-Start Offset Voltage	V_{SSOFFS}	V_{SSx} rising due to I_{SSSU}	100	200	270	mV
Soft-Start Fault/Hiccup Reset Voltage	$V_{SSRESET}$	V_{SSx} falling due to I_{SSHIC}	–	120	185	mV
Soft-Start Startup (Source) Current	I_{SSSU}	V_{SSx} = 1 V, HICCUP = FAULT = 0 (see Functional Block diagram)	–10	–20	–30	µA
Soft-Start Hiccup (Sink) Current	I_{SSHIC}	V_{SSx} = 0.5V, HICCUP = 1 (see Functional Block diagram)	5	10	20	µA
Soft-Start Input Resistance	R_{SS}	FAULT (see Functional Block diagram) = 1 or ENx = 0	–	2	–	kΩ
Soft-Start to V_{OUT} Delay Time	$t_{SS(DELAY)}$	C_{SSx} = 10 nF	–	85	–	µs
V_{OUT} Soft-Start Ramp Time	t_{SS}	C_{SSx} = 10 nF	–	400	–	µs
Soft-Start Switching Frequency	$f_{SW(SS)}$	0 V < V_{FBx} < 400 mV, $V_{COMPx} = V_{EAVO(max)}$, $I_{DSx} > I_{LIMx}$ [2]	–	f_{OSC} / 4	–	–
		0 V < V_{FBx} < 400 mV	–	f_{OSC} / 2	–	–
		V_{FBx} > 400 mV	–	f_{OSC}	–	–
NPOR OUTPUTS						
NPOR Undervoltage Threshold	V_{NPORUV}	Percentage of V_{REF}, V_{FBx} rising	89	92	95	%
NPOR Undervoltage Hysteresis	$V_{NPORUVhys}$	Percentage of V_{REF}, V_{FBx} falling	2	4	6	%
NPOR Overvoltage Threshold	V_{NPOROV}	Percentage of V_{REF}, V_{FBx} rising	112	115	118	%
NPOR Overvoltage Hysteresis	$V_{NPOROVhys}$	Percentage of V_{REF}, V_{FBx} falling	2	4	6	%
NPOR Rising Delay (A8651)	t_{NPOR}		4.0	7.5	11	ms
NPOR Rising Delay (A8651-1)			65	120	175	µs
NPOR Low Output Voltage	$V_{NPOR(L)}$	2.5 V < $V_{IN1} = V_{IN2}$ < 5 V, I_{NPOR} = 4 mA	—	—	400	mV
		$V_{IN1} = V_{IN2}$ =1.2 V, I_{NPOR} = 2 mA	—	—	800	mV
NPOR Leakage Current [1]	$I_{NPOR(LEAK)}$	V_{NPORx} = 3.3 V	—	—	1	µA
THERMAL PROTECTION (TSD)						
Thermal Shutdown Threshold [2]	$T_{SD(th)}$	Temperature rising	155	170	185	°C
Thermal Shutdown Hysteresis [2]	$T_{SD(HYS)}$	Temperature falling	–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization; not production tested.

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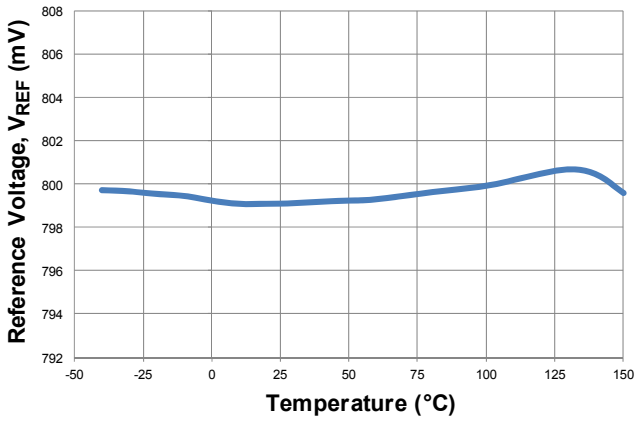
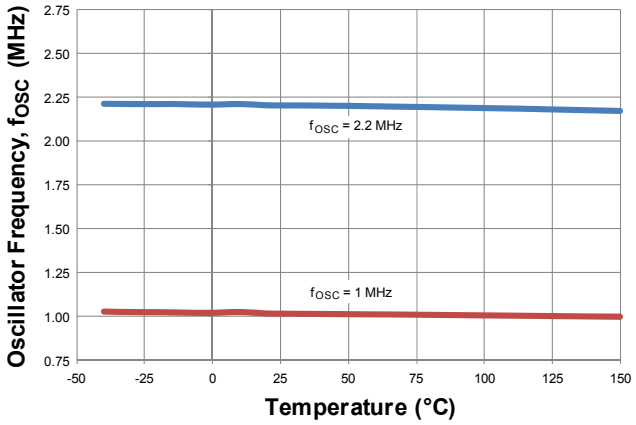
Characteristic Performance

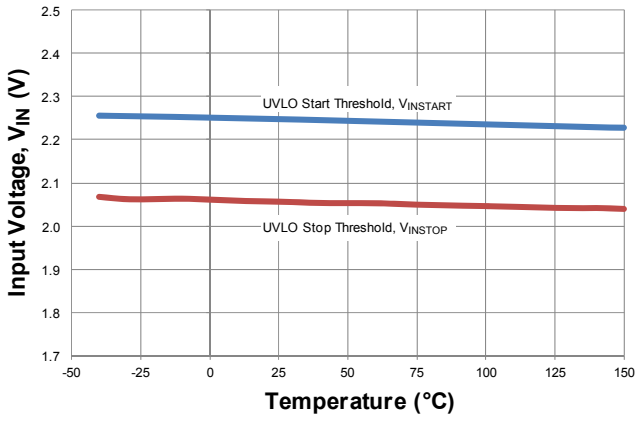
Reference Voltage versus Temperature



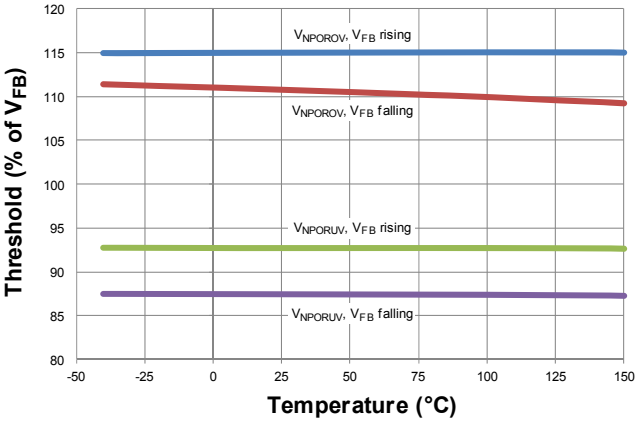
Oscillator Frequency versus Temperature



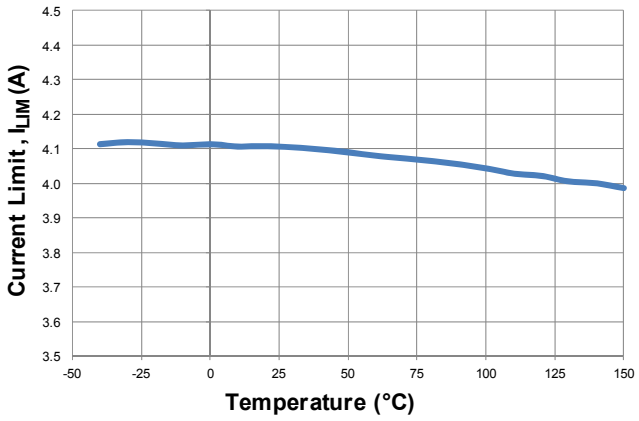
VIN UVLO Start and Stop Thresholds versus Temperature



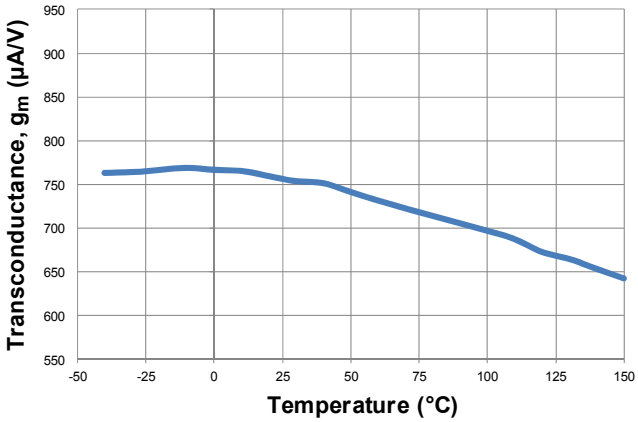
NPOR Overvoltage and Undervoltage Thresholds versus Temperature



Pulse-by-Pulse Current Limit at $t_{ON(MIN)}$ versus Temperature



Error Amplifier Transconductance versus Temperature



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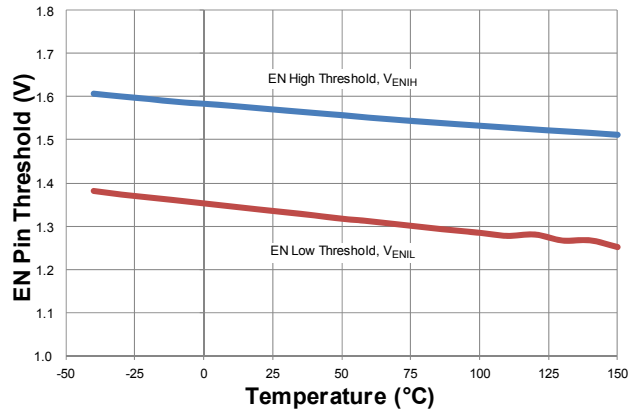
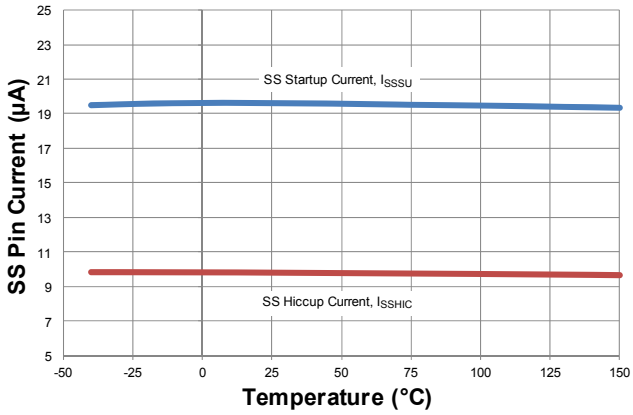
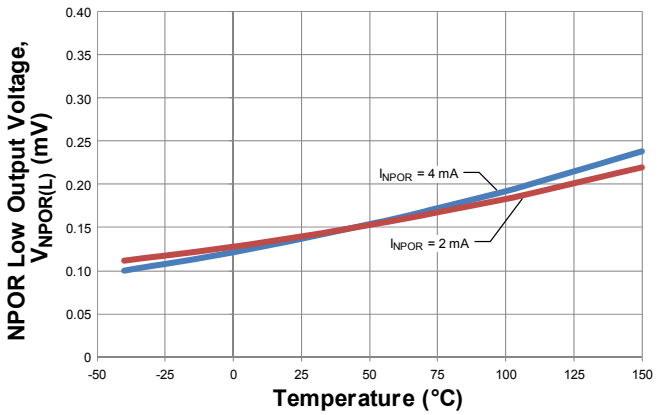
Enable High and Low Thresholds versus Temperature



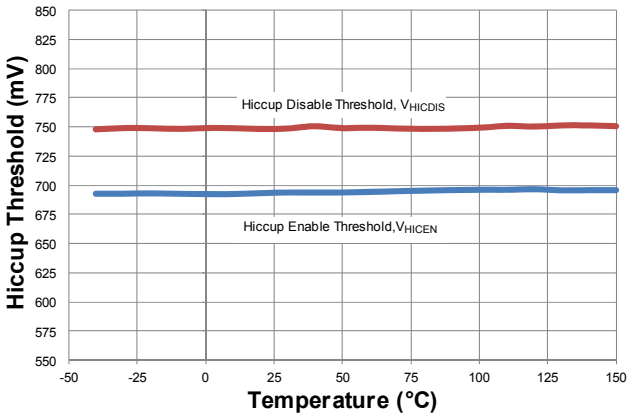
Soft Start Startup and Hiccup Currents versus Temperature



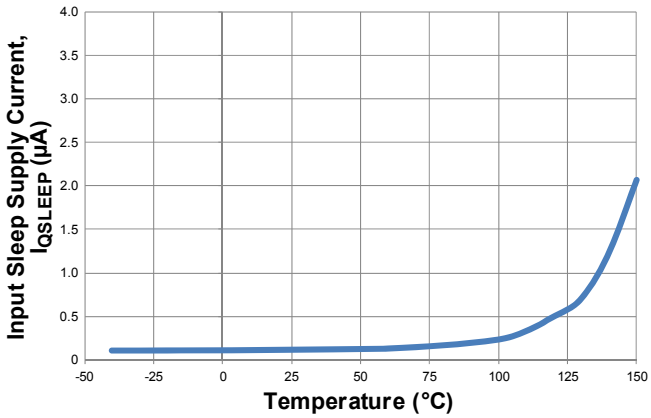
NPOR Low Output Voltage versus Temperature



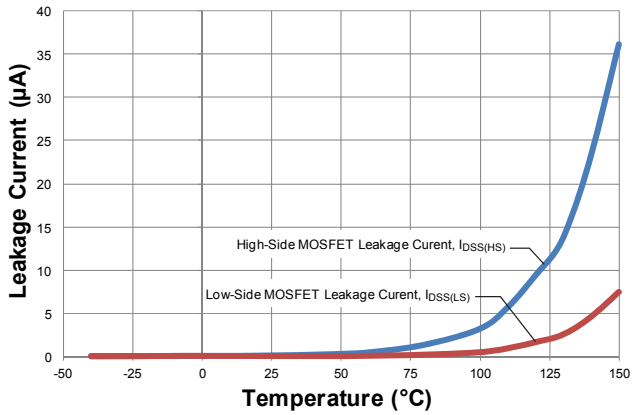
Hiccup Enable and Disable Thresholds versus Temperature



Input Sleep Supply Current versus Temperature



High- and Low-Side MOSFETs Leakage Current versus Temperature



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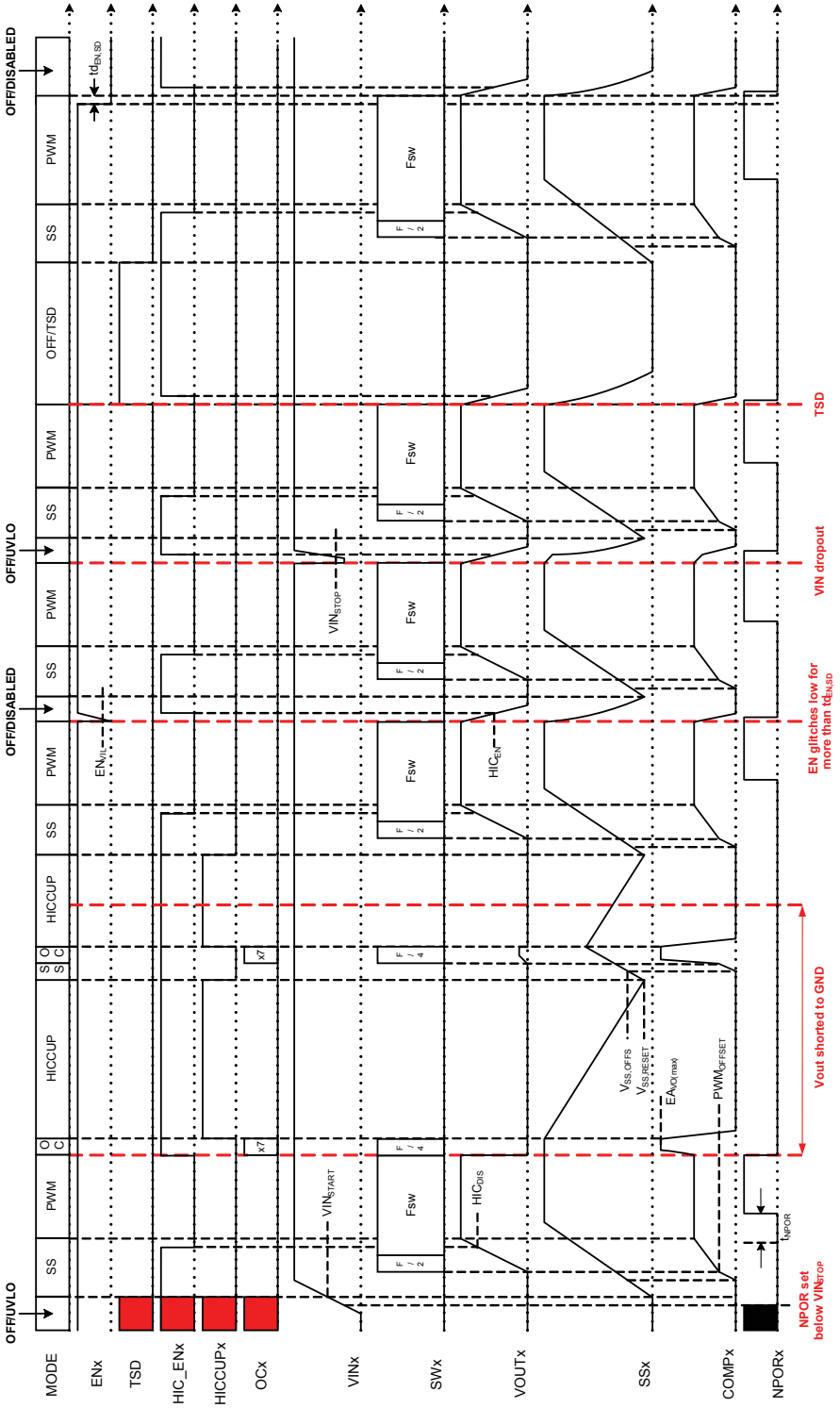
Timing Diagram (one of two regulators shown)



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FUNCTIONAL DESCRIPTION

Overview

The A8651 is a dual synchronous PWM regulator that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. The A8651 employs current mode control to provide fast transient response, simple compensation, and excellent stability. The features of the A8651 include, for each of the two regulators: a precision reference, an adjustable switching frequency, a transconductance error amplifier, an enable/synchronization input, integrated high-side and low-side MOSFETs, adjustable Soft-Start, pre-bias startup, low-current sleep mode, and a Power-On Reset output (NPOR). The protection features of the A8651 include undervoltage lockout (UVLO), pulse-by-pulse overcurrent protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8651 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short-circuit protection.

Reference Voltage

The A8651 incorporates an internal reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1% across the operating temperature range. The output voltage for each of the regulators is adjusted by connecting a resistor divider (R_{FB1}-R_{FB2} and R_{FB3}-R_{FB4} in the Typical Application diagram) from V_{OUTx} to the corresponding FBx pin of the A8651.

Oscillator/Switching Frequency (R_{FSET}, f_{OSC})

The PWM switching frequency of the A8651 is adjustable from 350 kHz to 2.2 MHz and has an accuracy of about ±10% across the operating temperature range. Connecting a resistor (R_{FSET}) from the FSET/SYNC pin to GND, as shown in the Typical Application diagram, sets the base switching frequency, f_{OSC}. An FSET/SYNC resistor with ±1% tolerance is recommended. A graph of switching frequency versus R_{FSET} resistor value is shown in the Design and Component Selection section of this datasheet.

Transconductance Error Amplifier

The transconductance error amplifier's primary function is to regulate the converter's output voltage. The error amplifier for one of the regulators is shown in Figure 1. It is shown as a three-terminal input device with two positive and one negative input. The negative input is simply connected to the FBx pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft-start and regulation. The error amplifier performs an "analog OR" selection between its two positive inputs. The error amplifier regulates to either the soft-start pin voltage minus 200 mV or the A8651's internal reference, whichever is lower.

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier output (COMPx pin) to GND as shown in the Typical Applications diagram. In some applications, an additional, low-value capacitor (C_P) may be connected in parallel with the R_Z-C_Z compensation network to reduce the loop gain at higher frequencies. However, if the C_P capacitor is too large, the phase margin of the converter may be reduced.

If the regulator is disabled or a fault occurs, the corresponding COMPx pin is immediately pulled to GND via approximately 1.5 kΩ and PWM switching is inhibited. During startup (V_{SSx} < 500 mV), the transconductance of the error amplifier is reduced to approximately one-third of the normal operating level to minimize transients when the system is requesting on-times less than or equal to the minimum controllable on-time.

Slope Compensation

The A8651 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the Detailed Functional Block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset ($V_{PWMOFFSET}$). The amount of slope compensation is scaled directly with the switching frequency.

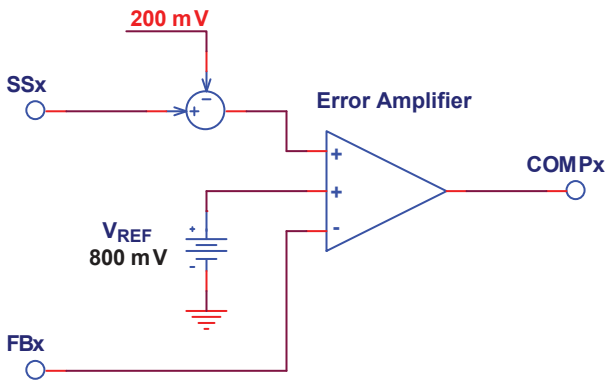

Figure 1: The A8651 Error Amplifier (for one regulator)

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ENx, VINx, and Sleep Mode

The A8651 provides two independent inputs, VIN1 and VIN2, to sequence the output voltages after the A8651 is powered up. However, VIN1 is the primary supply input. VIN1 must be greater than $V_{INSTART}$ or the A8651 will not come out of sleep mode. VIN2 can start or stop regulator 2 but cannot wake up the A8651.

If the voltage at EN1 or EN2 is driven below V_{ENIL} (800 mV) for more than $t_{dEN(SD)}$ (approximately 5 µs), the regulator stops switching.

In sleep mode (EN1< V_{ENVIL}), for more than $t_{dEN(SD)}$, the control circuits are de-biased and draw less than 5 µA from V_{IN}. However, the total current drawn by the VIN pin will be the sum of the current drawn by the control circuitry (I_{QSLEEP}) plus any leakage due to the high-side MOSFETs ($I_{DSS(HS)}$).

Synchronization (FSET/SYNC)

By using a 22 pF capacitor (C_{SYNC}) to AC-couple an external clock to the FSET/SYNC pin, as shown in Figure 2, the switching frequency of the A8651 can by increased from 1.2 × f_{OSC} to 1.5 × f_{OSC}. In these equations, f_{OSC} is the typical frequency determined by the R_{FSET} resistor. The applied SYNC waveform must satisfy the conditions shown in the Electrical Characteristics table. The SYNC waveform must simultaneously satisfy three conditions for all operating frequencies: duty cycle (D_{SYNC}), minimum on-time (t_{ONSYNC}), and minimum off-time ($t_{OFFSYNC}$). At relatively low frequencies (<1 MHz), the duty cycle will be the primary specification to satisfy; however, at higher frequencies (>2 MHz), the minimum on-time and minimum off-time will be the primary specifications to satisfy.

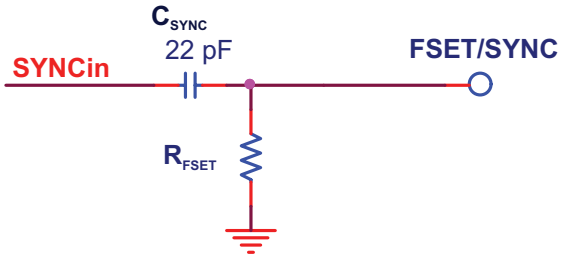

Figure 2: FSET/SYNC AC-Coupling

Power MOSFETs

The A8651 regulators each include an 80 mΩ, high-side P-channel MOSFET capable of delivering up to 4.1 A at a 5% duty cycle. The A8651 regulators also each include a 55 mΩ, low-side N-channel MOSFET to provide synchronous rectification.

The low-side MOSFET continues to conduct when the inductor current crosses zero to maintain constant conduction mode (CCM). This helps minimize EMI/EMC for noise sensitive applications by eliminating the SW high-frequency ringing associated with discontinuous conduction mode (DCM).

When the A8651 is disabled, via the ENx input or a fault condition, the A8651 output stage is tri-stated by turning off both the high-side and low-side MOSFETs.

Pulse-Width Modulation (PWM)

A high-speed PWM comparator, capable of pulse widths less than 105 ns, is included in each A8651 regulator. The inverting input of the comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and the PWM Ramp Offset ($V_{PWMOFFSET}$).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the upper MOSFET is turned on. When the summation of the DC offset, the current sense signal, and the slope compensation rises above the error amplifier voltage, the comparator resets the PWM flip-flop and the high-side MOSFET is turned off. If the output voltage of the error amplifier drops below the PWM Ramp Offset ($V_{PWMOFFSET}$) then a zero percent PWM duty cycle (pulse skipping) operation is achieved.

Current Sense Amplifier

A high-bandwidth current sense amplifier monitors the current in the high-side MOSFETs. The PWM comparator, the pulse-by-pulse current limiter, and the hiccup mode up/down counter require the current signal.

Soft-Start (Startup) and Inrush Current Control

Inrush currents to the converter are controlled by the soft-start function of the A8651. When the A8651 is enabled and all faults are cleared, the soft-start (SSx) pins source approximately 20 µA (I_{SSSU}) and the voltage on the soft-start capacitors (C_{SSx}) ramp

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upward from 0 V. When the voltage on a soft-start pin exceeds the Soft-Start Offset Voltage (V_{SSOFFS}, typically 200 mV measured at the SSx pin), the output of the error amplifier is released and shortly thereafter the high-side and low-side MOSFETs begin switching. As shown in Figure 3, there is a short delay ($t_{SS(DELAY)}$) between when the enable (ENx) pin transitions high and when the soft-start voltage reaches 200 mV to initiate PWM switching.

When the A8651 begins PWM switching, the error amplifier regulates the voltage at the FBx pin to the soft-start (SSx) pin voltage minus the soft-start offset voltage (V_{SSOFFS}). When PWM switching starts, the voltage at the SSx pin rises from 200 to 1000 mV, a difference of 800 mV, the voltage at the FBx pin rises from 0 to 800 mV, and the regulator output voltage rises from 0 V to the target setpoint determined by the feedback resistor divider (RFB1-RFB2 or RFB3-RFB4).

When the voltage at the soft-start pin reaches approximately 1000 mV, the error amplifier begin regulating using the A8651 internal reference, 800 mV. The voltage at the soft-start pin continues to rise to approximately V_{IN}. The soft-start functionality is shown in Figure 3.

If the A8651 is disabled or a fault occurs, the internal fault latch is set and the soft-start (SSx) pin is pulled to ground via approximately 2 kΩ. The A8651 clears the internal fault latch when the voltage at the SSx pin decays to approximately 120 mV ($V_{SSRESET}$).

If the A8651 enters hiccup mode, the capacitor (C_{SSx}) on the soft-start pin is discharged by a 10 µA current sink (I_{SSHIC}). Therefore, the soft-start pin capacitor value (C_{SSx}) controls the time between soft-start attempts. Hiccup mode operation is discussed in more detail in the Output Short Circuit (Hiccup Mode) Protection section of this datasheet.

When V_{FBx} > 400 mV, the PWM switching frequency is f_{OSC}. If V_{FBx} < 400 mV, the PWM switching frequency is reduced to f_{OSC} / 2 to provide the low duty cycles and accurate, stable control required during initial startup (when $V_{OUT} \approx 0$ V). Also, if V_{FBx} < 400 mV and COMPx = $V_{EAVO(max)}$, it can be assumed the regulator output is shorted to ground. In this case, the PWM switching frequency is further reduced to only f_{OSC}/4 to allow more off-time between PWM pulses. This is done to prevent staircasing of the output inductor current, which could result in damage to the inductor or the A8651. This is especially important when the input voltage is relatively high and the output of the regulator is either shorted or soft starting a relatively high output capacitance.

Pre-Biased Startup

If the output capacitors are pre-biased to some voltage, the A8651 modifies the normal startup routine to prevent discharging the output capacitors. Normally, the COMPx pin becomes active and PWM switching starts when the voltage at the soft-start (SSx) pin reaches 200 mV. With pre-bias at the output, the pre-bias voltage is sensed at the FBx pin. The A8651 does not start switching until the voltage at the soft-start pin increases to approximately V_{FBx} + 200 mV. At this soft-start pin voltage, the error amplifier output is released, the voltage at the COMPx pin rises, PWM

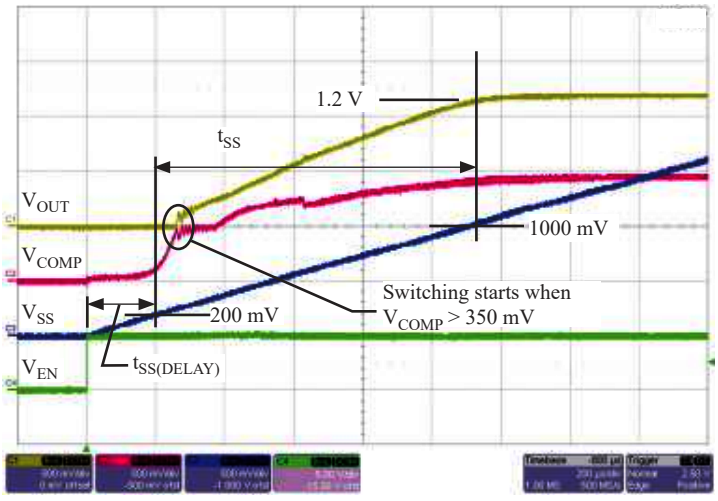

Figure 3: Startup to V_{OUTx} = 1.2 V, 2.0 A, with C_{SS} = 22 nF

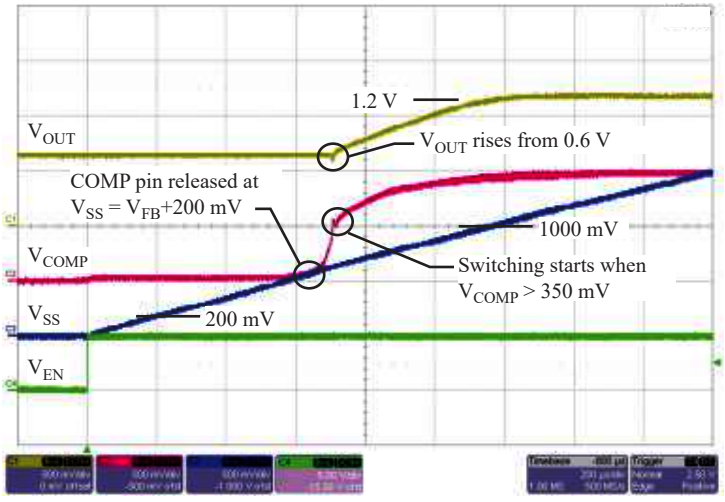

Figure 4: Startup to V_{OUTx} = 1.2 V, 2.0 A, with V_{OUT} pre-biased to 0.6 V

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switching starts, and V_{OUT} ramps upward, starting from the pre-bias level. Figure 4 shows startup when the output voltage is pre-biased to 0.9 V.

Active-Low Power-On Reset (NPORx)

The NPORx pins are open-drain outputs, so an external pull-up resistor must be connected to each. An internal comparator monitors the voltage at the FBx pin and controls the open-drain device at the NPORx pins. NPORx is pulled high by the external resistor approximately 7.5 ms after V_{OUTx} is within regulation. The NPORx output is pulled low if:

- $V_{FBx(RISING)}$ < 92% of the reference voltage, or
- $V_{FBx(RISING)}$ > 115% of the reference voltage, or
- EN is low, or
- V_{IN} UVLO occurs, or
- Thermal shutdown (TSD) occurs.

If the A8651 is running and VINx transitions low, then NPORx transitions low and remains low only as long as the internal circuitry is able to enhance the open-drain output device. When V_{IN} fully collapses, the NPORx pin returns to the high-impedance state. The NPOR comparator incorporates hysteresis to prevent chattering due to voltage ripple at the FBx pin.

Protection Features

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{INSTART}$). The UVLO comparator incorporates enough hysteresis ($V_{UVLO(HYS)}$) to prevent on-off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

THERMAL SHUTDOWN (TSD)

The A8651 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the upper thermal shutdown threshold ($T_{SD(th)}$, nominally 170°C), the voltages at the soft-start (SSx) and COMPx pins is pulled to GND and both the high-side and low-side MOSFETs are turned off. The A8651 stops PWM switching, but it does not enter the shutdown or sleep mode supply current levels. The A8651 automatically restarts when the junction temperature decreases more than the thermal shutdown hysteresis ($T_{SD(HYS)}$, 20°C (typ)).

OVERVOLTAGE PROTECTION (OVP)

The A8651 uses the FBx pins to provide a basic level of overvoltage protection. An overvoltage condition could occur if the load decreases very quickly or the COMPx pin or the regulator output are pulled high by some external voltage. When an overvoltage condition is detected, (1) NPORx is pulled low, and (2) PWM switching stops (the SWx node becomes high impedance). The COMPx and SSx pin voltages are not affected by OVP. If the regulator output decreases back to the normal operating range, NPORx transitions high and PWM switching resumes.

PULSE-BY-PULSE OVERCURRENT PROTECTION (OCP)

The A8651 monitors the current in the high-side P-channel MOSFET and if the current exceeds the pulse-by-pulse current overcurrent threshold (I_{LIM}), then the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The A8651 includes leading edge blanking to prevent false triggering of the pulse-by-pulse current limit when the high-side MOSFET is turned on. Pulse-by-pulse current limiting is always active.

A key feature of the A8651 is the ability to adjust the peak switch current limit. This can be useful when the full current capability of the regulator is not required for a given application. A smaller current limit may allow the use of power components with lower current ratings, thus saving space and reducing cost. A single resistor between the ISET pin and ground controls the current limit. Resistor values should be set in the range between 30.9 kΩ (for the lowest current limit setting) and 41.2 kΩ (for the highest current limit setting).

The maximum switch current is affected by slope compensation via the duty cycle. The A8651 is conservatively rated to deliver 2.0 ADC for most applications. However, the exact current the

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A8651 supports is heavily dependent on duty cycle, ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

The A8651 is designed to deliver more current at lower duty cycles and slightly less current at higher duty cycles. For example, the pulse-by-pulse current limit at 20% duty cycle is typically 3.85 A, but at 80% duty cycle the pulse limit is typically 3.10 A. Use Table 1a and Figure 5a, and Table 1b and Figure 5b to determine the real current limit given the duty cycle required for each application. Take care to do a careful thermal solution or thermal shutdown can occur.

OUTPUT SHORT-CIRCUIT (HICCUP MODE) PROTECTION

Hiccup mode protects the A8651 when the load is either too high or when the output of the converter is shorted to ground. When the voltage at the FBx pin is below the Hiccup Enable Threshold (V_{HICEN}, 700 mV (typ)), hiccup mode protection is enabled. When the voltage at the FBx pin is above the Hiccup Disable Threshold (V_{HICDIS}, 740 mV (typ)) hiccup mode protection is disabled.

Hiccup mode overcurrent protection monitors the number of overcurrent events using an up/down counter. An overcurrent pulse increments the counter by 1 and a PWM cycle without an

Table 1a. Pulse-by-Pulse Current Limit versus Duty Cycle

R_{SET} = 41.2 kΩ, f_{SW} = 2 MHz

Duty Cycle (%)	Pulse-by-Pulse Current Limit (A)		
	Min.	Typ.	Max.
5	3.42	4.04	4.65
20	3.17	3.86	4.51
40	2.83	3.61	4.31
60	–	3.37	4.12
80	–	3.12	3.92
90	–	3.00	3.83

Table 1b. Pulse-by-Pulse Current Limit versus Duty Cycle

R_{SET} = 30.9 kΩ, f_{SW} = 2 MHz

Duty Cycle (%)	Pulse-by-Pulse Current Limit (A)		
	Min.	Typ.	Max.
5	1.85	2.37	2.87
20	1.69	2.27	2.77
40	1.49	2.13	2.64
60	1.28	2.00	2.52
80	–	1.86	2.39
90	–	1.80	2.32

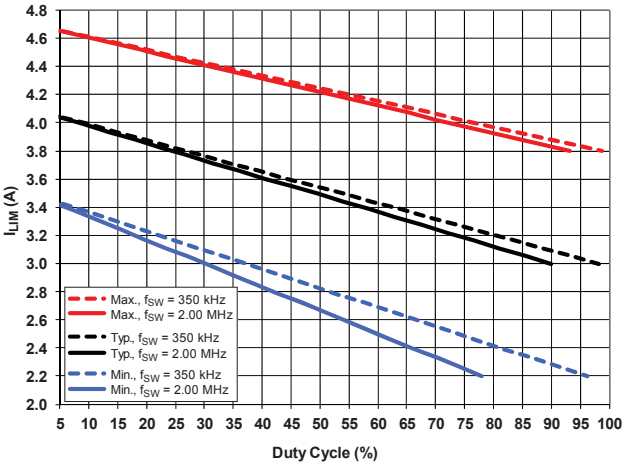

Figure 5a: Current Limit versus Duty Cycle, with R_{SET} = 41.2 kΩ

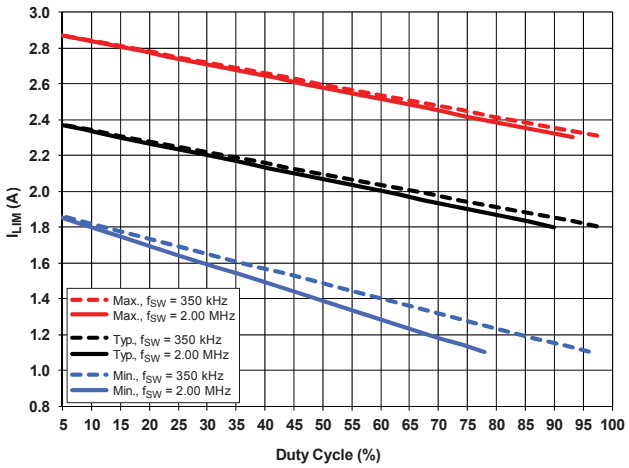

Figure 5b: Current Limit versus Duty Cycle, with R_{SET} = 30.9 kΩ

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overcurrent pulse decrements the counter by 1. If more than 7 consecutive overcurrents are detected, then the Hiccup latch is set and PWM switching is stopped. The Hiccup signal causes the COMPx pin to be pulled low with a relatively low resistance (1.5 kΩ). Hiccup mode also enables a current sink connected to the soft-start (SSx) pin (I_{SSHIC},10 µA), so when hiccup initially occurs, the voltage at the soft-start pin ramps downward. Hiccup mode operation is shown in Figure 6.

When the voltage at the soft-start pin decays to a low level ($V_{SSRESET}$, 120 mV (typ)), the hiccup latch is cleared and the 10 µA soft-start pin current sink is turned off. The soft-start pin resumes charging the soft-start capacitor with 20 µA, and the voltage at the soft-start pin ramps upward.

When the voltage at the soft-start pin exceeds the soft-start offset voltage (V_{SSOFFS}, 200 mV (typ)), the low-resistance pull-down at the COMPx pin is turned off. The error amplifier forces the voltage at the COMPx pin to ramp up quickly, and PWM switching begins. If the short-circuit at the converter output remains, another hiccup cycle occurs. Hiccup cycles repeat until the short-circuit is removed or the converter is disabled. If the short-circuit is removed, the A8651 soft-starts normally and the output voltage ramps to the operating level, as shown in Figure 6.

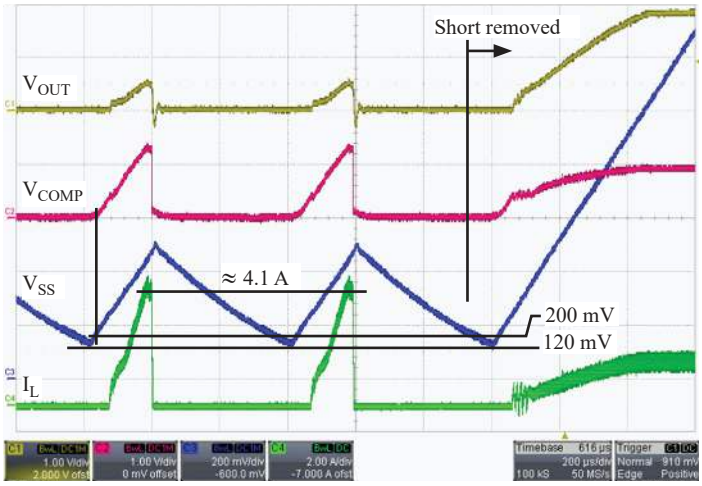

Figure 6: Hiccup Mode Operation and Recovery

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Table 2: Summary of A8651 Fault Modes and Operation

Fault Mode	V_{SS}	V_{COMP}	High-Side Switch	Low-Side Switch	NPOR	Reset Condition
Output hard short-to-ground (V_{OUT} and V_{FB} = 0 V)	Hiccup after V_{COMP} ≈ 1.25 V and 7 OC faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} / 4 if COMP ≈1.25 V and I_{LIM}	Active during t_{OFF}, off during hiccup	Depends on V_{OUT}	Automatic, remove the short
Output overcurrent and V_{FB} < V_{HICDIS}	Hiccup after V_{COMP} ≈ 1.25 V and 7 OC faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} / 4 if V_{COMP} ≈1.25 V and I_{LIM}	Active during t_{OFF}, off during hiccup	Depends on V_{OUT}	Automatic, decrease the load current
SW hard short to ground	Ramps to V_{IN}, hiccup may occur when the short is removed	Clamped to ≈1.25 V, pulled low if hiccup occurs	Controlled by V_{COMP}, turn off if V_{SW} ≈ 0 V and blanking time expires, f_{OSC} / 4	Active during t_{OFF}, off if hiccup occurs when the short is removed	Depends on V_{OUT}	Automatic, remove the short
SW soft short to ground	Hiccup after V_{COMP} ≈1.25 V and 7 OC faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} / 4 if V_{COMP} ≈1.25 V and I_{LIM}	Active during t_{OFF}, off during hiccup	Depends on V_{OUT}	Automatic, remove the short
FB pin open (V_{FB} floats high due to negative bias current)	Not affected	Transitions low via loop response as V_{FB} floats high	Off, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} if 400 mV < V_{FB}	Off, disabled if V_{COMP} < 200 mV	Pulled low when V_{FB} > 115% × V_{REF}	Automatic, connect the FB pin
Output overvoltage (V_{FB} > 115% × V_{REF})	Not affected	Transitions low via loop response because V_{FB} > V_{REF}	Off, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} if 400 mV < V_{FB}	Off, disabled if V_{COMP} < 200 mV	Pulled low when V_{FB} > 115% × V_{REF}	Automatic, V_{FB} returns to the normal range
Output undervoltage	Not affected	Transitions high via loop response	Controlled by V_{COMP}, f_{OSC} / 2 if 0 < V_{FB} < 400 mV, f_{OSC} if 400 mV < V_{FB}	Active during t_{OFF}	Pulled low when V_{FB} < 92% × V_{REF}	Automatic, V_{FB} returns to the normal range
Thermal shutdown (TSD)	Pulled low and latched until V_{SS} < $V_{SSRESET}$	Pulled low and latched until V_{SS} > $V_{SS(RELEASE)}$	Off	Off	Pulled low	Automatic, after the junction cools down

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DESIGN AND COMPONENT SELECTION

This section shows how to design and select external component values. For simplicity, the naming convention used here refers only to regulator 1, but the same design methods can be used for regulator 2.

Setting the Output Voltage (V_{OUT1}, R_{FBx})

The output voltage of the A8651 is determined by connecting a resistor divider from the output node (V_{OUT1}) to the FB1 pin as shown in Figure 7. There are trade-offs when choosing the value of the feedback resistors. If the series combination (R_{FB1}+R_{FB2}) is relatively low, then the light load efficiency of the regulator is reduced. So, to maximize the efficiency it is best to choose high values of resistors. On the other hand, if the parallel combination (R_{FB1} // R_{FB2}) is too high, then the regulator may be susceptible to noise coupling into the FB1 pin.

In general, the feedback resistors must satisfy the ratio shown in equation 1 to produce an output voltage, V_{OUT1}:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT1}}{0.8\ (V)} - 1 \qquad (1)$$

Table 3 shows the most common output voltages and recommended feedback resistors, assuming less than 0.2% efficiency loss at a light load of 100 mA and a parallel combination of 4 kΩ presented to the FB1 pin. For optimal system accuracy, it is recommended that the feedback resistors have ≤1% tolerances.

PWM Switching Frequency (R_{FSET})

The PWM switching frequency is set by connecting a resistor from the FSET/SYNC pin to ground. Figure 8 is a graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis).

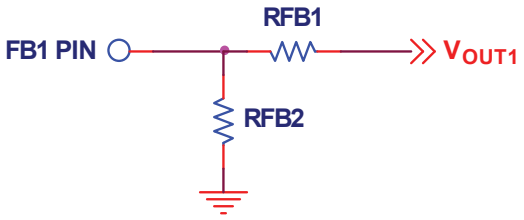

Figure 7: Connection for the Feedback Divider

Table 3. Recommended Feedback Resistors

V_{OUT1} (V)	R_{FB1} (V_{OUT1} to FB1 pin) (kΩ)	R_{FB2} (FB1 pin to GND) (kΩ)
1.2	6.04	12.1
1.5	7.50	8.45
1.8	9.09	7.15
2.5	12.4	5.76
3.3	16.5	5.23

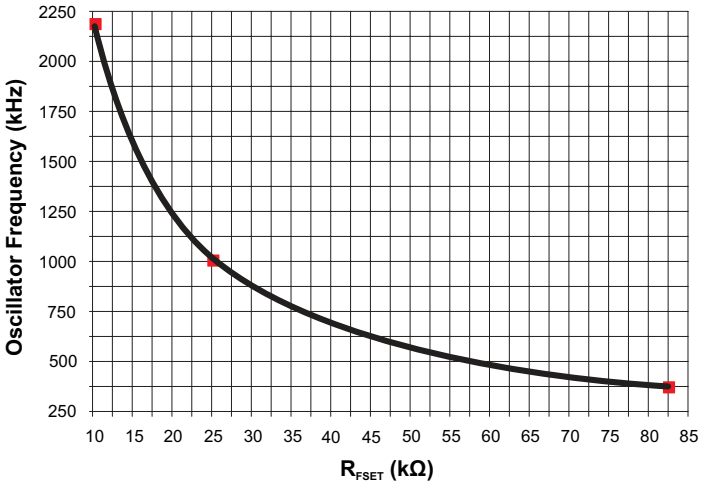

Figure 8. PWM Switching Frequency versus R_{FSET}

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To set a specific oscillator frequency (f_{osc}), the R_{FSET} resistor can be calculated as follows:

$$R_{FSET} = \left(\frac{f_{OSC}}{15456}\right)^{-1.186} \quad (2)$$

where f_{osc} is in kHz and R_{FSET} is in kΩ.

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time ($t_{ON(MIN)}$) of the A8651. If the application system required on-time is less than the A8651 minimum controllable on-time, then switch node jitter occurs and the output voltage has increased ripple or oscillations.

The PWM switching frequency should be calculated as follows:

$$f_{SWMAX} = \frac{V_{OUT1}}{t_{ON(MIN)} \times V_{IN1(MAX)}} \quad (3)$$

where V_{OUT1} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the A8651 (worst case is 105 ns), and $V_{IN1(MAX)}$ is the maximum required operational input voltage to the A8651 (not the peak surge voltage).

If the A8651 synchronization function is employed, then the base switching frequency should be chosen such that jitter does not result at the maximum synchronized switching frequency according to equation 3: $1.5 \times f_{SW} < f_{SWMAX}$ calculated by equation 3.

Output Inductor (L_O)

For a peak current mode regulator, it is common knowledge that, without adequate slope compensation, the system becomes unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8651 is a fixed value (S_E). Therefore, it is important to calculate an inductor value such that the falling slope of the inductor current (S_F) works well with the A8651 slope compensation.

Equations 4a and 4b can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the down slope of the inductor current.

$$\frac{V_{OUT1}}{2 \times S_E} \le L_{O1} \le \frac{V_{OUT1}}{S_E} \quad (4a)$$

where L_O is in µH and the slope compensation (S_E) is a function of switching frequency, as follows:

$$S_E = (0.054 \times R_{SET} - 0.96) \times f_{SW} \quad (4b)$$

where R_{SET} is in kΩ, f_{SW} is in MHz, and the calculated S_E is in A/µs.

Another limitation is shown in equation 5. This is based on a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency (this approach includes the duty cycle (D), which should be calculated at the minimum input voltage to insure optimal stability):

$$L_{O1} \ge \frac{V_{OUT1}}{S_E}\left(1 - 0.18 \times \frac{V_{IN1(MIN)}}{V_{OUT1}}\right) \quad (5)$$

To avoid dropout (saturation of the buck regulator), $V_{IN1(MIN)}$ must be approximately 0.75 to 1.0 V above V_{OUT1} when calculating the inductor value with equation 5.

If equations 4a or 5 yield an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 10% to 20% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8651. Ideally, for output short circuit conditions, the inductor should not saturate given the highest pulse-by-pulse current limit at minimum duty cycle ($I_{LIM(5\%)}$); 4.7 A. This may be too costly. At the very least, the inductor should not saturate given the peak operating current according to the following equation:

$$I_{PEAK} = 4.1 - \frac{S_E \times V_{OUT1}}{1.15 \times f_{SW} \times V_{IN1(MAX)}} \quad (6)$$

where $V_{IN1(MAX)}$ is the maximum continuous input voltage, such as 5.5 V.

Starting with equation 6 and subtracting half of the inductor ripple current provides us with an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle ($D = V_{OUT1} / V_{IN1}$):

$$I_{OUT1(DC)} \le 4.1 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT1} \times (1 - D)}{2 \times f_{SW} \times L_{O1}} \quad (7)$$

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After an inductor is chosen it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT1}) is a function of the output capacitors parameters: C_{OUT1}, ESR_{COUT1}, and ESL_{COUT1}:

$$\Delta V_{OUT1} = \Delta I_{L1} \times ESR_{COUT1} + \frac{V_{IN1} - V_{OUT1}}{L_{O1}} \times ESL_{COUT1} + \frac{\Delta I_{L1}}{8 f_{SW} C_{OUT1}} \quad (8)$$

The type of output capacitors determines which terms of equation 8 are dominant. For ceramic output capacitors the ESR_{COUT1} and ESL_{COUT1} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 8:

$$\Delta V_{OUT1} \leq \frac{\Delta I_{L1}}{8 f_{SW} C_{OUT1}} \quad (9)$$

To reduce the voltage ripple of a design using ceramic output capacitors simply: increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high, so the third term in equation 8 will be very small and the output voltage ripple will be determined primarily by the first two terms of equation 8:

$$\Delta V_{OUT1} = \Delta I_{L1} \times ESR_{COUT1} + \frac{V_{IN1}}{L_{O1}} \times ESL_{COUT1} \quad (10)$$

To reduce the voltage ripple of a design using electrolytic output capacitors simply: decrease the equivalent ESR_{COUT1} and ESL_{COUT1} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage changes by the amount:

$$\Delta V_{OUT1} = \Delta I_{L1} \times ESR_{COUT1} + \frac{di}{dt} \times ESL_{COUT1} \quad (11)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. The length of this time depends on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier brings the output voltage back to its nominal value.

The speed at which the error amplifier brings the output voltage back to the setpoint depends mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, and C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Input Capacitors

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor rms current rating must be higher than the expected rms input current to the regulator. Third, the capacitors must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the UVLO circuitry (nominally 200 mV for the A8651) at maximum loading and minimum input voltage.

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The input capacitor(s) must limit the voltage deviations at the VIN1 pin to something significantly less than the device UVLO hysteresis during maximum load and minimum input voltage. The following equation allows us to calculate the minimum input capacitance:

$$C_{IN1} \geq \frac{I_{OUT1} \times D \times (1-D)}{0.85 \times f_{SW} \times \Delta V_{IN1(MIN)}} \quad (12)$$

where $\Delta V_{IN1(MIN)}$ is chosen to be much less than the hysteresis of the V_{IN1} UVLO comparator ($\Delta V_{IN1(MIN)} \leq 100$ mV is recommended), and f_{SW} is the nominal PWM frequency.

The $D \times (1–D)$ term in equation 12 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on $I_{OUT1} = 2.0$ A, $f_{SW} = 85\%$ of 2 MHz, $D \times (1–D) = 0.25$, and $\Delta V_{IN1} = 100$ mV yields:

$$C_{IN} \geq \frac{2.0\ (A) \times 0.25}{1.7\ (MHz) \times 100\ (mV)} = 2.9\ \mu F$$

The input capacitors must deliver an rms current (I_{RMS}) according to the following formula:

$$I_{RMS} = I_{OUT1} \sqrt{D \times (1-D)} \quad (13)$$

where the duty cycle (D) is defined as:

$$D = V_{OUT1} / V_{IN1} \quad (14)$$

Figure 9 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 2.0 A or 0.8 Arms.

A good design should consider the DC-bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC-bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage.

Soft-Start and Hiccup Mode Timing (C_{SS1})

The soft-start time of the A8651 is determined by the value of the capacitance at the soft start pin, C_{SS1}. When the A8651 is enabled the voltage at the soft start pin (SS1) starts from 0 V and is charged by the soft-start current, I_{SSSU1}. However, PWM switching does not begin instantly because the voltage at the soft-start pin must rise above 200 mV. The soft-start delay ($t_{SS(DELAY)}$) can be calculated using the following equation:

$$t_{SS(DELAY)} = C_{SS1} \times \frac{200\ (mV)}{I_{SSSU}} \quad (15)$$

If the A8651 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the cycle-by-cycle overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors:

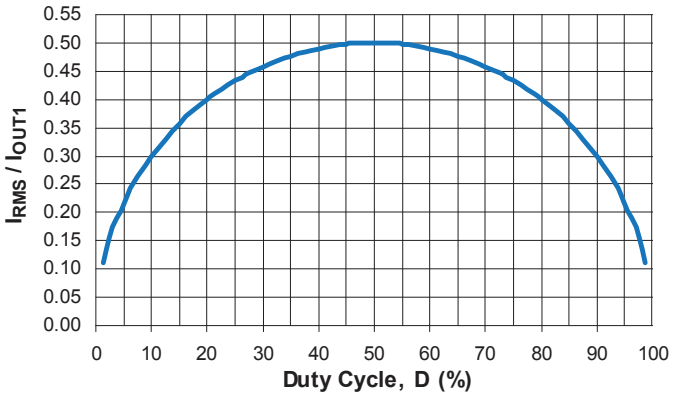

Figure 9: Normalized Input Capacitor Ripple versus Duty Cycle

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$$I_{COUT1} = C_{OUT1} \times V_{OUT1} / t_{SS} \quad (16)$$

is higher than the cycle-by-cycle current threshold, as shown in Figure 10. This phenomenon is more pronounced when using high value electrolytic type output capacitors. To avoid prematurely triggering hiccup mode, the soft-start capacitor, C_{SS1}, should be calculated according to:

$$C_{SS1} \geq \frac{I_{SSSU} \times V_{OUT1} \times C_{OUT1}}{0.8\ (V) \times I_{COUT1}} \quad (17)$$

where V_{OUT1} is the output voltage, C_{OUT1} is the output capacitance, I_{COUT1} is the amount of current allowed to charge the output capacitance during soft-start (recommend 0.1 A < I_{COUT1} < 0.3 A). Higher values of I_{COUT1} result in faster soft-start times. However, lower values of I_{COUT1} ensure that hiccup mode is not inappropriately triggered. Allegro recommends starting the design with an I_{COUT1} of 0.1 A and increasing it only if the soft-start time is too slow. If a non-standard capacitor value for C_{SS1} is calculated, the next larger value should be used.

The output voltage ramp time, t_{SS}, can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT1} \times \frac{C_{OUT1}}{I_{COUT1}} \quad (18)$$

or

$$t_{SS} = 0.8\ (V) \times \frac{C_{SS1}}{I_{SSSU}} \quad (19)$$

When the A8651 is in hiccup mode, the soft-start capacitor is used as a timing capacitor and sets the hiccup period. The soft-start pin charges the soft-start capacitor with I_{SSSU} during a startup attempt, and discharges the same capacitor with I_{SSHIC} between startup attempts. Because the ratio I_{SSSU} / I_{SSHIC} is approximately 2:1, the time between hiccups is about two times as long as the startup time. Therefore, the effective duty-cycle of the A8651 is very low and the junction temperature is kept low.

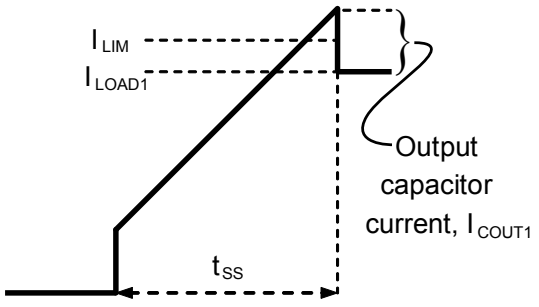

Figure 10. Output Current (I_{COUT1}) During Startup

Compensation Components (RZ, CZ, CP)

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8651, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* transfer function. The low frequency gain of this circuitry depends on the COMP1 to SW1 current gain (g_{mPOWER}), and the value of the load resistor (R_{L1}). The DC gain ($G_{CO(0HZ)}$) of the control-to-output is:

$$G_{CO(0Hz)} = g_{mPOWER} \times R_{L1} \quad (20)$$

The control-to-output transfer function has a pole (f_{P1}), formed by the output capacitance (C_{OUT1}) and load resistance (R_{L1}), located at:

$$f_{P1} = \frac{1}{2\pi \times R_{L1} \times C_{OUT1}} \quad (21)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT1}) and its associated ESR:

$$f_{Z1} = \frac{1}{2\pi \times ESR_{COUT1} \times C_{OUT1}} \quad (22)$$

For a design with very low-ESR type output capacitors (such as ceramic capacitors), the ESR zero, f_{Z1}, is usually at a very high frequency so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as happens with electrolytic output capacitors), then it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (discussed and identified later as f_{P3}).

A Bode plot of the control-to-output transfer function for the schematic shown in figure 15, with V_{OUT1} = 1.2 V, I_{OUT1} = 1.5 A,

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and R_{L1} = 0.8 Ω, is shown in Figure 11. The pole at f_{P1} can easily be seen at 8.8 kHz, while the ESR zero, f_{Z1}, occurs at a very high frequency, 4 MHz (this is typical for a design using ceramic output capacitors). Note, there is more than 90° of total phase shift because of the double-pole at half the switching frequency.

Next, consider the feedback resistor divider, (R_{FB1} and R_{FB2}), the error amplifier (gm), and its compensation network R_Z-C_Z-C_P. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$. In most cases, R_O > 2 MΩ, 1 kΩ < R_Z <100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low frequency gain of the control section ($G_{C(0Hz)}$) is formed by the feedback resistor divider and the error amplifier. It can be calculated as:

$$G_{C(0Hz)} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \times g_m \times R_O = \frac{V_{FB1}}{V_{OUT1}} \times g_m \times R_O = \frac{V_{FB1}}{V_{OUT1}} \times A_{VOL} \quad (23)$$

where

V_{OUT} is the output voltage,

V_{FB} is the reference voltage (0.8 V),

g_m is the error amplifier transconductance (750 µA/V), and

R_O is the error amplifier output impedance (A_{VOL}/g_m).

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier output impedance (R_O) and the C_Z compensation capacitor:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (24)$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (25)$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor:

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \quad (26)$$

A Bode plot of the error amplifier and its compensation network is shown in Figure 12, where f_{P2}, f_{P3}, and f_{Z2} are indicated on the Gain plot. Notice that the zero (f_{Z2} at 16 kHz) has been placed so that it is just above the pole at f_{P1} previously shown at 8.8 kHz in the control-to-output Bode plot (Figure 11). Placing f_{Z2} just above f_{P1} results in excellent phase margin, but relatively slow transient recovery time, as we will see later.

Finally, consider the combined Bode plot of both the control-to-output and the compensated error amplifier (Figure 13). Careful examination of this plot shows that the magnitude and phase of the entire system (red curve) are simply the sum of the error

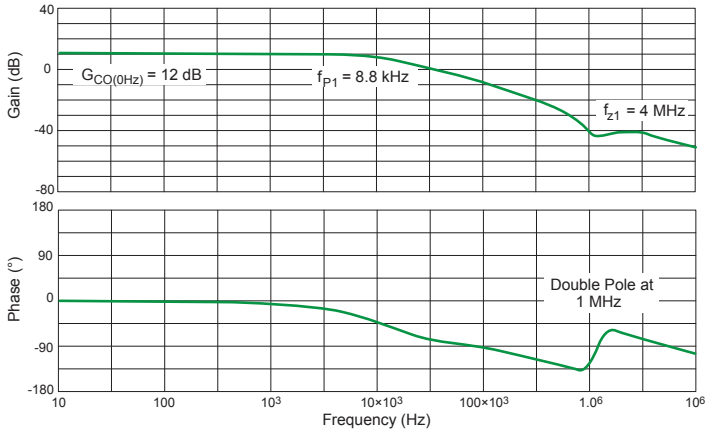

Figure 11: Control-to-Output Bode Plot

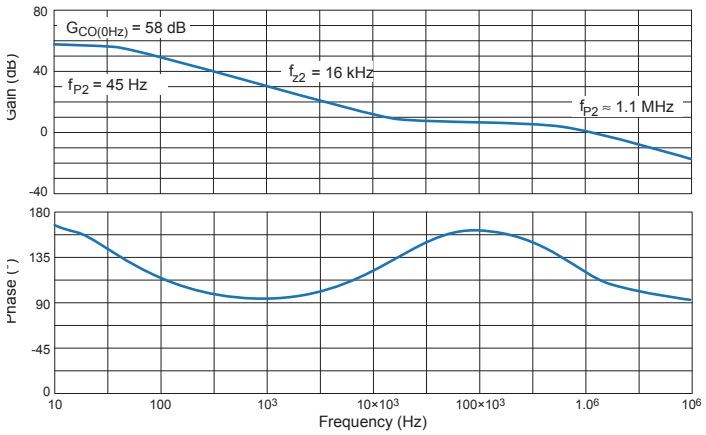

Figure 12: Type-II Compensated Error Amplifier Bode Plot

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amplifier response (blue curve) and the control to output response (green curve). As shown in Figure 13, the bandwidth of this system (f_c) is 72 kHz, the phase margin is 73 degrees, and the gain margin is 27 dB.

A Generalized Tuning Procedure

This section presents a methodology to systematically apply design considerations provided above.

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW}/20 < f_C < f_{SW}/7.5$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.
2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

$$R_Z = f_C \times \frac{V_{OUT1}}{V_{FB1}} \times \frac{2\pi \times C_{OUT1}}{g_{mPOWER} \times g_m} \qquad (27)$$

3. Determine the frequency of the pole (f_{P1}). This pole is formed by C_{OUT} and R_L. Use equation 21 (repeated here):

$$f_{P1} = \frac{1}{2\pi \times R_{L1} \times C_{OUT1}}$$

4. Calculate a range of values for the C_Z capacitor. Use the following:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}} \qquad (28)$$

To maximize system stability (that is, to have the greatest gain margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using equation 22 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times ESR_{COUT1} \times C_{OUT1}}$$

If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C), then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 26 to calculate the value of C_P by setting f_{P3} to either $5 \times f_C$ or $f_{SW}/2$, whichever is higher.

Alternatively, if f_{Z1} is near or below the target crossover frequency (f_C), then use equation 26 to calculate the value of C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

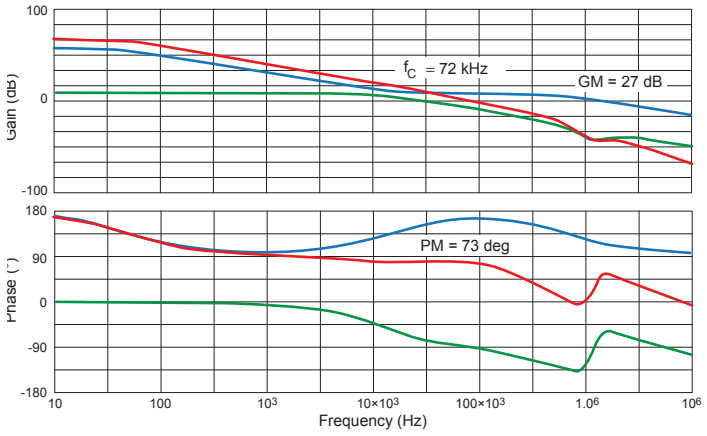

Figure 13: Bode Plot of the Complete System (red curve)

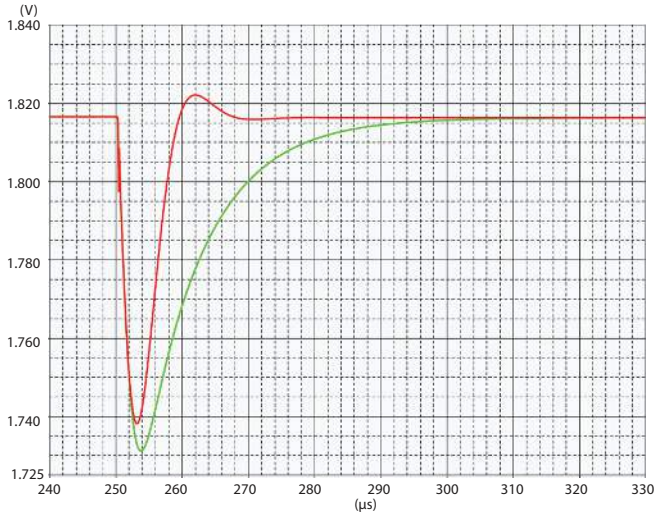

Figure 14: Transient Recovery Comparison for f_{Z2} at 16 kHz/69° and 50 kHz/51°

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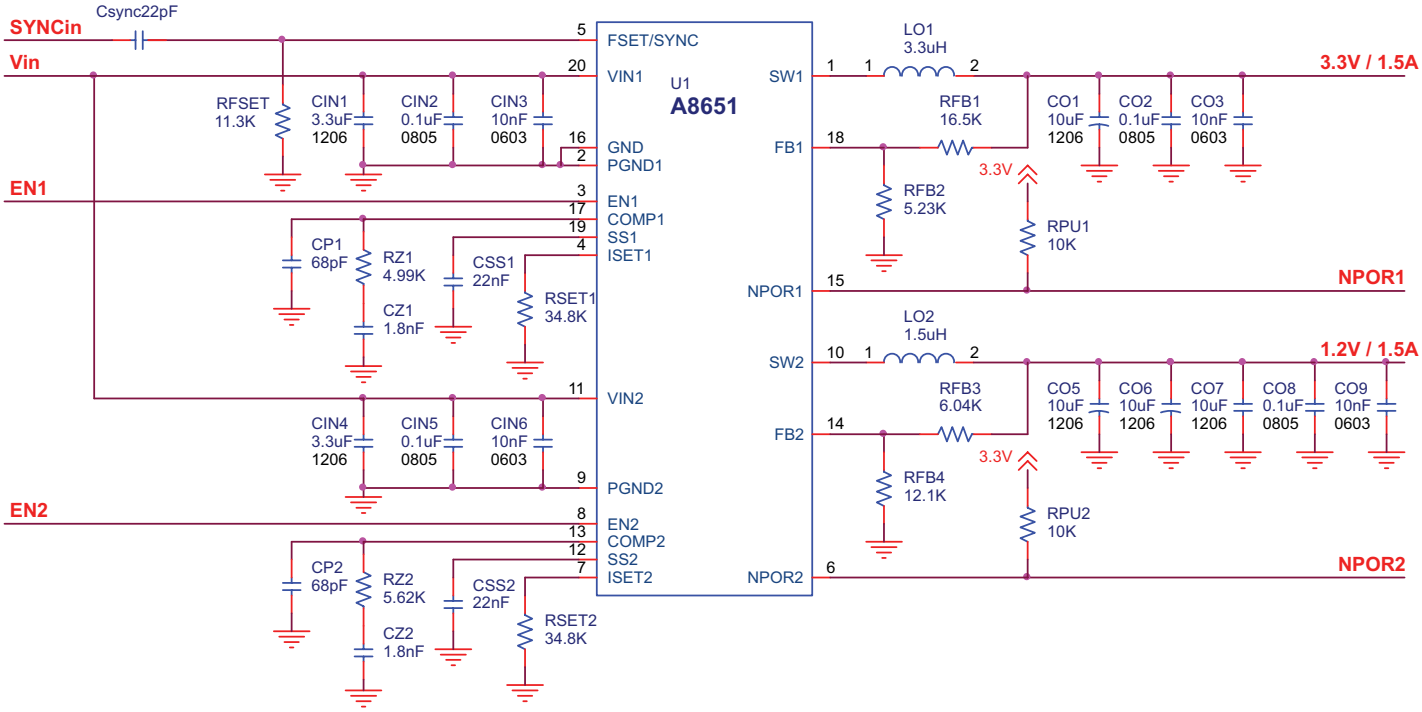

Figure 15: Typical Application Circuit for V_{IN} = 5 V at T_A = 125°C: V_{OUT} 3.3 V / 1.5 A and 1.2 V / 1.5 A at 2 MHz
C_{SYNC} are only required if synchronizing to an external clock

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POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A8651 is the sum of the power dissipated from the VIN supply current (P_{IN}) and the power dissipated by the two regulators. The regulator power dissipation is composed of: the power dissipated due to the switching of the high-side power MOSFET ($P_{SW(HS)}$), the power dissipated due to the rms current being conducted by the high-side and low-side MOSFETs ($P_{COND(HS)}$ and $P_{COND(LS)}$), and the power dissipated by the low-side body diode (P_{NO}) during the non-overlap time.

The power dissipated from the VIN supply current can be calculated using the following equation:

$$P_{IN} = V_{IN1} \times I_Q + (V_{IN1} + V_{IN2}) \times (Q_{G(HS)} + Q_{G(LS)}) \times f_{SW} \quad (29)$$

where

V_{INx} are the input voltages,

I_Q is the input quiescent current drawn by the device (nominally 2 mA),

$Q_{G(HS)}$ and $Q_{G(LS)}$ are the internal high- and low-side MOSFET gate charges (approximately 3.3 nC and 1.4 nC, respectively), and

f_{SW} is the PWM switching frequency.

Note: The calculation after this point refers only to regulator 1.

The power dissipated by the internal high-side MOSFET during PWM switching can be calculated using the following equation:

$$P_{SW1} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (30)$$

where

V_{IN} is the input voltage,

I_{OUT} is the output current,

f_{SW} is the PWM switching frequency, and

t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node depend on the external components and PCB layout so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 15 ns. The fall time is usually about 50% faster than the rise time.

The conduction losses dissipated by the high-side MOSFET while it is conducting can be calculated using the following equation:

$$P_{COND(HS)} = I^2_{rms(FET)} \times R_{DS(on)HS} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)HS} \quad (31)$$

where

I_{OUT} is the regulator output current,

ΔI_L is the peak-to-peak inductor ripple current, and

$R_{DS(on)1}$ is the on-resistance of the high-side MOSFET.

The conduction losses dissipated by the low-side MOSFET can be calculated as:

$$P_{COND2} = I^2_{rms(FET)} \times R_{DS(on)2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)2} \quad (32)$$

where

I_{OUT} is the regulator output current,

ΔI_L is the peak-to-peak inductor ripple current, and

$R_{DS(on)1}$ is the on-resistance of the high-side MOSFET.

The $R_{DS(on)}$ of the MOSFETs has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated by the low-side MOSFETs body diode during the non-overlap time can be calculated as:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW} \quad (33)$$

where

The deadtime is the same for the rising and falling edges of SW, V_{SD} is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and t_{NO} is the non-overlap time (typically 15 ns),

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Finally, the total power dissipated by the device (P_{TOTAL}) is the sum of the previous equations:

$$P_{TOTAL} = P_{IN} + P_{REGULATOR1} + P_{REGULATOR2} \quad (35)$$

where

$$P_{REGULATOR1} = P_{SW} + P_{COND(HS)} + P_{COND(LS)} + P_{NO} \quad (36)$$

The average junction temperature can be calculated with the following equation:

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A \quad (37)$$

where

P_{TOTAL} is the total power dissipated as described in equation 35,

$R_{\theta JA}$ is the junction-to-ambient thermal resistance (48°C/W on a 4-layer PCB), and

T_A is the ambient temperature.

The maximum junction temperature is dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs among: ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

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PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical if the A8651 is to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 16 shows a typical buck converter schematic with the critical power paths/loops. Figure 17 shows an example PCB component placement and routing with the same critical power paths/loops from the schematic.

1. Place the ceramic input capacitors as close as possible to the VINx pins and ground the capacitors at the PGNDx pins. The ceramic input capacitors and the A8651 must be on the same layer. Connect the input capacitors, the VINx pins, and the PGNDx pins with a wide trace. This critical loop is shown as a red trace in Figures 16 and 17.
2. Place the output inductor (L_{Ox}) as close as possible to the SWx pins. The output inductor and the A8651 must be on the same layer. Connect the SWx pins to the output inductor with a relatively wide trace or polygon. For EMI/EMC reasons, it is best to minimize the area of this trace/polygon. This critical trace is shown as a green trace in Figure 16. Also, keep low-level analog signals (like FB and COMP) away from the SW metal.
3. Place the output capacitors relatively close to the output inductor and the A8651. Ideally, the output capacitors, output inductor and the A8651 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low inductance connection back to the PGND pin. These critical connections are shown in blue in Figures 16 and 17.
4. Place the feedback resistor dividers (R_{FB1}-R_{FB2}) very close to the FB pin. Orient R_{FB2} such that its ground is as close as possible to the A8651.
5. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. Orient CZ and CP such that their ground connections are as close as possible to the A8651.
6. Place and ground the FSET resistor as close as possible to the FSET pin.
7. The output voltage sense trace (from V_{OUT} to R_{FB1}) should be connected as close as possible to the load to obtain the best load regulation.
8. The thermal pad under the IC should be connected a ground plane (preferably on the bottom layer) with as many vias as possible. Allegro recommends vias with approximately a 10-15 mil hole and a 5-7 mil ring.
9. Place the soft-start capacitor (CSS) as close as possible to the SS pin. Place a via to the GND plane as close as possible to this component.
10. When connecting the input and output ceramic capacitors to a power or ground plane, use multiple vias and place the vias as close as possible to the component's pads. Do not use thermal reliefs (spokes) around the pads for the input and output ceramic capacitors.
11. EMI/EMC issues are always a concern. Allegro recommends having locations for an RC snubber from SW to ground. The snubber components can be placed on the back of the PCB and populated only if necessary. The resister should be 0805 or 1206 size.
12. Allegro strongly recommends the use of current steering (a cut in the ground plane) to prevent current from SW1 from disturbing SW2 and vice versa. Notice the horizontal cut in the ground plane as shown in Figure 17.

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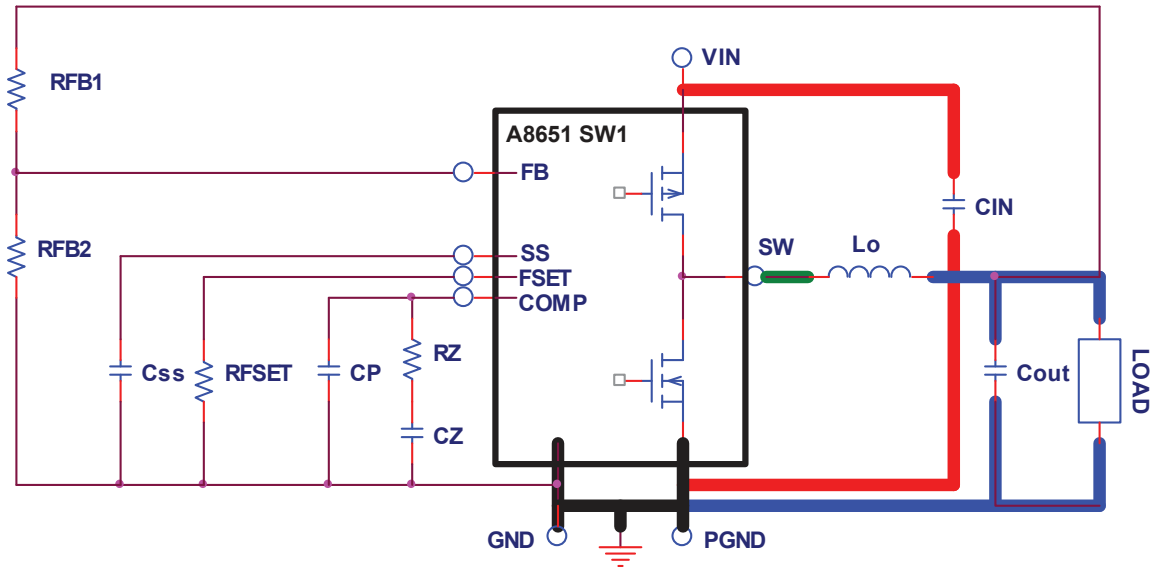

Figure 16: Typical Synchronous Buck Converter with Critical Paths/Loops Shown

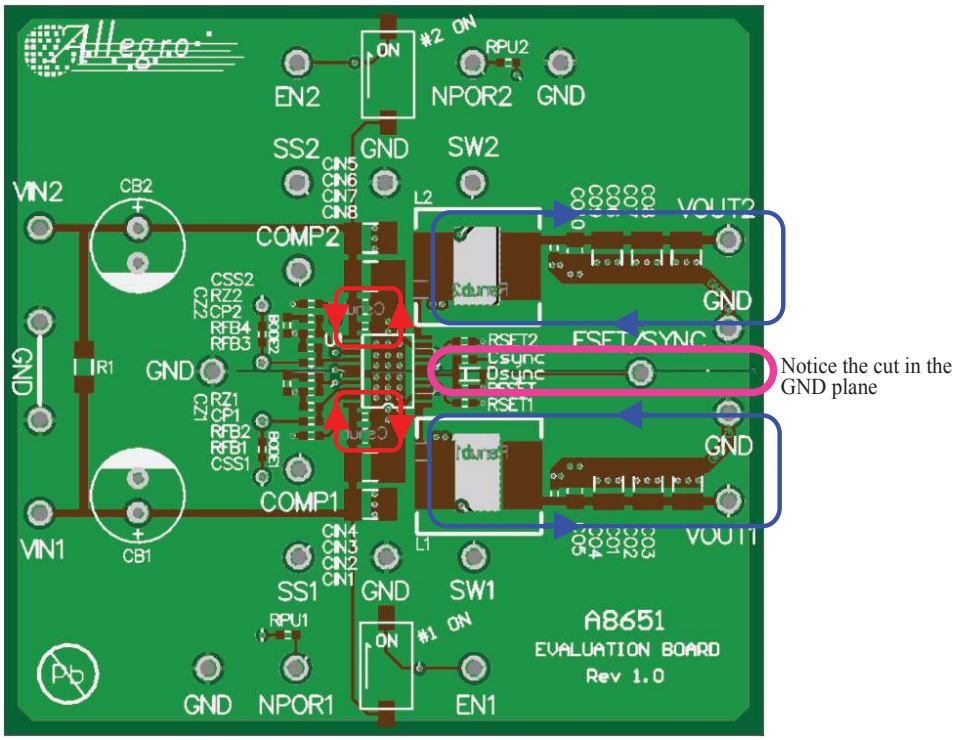

Figure 17: Example PCB Component Placement and Routing

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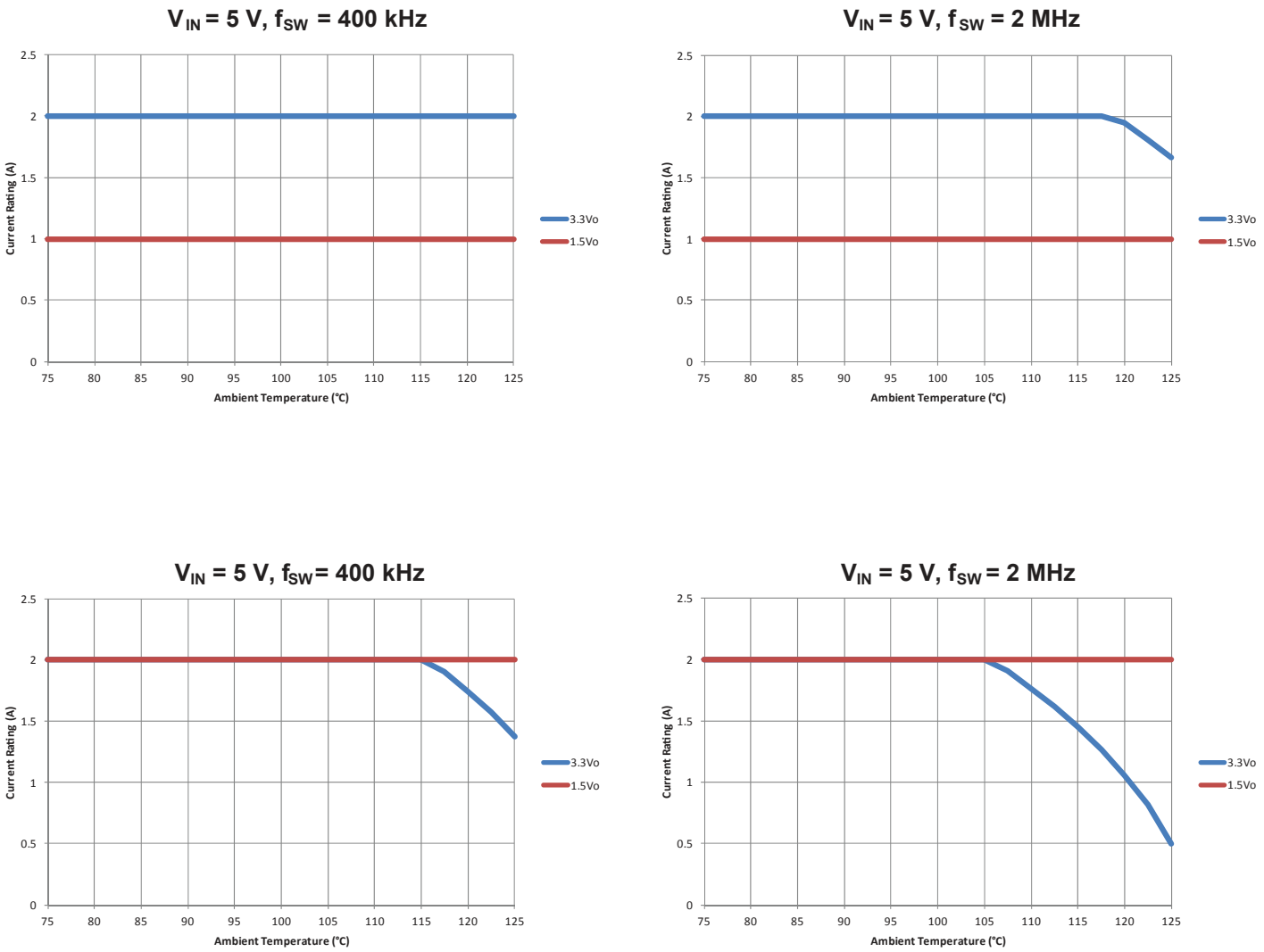

Figure 16: Current Derating Curve versus Output Voltages, Switching Frequency, and Ambient Temperature

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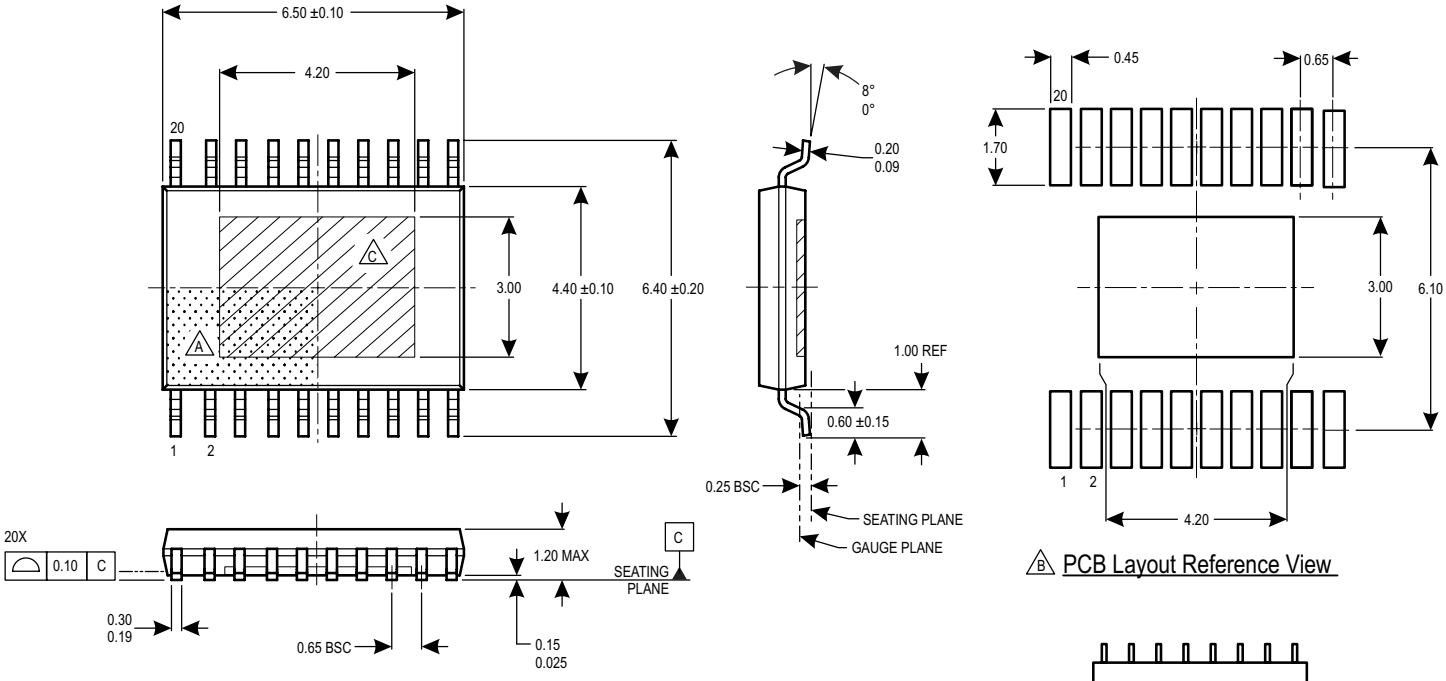
PACKAGE OUTLINE DIAGRAM

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 17: Package LP, 20-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
1	July 2, 2014	Removed references to D_{SYNC}
2	September 25, 2014	Revised equation 2
3	September 29, 2014	Revised Switching Frequency values
4	February 20, 2015	Revised equation 4b
5	April 17, 2015	Added -1 option
6	June 10, 2015	Revised soft-start fault/hiccup reset voltage values
7	January 28, 2016	Updated functional block diagrams, last paragraph of Soft-Start (startup) and Inrush Current Control section, and Table 2: Summary of A8651 Fault Modes and Operation.
8	December 5, 2016	Updated status of A8651KLPTR-T part variant to Discontinued
9	April 22, 2020	Minor editorial updates
10	April 19, 2022	Updated package drawing (page 33)

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