L6585DE

Combo IC for PFC and ballast control

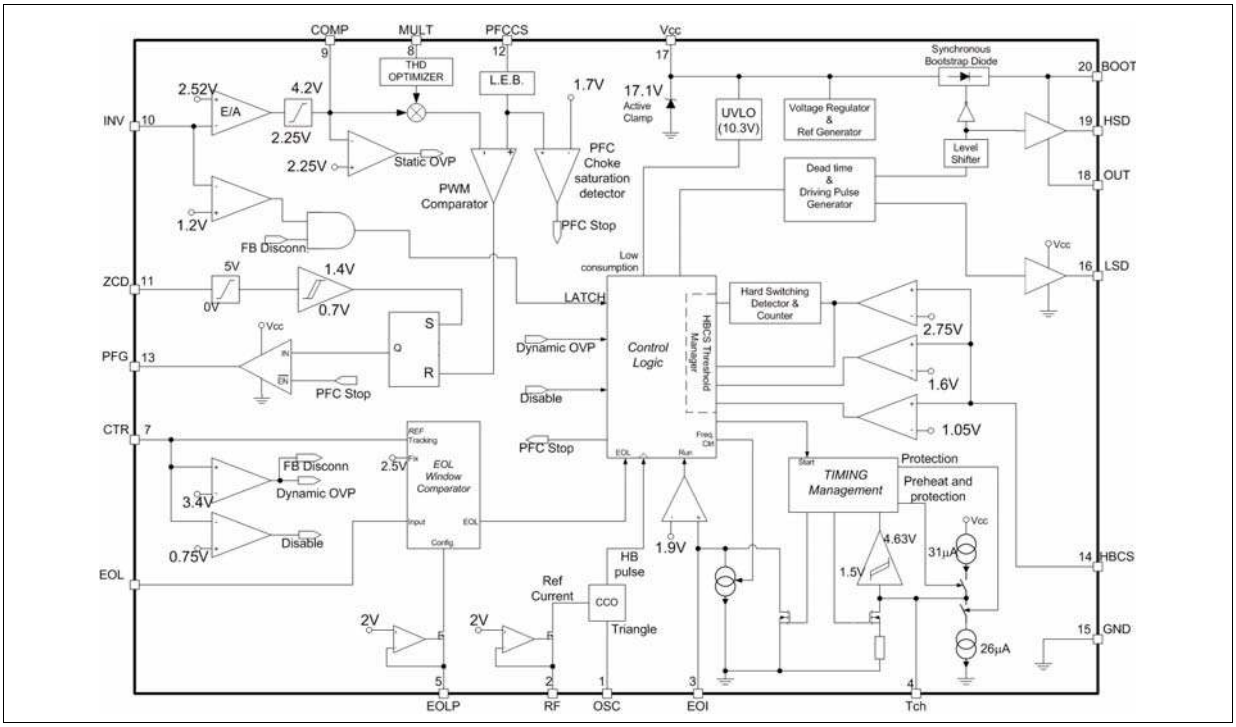
Features

- PFC section
  - transition mode PFC with over-current protection
  - over-voltage protection
  - feedback disconnection
  - under-voltage lockout
  - PFC choke saturation detection
  - THD optimizer
- Half-bridge section
  - preheating and ignition phases independently programmable
  - 3 % oscillator precision
  - 1.2 µs dead time

SO-20

  - programmable and precise end-of-life protection compliant with all ballast configurations
  - smart hard switching detection
  - fast ignition voltage control with choke saturation detection
  - half-bridge over-current control

Figure 1. Block diagram



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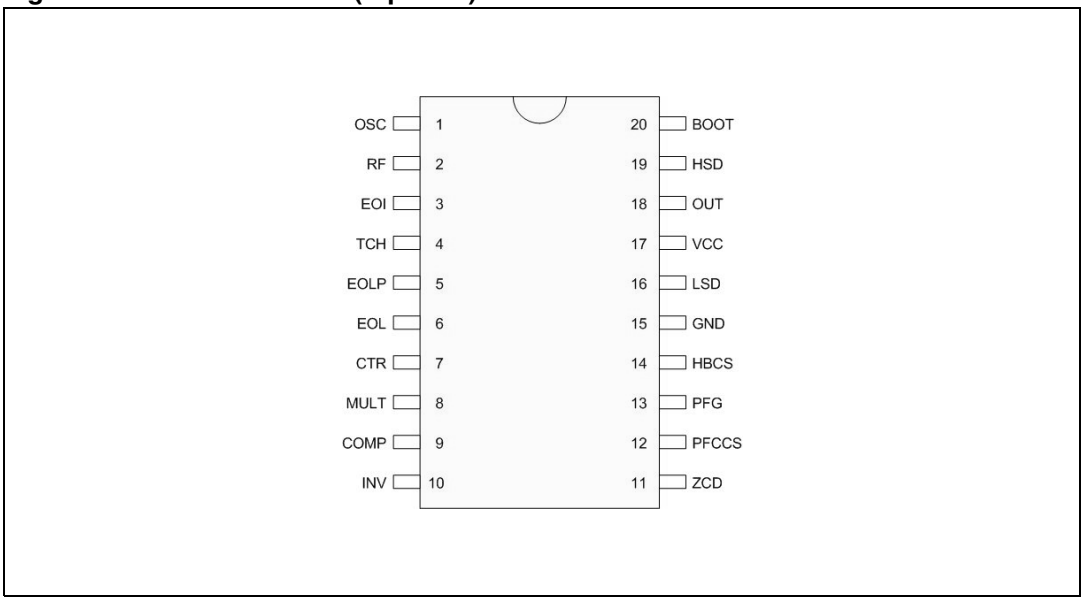
1 Pin settings

1.1 Connection

Figure 2. Pin connection (top view)



1.2 Functions

Table 1. Pin functions

Pin n.	Name	Function
1	OSC	An external capacitor to ground fixes the half-bridge switching frequency with a ± 3 % precision.
2	RF	Voltage reference capable of sourcing up to 240 µA. The current sunk from this pin fixes the switching frequency of the half-bridge for each operating state. A resistor (R_{RUN}) connected to ground sets the half-bridge operating frequency combined with the capacitor connected to the pin OSC. A resistor connected to EOI (R_{PRE}) sets the maximum half-bridge switching frequency during preheating combined with R_{RUN} and C_{OSC}.
3	EOI	Connected to ground by a capacitor that, combined with R_{PRE}, determines the ignition time. *Preheating*: low impedance to set high switching frequency *Ignition and run mode*: high impedance with controlled current sink in case of HBCS threshold triggering.

Table 1. Pin functions (continued)

Pin n.	Name	Function
4	Tch	Pin for setting the preheating time and protection intervention. Connect an RC parallel network (R_d and C_d) to ground. *Preheating:* the C_d is charged by an internal current generator. When the pin voltage reaches 4.63 V the generator is disabled and the capacitor discharges because of R_d. Once the voltage drops below 1.5 V, the preheating finishes, the ignition phase starts and the R_dC_d is pulled to ground. *Ignition and Run mode:* During proper behavior of the IC, this pin is low impedance. During a fault (either over-current or EOL) the internal generator charges the C_d to 4.63 V and then another current generator discharges the same capacitor. In this way, C_d sets the fault timing (shorter than preheating time).
5	EOLP	Pin to program the EOL comparator. It is possible to select both the EOL sensing method (fixed reference or reference in tracking with CTR) and the window comparator amplitude by connecting a resistor (R_{EOLP}) to ground.
6	EOL	Input for the window comparator. It can be used to detect lamp ageing for either “lamp to ground” or “block capacitor to ground” configurations. This function is blanked during the ignition phase.
7	CTR	Input pin for: - PFC over-voltage detection: the PFC driver is stopped until the voltage returns in the proper operating range - Feedback disconnection detection - Reference for EOL comparator (in case tracking reference) - The pin can be used also for shutdown
8	MULT	Multiplier external input. This pin is connected to the rectified mains voltage via a voltage divider and provides the sinusoidal reference to the PFC current loop.
9	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the PFC voltage control loop and ensure high power factor and low THD.
10	INV	Inverting input of the error amplifier. Output voltage of the PFC pre-regulator is fed to the pin through a voltage divider.
11	ZCD	Boost inductor demagnetization sensing input for PFC transition-mode operation. A negative-going edge triggers PFC MOSFET turn-on. During startup or when the voltage is not high enough to arm the internal comparator, the PFC driver is triggered by means of an internal starter.
12	PFCCS	Input to the PFC PWM comparator. The current flowing through the PFC MOSFET is sensed through a resistor. The resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine the PFC MOSFET’ s turnoff. A second comparison level detects abnormal currents (due to boost inductor saturation, for example) and, on this occurrence, shuts down the PFC gate. An internal LEB prevents undesired function triggering.

Table 1. Pin functions (continued)

Pin n.	Name	Function
13	PFG	PFC gate driver output. The totem pole output stage is able to drive power MOSFETs with a peak current of 300 mA source and 600 mA sink (typ. values).
14	HBCS	3-level half-bridge current monitor for current control. The current flowing through the HB MOSFET is sensed through a resistor. The resulting voltage is applied to this pin. *First level threshold* (1.05 V, active during run mode): in case of threshold crossing the IC reacts with frequency increase in order to limit the half-bridge (and lamp) current. *Second level threshold* (1.6 V, active during ignition and run mode): - Ignition: in case of threshold crossing during the frequency shift, the IC reacts with frequency increase in order to limit the lamp voltage and preventing operation below resonance. - Run mode: in case of threshold crossing because of current spikes (due, for example, to capacitive mode / cross-conduction) longer than 200 ns the L6585DE is latched in low consumption mode to avoid damage to the MOSFETs. *Third level threshold* (2.75 V, active during ignition and run mode): - Ignition: in case of threshold crossing during frequency shift (e.g. caused by choke saturation), the IC latches to avoid damage to the MOSFETs. - Run mode: in case of threshold crossing by a hard switching event (spike duration equal to around 40 ns) an internal counter is increased. After around 350 (typ.) subsequent hard switching events the IC is latched in low consumption mode.
15	GND	Ground.
16	LSD	Low side driver output: the output stage can deliver 290 mA source and 480 mA sink (typ. values).
17	VCC	Supply voltage of both the signal part of the IC and the gate driver. Clamped with a Zener inside.
18	OUT	High-side driver floating reference. This pin must be connected close to the source of the high side power MOSFET.
19	HSD	High-side driver output: the output stage can deliver 290 mA source and 480 mA sink (typ. values).
20	BOOT	Bootstrapped supply voltage. Bootstrap capacitor must be connected between this pin and OUT pin. Patented, integrated circuitry replaces the external bootstrap diode by means of a high voltage DMOS, synchronously driven with the low side power MOSFET.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{BOOT}	20	Floating supply voltage	-1 to 618	V
V_{OUT}	18	Floating ground voltage	-3 to V_{BOOT} – 18	V
dV_{OUT}/dt	18	Floating ground max. slew rate	50	V/ns
V_{CC}	17	IC supply voltage (I_{CC} = 20 mA)(1)	Self-limited	V
	1, 3, 4, 8, 10, 12	Analog input and outputs	-0.3 to 5	V
	2, 5		-0.3 to 2.7	V
V_{EOL}	6	Maximum EOL voltage	-0.3 to V_{CC}	V
V_{CTR}	7	Maximum CTR voltage	-0.3 to 7	V
V_{HBCS}	14	Maximum half-bridge current sense voltage	-5 to 5	V
	9, 11		Self-limited	
I_{RF}	2	Current capability	240	µA
I_{EOLP}	5	Current capability	100	µA
$F_{OSC(MAX)}$		Maximum operating frequency	250	kHz
P_{TOT}		Power dissipation @T_A = 70 °C	0.83	W

1. The device has an internal clamping Zener between GND and the VCC pin. It must not be supplied by a low impedance voltage source.

Note: ESD immunity for pins 18, 19 and 20 is guaranteed up to 900 V (human body model)

2.2 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
R_{thJA}	Max. thermal resistance junction to ambient	120	°C/W
T_J	Junction operating temperature range	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

3 Electrical characteristics

V_{CC} = 15 V, T_A = 25 °C, C_L = 1 nF, C_{OSC} = 470 pF, R_{RUN} = 47 kΩ, unless otherwise specified

Table 4. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
Vcc	V_{CC}	Operating range	After turn-on	11		16	V
$V_{CC(on)}$	V_{CC}	Turn-on threshold	(1)	13.6	14.3	15	V
$V_{CC(OFF)}$	V_{CC}	Turn-off threshold	(1)	9.6	10.3	11	V
V_Z	V_{CC}	Zener voltage	Icc = 20 mA, T_A = 25 °C	16.7	17.1	17.5	V
			Icc = 20 mA, full temperature range	16	17.1	18	V
Supply current							
I_{ST-UP}	V_{CC}	Start-up current	Before turn-on @ 13 V		250	370	µA
I_{CC}	V_{CC}	Operating supply current	Fpfc = 50 kHz		7		mA
Iq	V_{CC}	Residual current	IC latched			350	µA
PFC section – multiplier input							
I_{MULT}	MULT	Input bias current	V_{MULT} = 0 V			-1	µA
V_{MULT}	MULT	Linear operation range	V_{COMP} = 3 V	0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	MULT	Output max. slope	V_{MULT} = 0 to 1 V, V_{COMP} = Upper clamp		0.75		V/V
K_M	MULT	Gain	V_{MULT} = 1 V, V_{COMP}= 3 V		0.52		1/V
PFC section – error amplifier							
V_{INV}	INV	Voltage feedback input threshold		2.47	2.52	2.57	V
	INV	Line regulation	V_{CC} = 10.3 V to 16 V			50	mV
I_{INV}	INV	Input bias current				-1	µA
Gv	INV	Voltage gain	Open loop (2)	60	80		dB
GB	INV	Gain-bandwidth product	(2)		1		MHz
I_{COMP}	COMP	Source current	V_{COMP} = 4V, V_{INV} = 2.4 V		-2.6		mA
		Sink current	V_{COMP} = 4V, V_{INV} = 2.6 V		4		mA
V_{COMP}	COMP	Upper clamp voltage	I_{SOURCE} = 0.5 mA		4.2		V
		Lower clamp voltage	I_{SINK} = 0.5 mA		2.25		V
V_{DIS}	INV	Open loop detection threshold	CTR > 3.4 V		1.2		V
	COMP	Static OVP threshold		2.1	2.25	2.4	V

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
CTR pin							
DIS	CTR	Shutdown threshold	Falling edge		0.75		V
		Hysteresis			120		mV
PFOV	CTR	Dynamic PFC over-voltage	Rising edge		3.4		V
		Hysteresis			140		mV
	CTR	Available range as tracking reference	Lower threshold (falling)		1.7		V
			Hysteresis		120		mV
			Higher threshold (rising)		3.4		V
			Hysteresis		140		mV
PFC section – current sense comparator							
I_{CS}	PFCS	Input bias current	V_{CS} = 0 V			-1	µA
t_{LEB}	PFCS	Leading edge blanking	(2)	100	200	300	ns
V_{CSstop}	PFCS	PFC stop threshold	V_{CTR}	1.65	1.75	1.85	V
$t_{d(H-L)}$	PFCS	Delay to output			120		ns
$V_{CSclamp}$	PFCS	Current sense reference clamp	V_{COMP} = Upper clamp	1	1.08	1.16	V
PFC section – zero current detector							
V_{ZCDH}	ZCD	Upper clamp voltage	I_{ZCD} = 2.5 mA	5			V
V_{ZCDL}	ZCD	Lower clamp voltage	I_{ZCD} = -2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	ZCD	Arming voltage (positive-going edge)	(2)		1.4		V
V_{ZCDT}	ZCD	Triggering voltage (negative-going edge)	(2)		0.7		V
I_{ZCDb}	ZCD	Input bias current	V_{ZCD} = 1 to 4.5 V			1	µA
I_{ZCDsrc}	ZCD	Source current capability		-4			mA
I_{ZCDsnk}	ZCD	Sink current capability		4			mA
PFC section – gate driver							
	PFG	Output high/low	I_{SINK} = 10 mA			0.2	V
			I_{SOURCE} = 10 mA	14.5			V
tf	PFG	Fall time			40	90	ns
tr	PFG	Rise time			90	140	ns
I_{SINK}	PFG	Peak sink current		475	600		mA
I_{SOURCE}	PFG	Peak source current		200	300		mA
	PFG	Pull-down resistor			10		kΩ

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Half bridge section – timing and oscillator							
I_{CH}	T_{CH}	Charge current	V_{TCH} = 2.2 V		31		µA
V_{CHP}	T_{CH}	Charge threshold (positive going-edge)	(1)	4.53	4.63	4.73	V
V_{CHN}	T_{CH}	Discharge threshold (negative going edge)	(1)		1.50		V
	T_{CH}	Leakage current	1.5 V < V_{TCH} < 4.5 V, falling			0.1	µA
I_{CHsnk}	T_{CH}	Discharge current	During protection: reduced timing V_{TCH} = 3 V		26		µA
R_{TCH}	T_{CH}	Internal impedance	Run mode		100	200	Ω
	EOI	Open state current	V_{EOI} = 2 V			0.15	µA
R_{EOI}	EOI	EOI impedance	During preheating			150	Ω
I_{EOI}	EOI	EOI current generator during ignition and run mode	Tspike = 200 ns (3)		20		µA
			Tspike = 400 ns (3)		100		
			Tspike = 600 ns (3)		200		
			Tspike = 1 µs (3)		270		
V_{EOI}	EOI	EOI threshold	(1)	1.83	1.9	1.98	V
V_{REF}	RF	Reference voltage	(1)	1.92	2	2.08	V
I_{RF}	RF	Max current capability		240			µA
$I_{OSCratio}$	OSC	I_{OSC}/I_{RF}	V_{OSC} = 3 V		4		
	OSC	Rising threshold	(1)		3.7		V
	OSC	Falling threshold	(1)		0.9		V
D	OSC	Output duty cycle		48	50	52	%
T_{DEAD}	OSC	Dead time		0.96	1.2	1.44	µs
F_{RUN}	OSC	Half-bridge oscillation frequency (run mode)		58.4	60.2	62	KHz
F_{PRE}	OSC	Half-bridge oscillation frequency (preheating)	R_{PRE} = 50 kΩ	113.2	116.7	120.2	KHz
Half bridge section – end-of-life function							
I_{EOLP}	EOLP	Current capability		100			µA
V_{EOLP}	EOLP	Reference voltage		1.92	2	2.08	V
	EOL	Operating range	EOLP = 27 kΩ	0.95		4.15	V
V_S	EOL	Window comparator reference	220 kΩ < R_{EOLP} < 270 kΩ or 22 kΩ < R_{EOLP} < 27 kΩ	tracking with CTR			V
			R_{EOLP} > 620KΩ or 75 kΩ < R_{EOLP} < 91 kΩ		2.5		

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_W	EOL	Half window amplitude	220 kΩ < R_{EOLP} < 270 kΩ		+250		mV
					-240		
			22 kΩ < R_{EOLP} < 27 kΩ		+160		
					-150		
			R_{EOLP} > 620 kΩ		720		
			75 kΩ < R_{EOLP} < 91 kΩ		240		
	EOL	Sink/source capability			5.5		µA
Half bridge section – Half-bridge current sense							
$HBCS_H$	HBCS	Frequency increase	V_{EOI} < 1.9 V (*ignition*)	1.53	1.6	1.66	V
$HBCS_L$	HBCS	Threshold	V_{EOI} > 1.9 V (*run mode*)	0.98	1.05	1.12	V
$HBCS_{H,test}$	HBCS	Shut down threshold during first low side on time after Tch cycle	V_{EOI} < 1.9 V (*ignition*)		1.05		V
$HBCS_{L,test}$	HBCS		V_{EOI} > 1.9 V (*run mode*)		0.82		V
$HBCS_{AS}$	HBCS	Anti saturation threshold	Ignition		2.75		V
$t_{LEB,HBCS}$	HBCS	Leading edge blanking	Ignition		270		ns
$HBCS_{CM}$	HBCS	Capacitive mode threshold	*Run mode, Tpulse > 200 ns*	1.53	1.6	1.66	V
$HBCS_{HS}$	HBCS	Hard switching detector	*Run mode, Tpulse > 40 ns*		2.75		V
		Hysteresis			450		mV
N_{HS}		Hard switching events before shutdown	Run mode		350		
Half bridge section – Low side gate driver							
	LSD	Output low voltage	I_{SINK} = 10 mA			0.3	V
	LSD	Output high voltage	I_{SOURCE} = 10 mA	14.5			V
	LSD	Peak source current		200	290		mA
	LSD	Peak sink current		400	480		mA
T_{RISE}	LSD	Rise time			120		ns
T_{FALL}	LSD	Fall time			80		ns
	LSD	Pull-down resistor			45		kΩ
Half bridge section – High side gate driver (voltages referred to OUT)							
	HSD	Output low voltage	I_{SINK} = 10 mA			V_{OUT} + 0.3	V
	HSD	Output high voltage	I_{SOURCE} = 10 mA	V_{BOOT} _ 0.5			V
	HSD	Peak source current		200	290		mA
	HSD	Peak sink current		400	480		mA

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{RISE}	HSD	Rise time			120		ns
T_{FALL}	HSD	Fall time			80		ns
	HSD	HSD-OUT pull-down			50		kΩ
High-side floating gate-drive supply							
	BOOT	Leakage current	V_{BOOT} = 600 V (2)			5	µA
	OUT	Leakage current	V_{OUT} = 600 V (2)			5	µA
		Synchronous bootstrap diode on-resistance	V_{LSD} = HIGH		250		Ω

1. Parameter in tracking
2. Specification over the -40 °C to 125 °C junction temperature range are ensured by design, characterization and statistical correlation
3. A pulse train has been sent to the HBCS pin with f = 6 kHz; the pulse duration is the one indicated in the notes as "TON"

4 Device description

The L6585DE embeds a high performance PFC controller, a ballast controller and all the relevant drivers necessary to build an electronic ballast.

The PFC section achieves current mode control operating in transition mode, offering a highly linear multiplier including a THD optimizer that allows for an extremely low THD, even over a large range of input voltages and loading conditions.

The PFC output voltage is controlled by means of a voltage-mode error amplifier and a precise internal voltage reference.

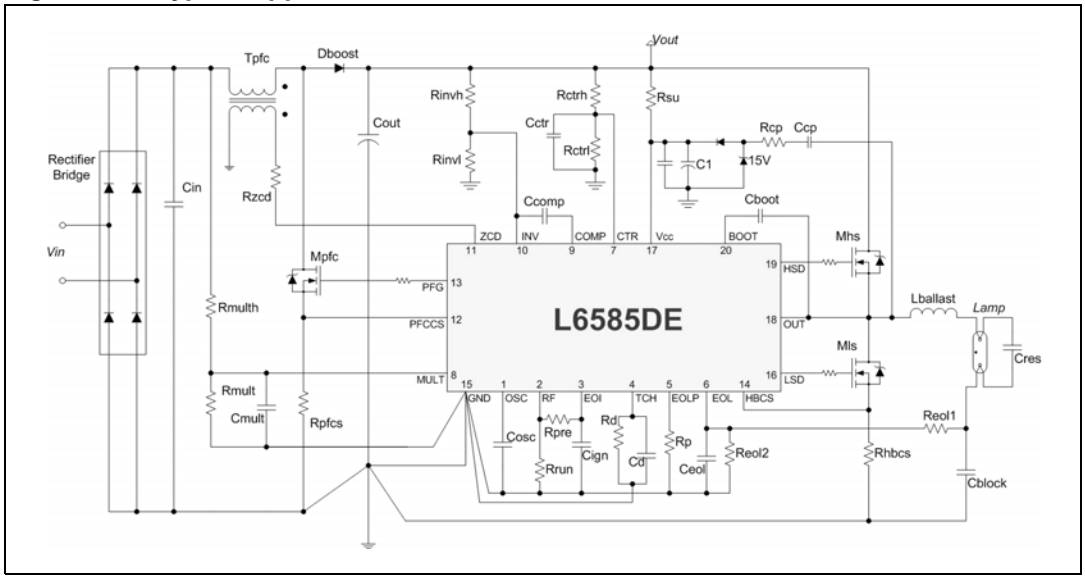
The ballast controller offers the designer a very precise oscillator, a logic that manages all the operating steps and a full set of protection features:

- Programmable end-of-life detection, compliant with both lamp-to-ground and capacitor-to-ground configurations
- Over-current protection with either current limiting or choke saturation protection
- Hard switching events detection

High current capability drivers for both the PFC (300 mA source and 600 mA sink) and the half-bridge (290 mA source and 480 mA sink) also allow ballast designs for very high output power (up to 160 W).

5 Application information

Figure 3. Typical application



5.1 VCC section

The L6585DE is supplied by applying voltage between the V_{CC} pin and GND pin. An under-voltage lockout (UVLO) prevents the IC from operating with supply voltages too low to guarantee the correct behavior of the internal structures.

An internal voltage clamp limits the voltage to around 17 V and can deliver up to 20 mA. For this reason it cannot be used directly as a clamp for the charge pump (current peaks usually reach several hundreds of mA), but can be easily used during startup in order to charge the V_{CC} capacitor or during save mode in order to keep the IC alive, for example, connecting V_{CC} to input voltage through a resistor.

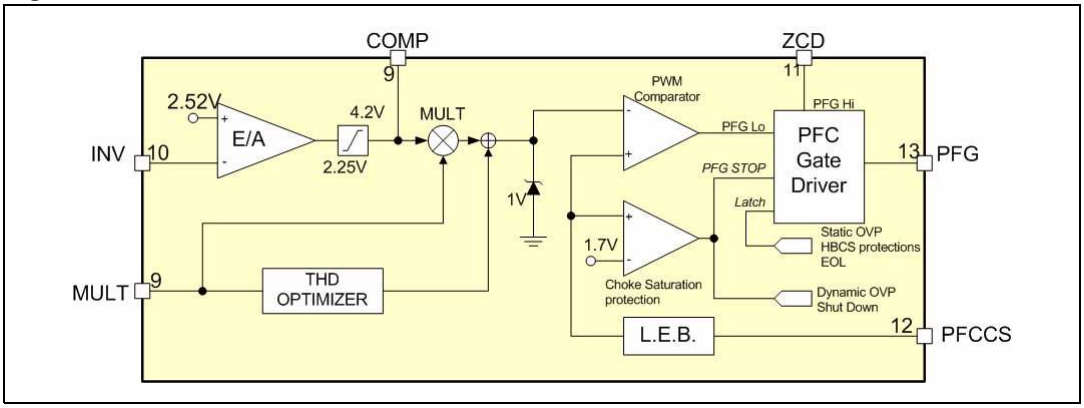
In addition to the bulk capacitor (>1 µF)it is suggested to place a 100 nF ceramic capacitor close to V_{CC} pin.

5.2 PFC section

5.2.1 TM PFC operation

The PFC stage contains all the features needed to implement a transition mode PFC controller.

Figure 4. PFC section



The control loop can be implemented thanks to the high performance error amplifier and the very precise internal voltage reference that fixes the non-inverting input of the E/A to 2.52 V ± 2 %.

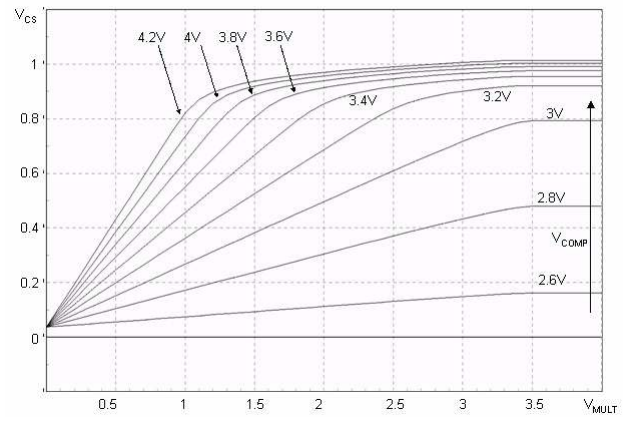
The control loop reacts in order to bring the inverting input to the same voltage. Connecting the high voltage rail to INV pin, by means of a voltage divider, the output voltage will be easily set.

The output of the E/A can be used in order to compensate the control loop with an RC network or, more often, with a simple capacitor connected between INV and COMP pin.

The output voltage of the E/A is also fed to the multiplier. This block multiplies the waveform present at the MULT pin by the output of the E/A. The resulting voltage will be used as the threshold for the current sense input. An internal clamp limits the threshold to a maximum value equal to 1 V.

In *Figure 5* the characteristic curves of the multiplier are reported.

Figure 5. Multiplier



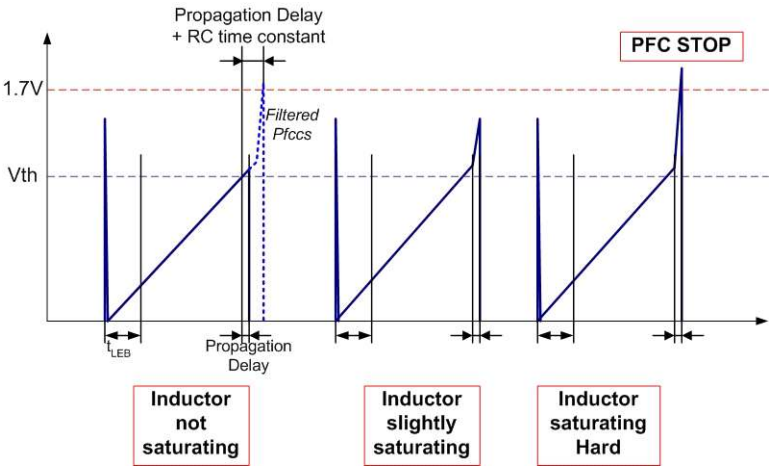
The ZCD input can be connected directly to an auxiliary winding of the PFC choke in order to turn on the MOSFET when the choke current reaches zero. This pin has internal clamps and high current capability that makes it compliant with a very wide range of input voltage. At startup, when PFC choke is not yet energized, an internal starter gives ZCD pulses to the PFC gate driver with a repetition rate of approximately 15 kHz.

By turning off the MOSFET when the current reaches the threshold and turning on the MOSFET when the choke current reaches zero, a triangular input current whose peaks are modulated by the MULT voltage is obtained. By feeding the MULT pin with the mains waveform, a power factor correction and THD reduction is achieved.

5.2.2 Leading edge blanking

Usually current sense voltage is filtered by means of an RC network in order to avoid false turning off of the MOSFET because of the discharge current related to parasitic drain capacitance present at the beginning of the on time of the MOSFET. This filtering generates a delay between the actual threshold crossing and the input triggering. During this time the PFC inductor current increases and the choke may saturate. A leading edge blanking structure makes the PFCCS input active only after 200 ns (typ.) after the PFG turn on. This allows the use of inductors with lower saturation current. However, if saturation occurs, a choke saturation protection turns off the PFC gate as soon as the voltage at pin PFCCS is above 1.7 V.

Figure 6. PFCCS waveforms



5.2.3 THD optimizer feature

When the input voltage passes through zero, the PFC choke cannot store energy because of the very low voltage across it. This may cause heavy crossover distortion and subsequent THD degradation. A small offset voltage superimposed over the MULT voltage can reduce this issue.

The internal THD optimizer increases the performance when the mains voltage reaches zero; this reduces crossover distortion and avoids offset introduction.

5.2.4 Over-voltage protection

Two different over-voltage protections can be detected: dynamic over-voltage, usually due to fast load transition and static over-voltage, due to an excessive input voltage.

- **Dynamic OVP**
  The CTR pin is connected to high voltage rail through a voltage divider. If the voltage at this pin is above 3.4 V, the PFC gate driver is stopped until the voltage returns below the threshold. This limits the risk of choke saturation and MOSFET's damage.
- **Static OVP**
  A steady over-voltage may cause abnormal behavior in both the PFC (e.g. because input voltage is higher than PFC output voltage) and the ballast (e.g. overheating, lamp over-current, capacitive mode operating point). A steady over-voltage causes a slow transition of the COMP pin towards the low saturation (around 2.25 V). This fact is considered by the L6585DE as a static over-voltage event and a Tch cycle is started. After this cycle, if the COMP pin is saturated low the IC is latched in low consumption mode.

5.2.5 Disabling the L6585DE

the CTR pin can be used to shut down the IC without mains disconnection. When CTR is pulled below 0.75 V, the IC is stopped and the internal logic is reset. When CTR is released, the IC starts with a new preheating sequence. This function is available only if the IC is not latched due to a fault protection intervention.

5.2.6 Feedback disconnection protection

Very fast output voltage surges may damage the upper resistors of the voltage divider feeding the INV pin, causing a feedback disconnection. In this case, the E/A saturates high and the PFC gate drive turns on the MOSFET for a long time (the current sense threshold assumes its maximum value equal to 1 V) and the choke may saturate, destroying the MOSFET.

The output voltage increases very fast and may reach very high value even if OVP is triggered.

Feedback disconnection protection is then activated if V_{INV} < 1.2 V and dynamic over-voltage protection is triggered.

5.2.7 PFC over-current protection

The PFC MOSFET over-current can occur in cases of PFC choke saturation or in cases of surge from the input, due to the breakdown of the MOSFET body diode. The latter case is observed together with an over-voltage of the PFC output.

In both cases, the PFC stage is stopped, whereas the HB stage continues switching. The protection is not latched: once the PFCCS falls below 1.7 V, the PFC driver restarts.

6 Ballast section

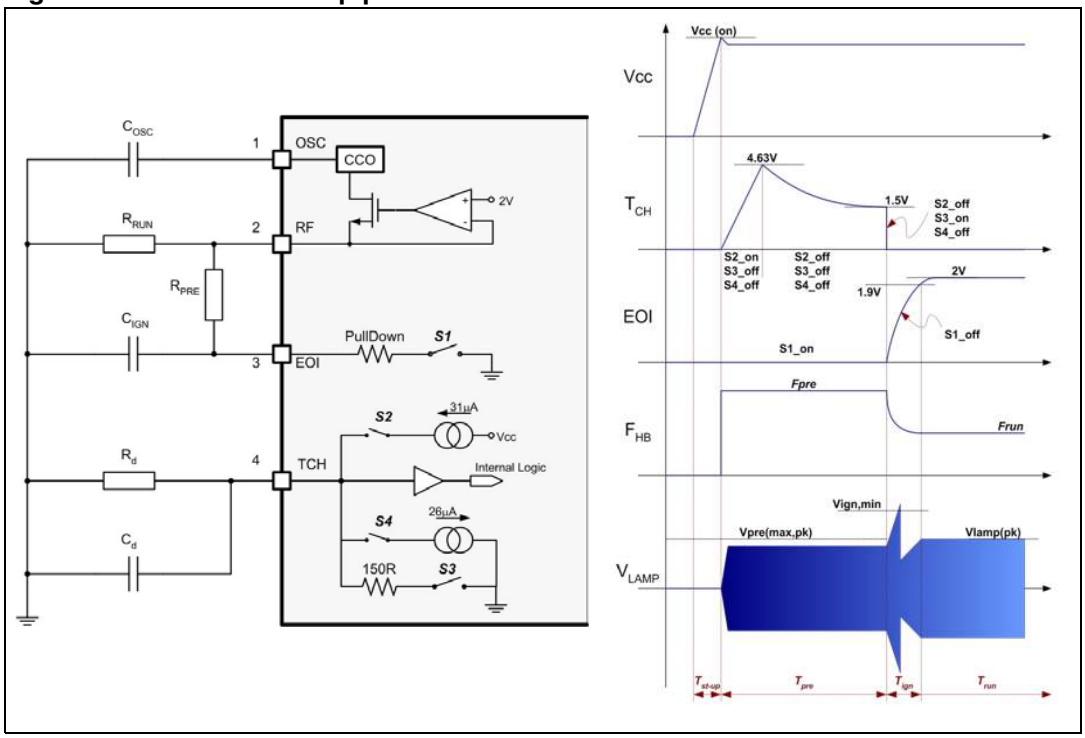
6.1 Half-bridge drivers and integrated bootstrap diode

The half-bridge drivers are capable of 290 mA source and 480 mA sink current. This makes them able to effectively drive also big MOSFETs Cg up to 2.2 nF. The high-side MOSFET is driven by means of a bootstrapped structure reducing the number of external components.

6.2 Normal start-up description

Referring to *Figure 7*, normal startup proceeds as follows:

Figure 7. Normal start-up procedure

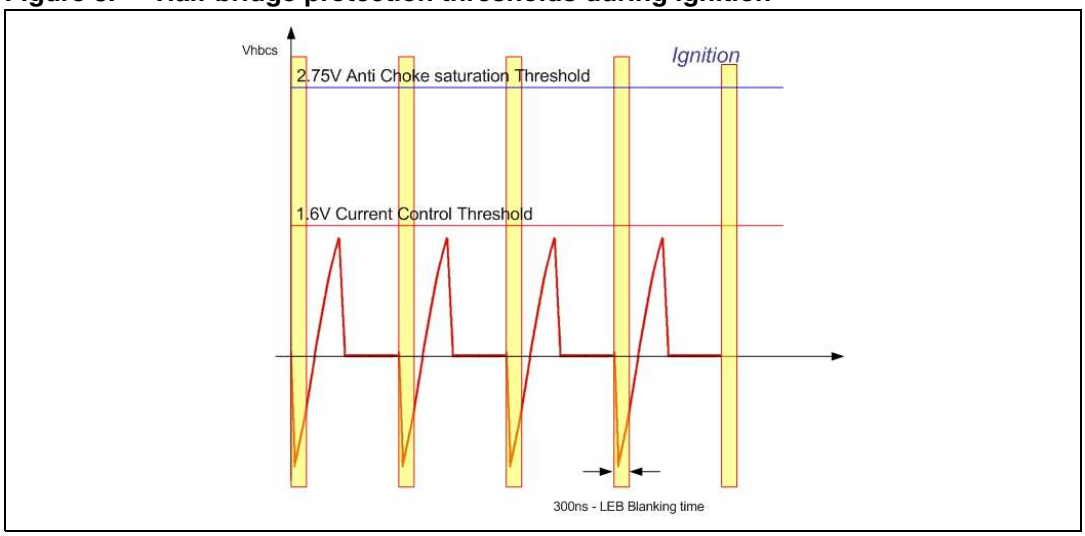


1. Startup*:* As soon as Vcc reaches the startup threshold voltage references are built up, the RF and EOLP pin are biased, the EOI pin is pulled down and the TCH pin starts sourcing 31 µA. The frequency of the half-bridge is generated by an internal CCO, connected to C_{OSC} and using the RF current as the control signal. With the EOI pin pulled down, the startup frequency will be due to the current flowing in parallel with R_{PRE} and R_{RUN} (see typical application diagram).
2. Preheating: the TCH pin continues to source 31 µA until its voltage reaches 4.63 V, therefore it is left in a high impedance status. As this pin loaded with an RC parallel network, the voltage across this pin decreases exponentially. When it reaches 1.5 V the TCH pin is pulled down and the preheating time ends. During this sequence the EOI pin is pulled down and the half-bridge frequency is the startup frequency. A leading

edge blanking is active during this time in order to avoid any detection of hard switching events, very common during this phase.

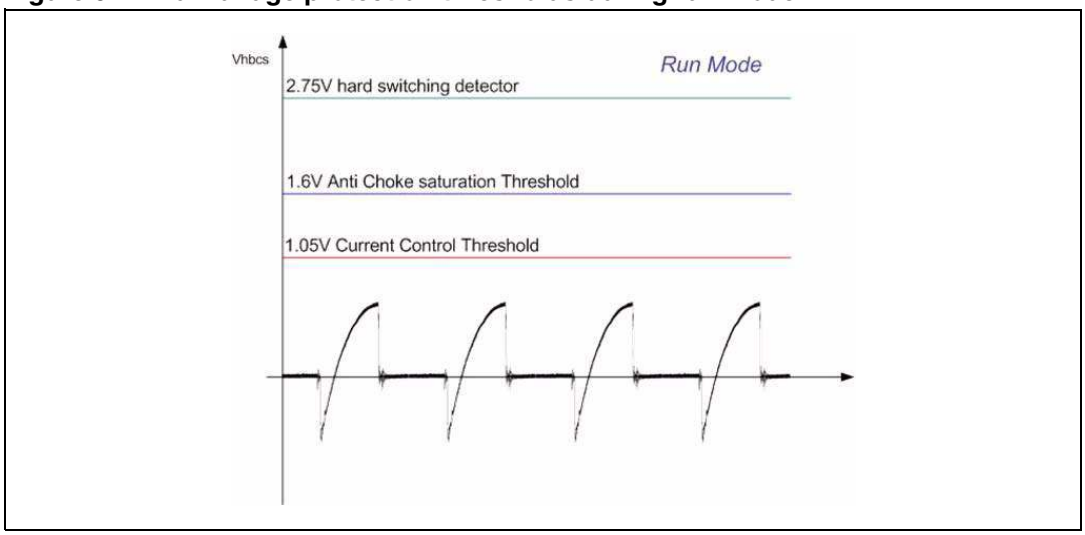
3. Ignition: At the end of the TCH cycle, the EOI pin is left free in high impedance mode. Therefore, the capacitor connected between EOI and ground is charged by RF through R_{PRE}. The current sunk from the RF pin decreases exponentially, and the frequency along with it. An exponential decrease in switching frequency causes a linear increase of the lamp voltage. When the lamp voltage reaches the strike value, the lamp ignites. Ignition time is set by the value of R_{PRE} and C_{IGN}.
During ignition current control protection, anti-ballast choke saturation protection and leading edge blanking are all active.

Figure 8. Half-bridge protection thresholds during ignition



4. Run mode: When the EOI voltage reaches 1.9 V, the IC enters run mode and the switching frequency is set only by R_{RUN}. Current control protection and anti-ballast choke saturation are now active with a lower threshold, leading edge blanking is not active and a fast hard switching detector is activated.

Figure 9. Half-bridge protection thresholds during run mode

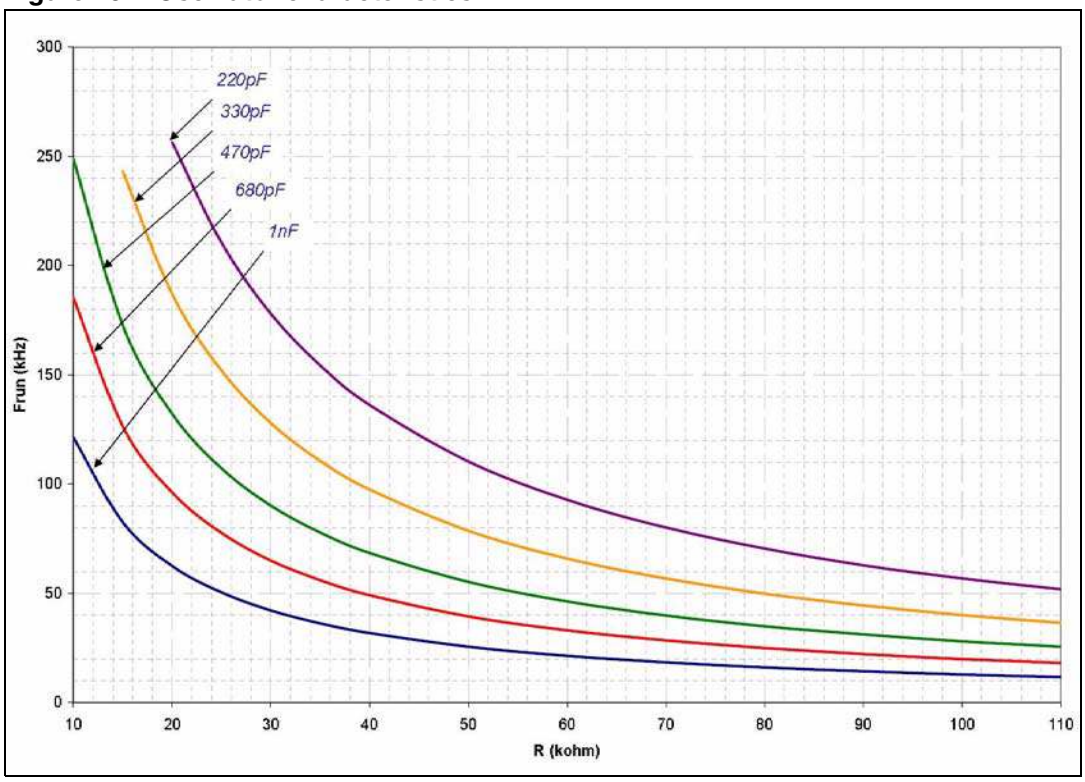


The oscillator characteristic curves represent the half bridge frequency versus the resistance R placed between RF pin and ground. During preheating R is equal to R_{RUN} in parallel with R_{PRE} whereas during Run mode R is equal to R_{RUN}. Each curve is related to a value of the C_{OSC} capacitor and are depicted in Figure 10.

The value of C_{OSC} is measured between pin 1 (OSC) and 15 (GND); for other capacitor values please refer to AN2870.

The right value of R during preheating and run mode can be found graphically considering the curve related with the chosen capacitor and respectively F_{PRE} and F_{RUN}“

Figure 10. Oscillator characteristics



Some useful equations are given:

$$T_{PRE} = T_{Tch} = \frac{4.63}{I_{CH}} C_d + R_d C_d \cdot \ln\left(\frac{4.63}{1.5}\right)$$

$$T_{IGN} \cong 3 \cdot R_{PRE} \cdot C_{IGN}$$

6.3 Startup sequence with old or damaged lamps

When an old lamp is connected to the ballast the strike voltage is higher than the nominal voltage and may also be higher than the safety threshold. In this case the lamp can ignite in a time longer than ignition time or may not ignite. In both cases, during ignition time, because of the frequency decrease, the voltage at the output of the ballast can easily reach dangerous values.

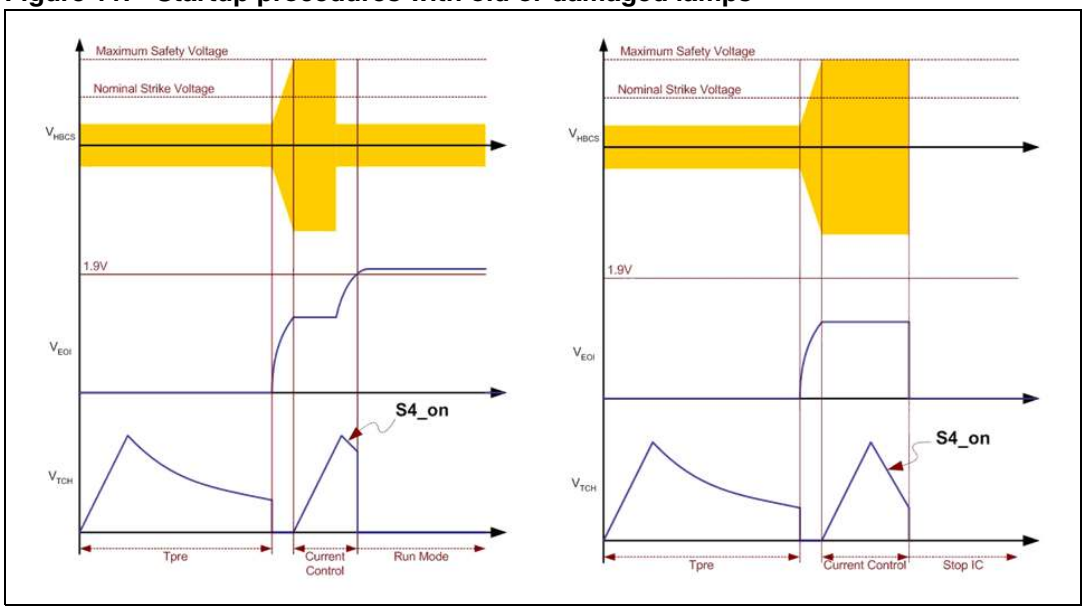
The same occurs if the lamp tube is broken: the lamp cannot ignite and the lamp voltage must be limited.

During ignition time, the L6585DE senses the current flowing into the lamp through a sense resistor connected to the HBCS pin. If the HBCS pin voltage reaches 1.6 V, a small amount of current is sunk from the EOI pin causing a small frequency increase. This frequency modification results, macroscopically, in a frequency regulation and therefore a current regulation and a lamp voltage limiting.

As soon as the HBCS pin voltage reaches 1.6 V, the TCH pin starts to charge Cd: when the TCH voltage reaches 4.63 V, the TCH pin is no longer left free (as during preheating), but it sinks 26 uA, causing a faster discharge of Cd. When the TCH voltage reaches 1.5 V, the pin is pulled down and HBCS voltage is checked. If it is above 1.05 V the IC is stopped.

If the lamp ignites during this reduced TCH cycle, the EOI pin stops sinking current and if it reaches 1.9 V, the IC enters run mode and TCH pin is immediately pulled down.

Figure 11. Startup procedures with old or damaged lamps



It can be noted that the reduced TCH cycle time depends only on the value of Cd. It is suggested to start from the choice of Cd in order to obtain the protection time, and then can proceed to the choice of Rd to obtain the desired T_{PRE}.

$$T_{Tch,reduced} = C_d\left(\frac{4.63}{I_{Tch,source}} + \frac{4.63 - 1.5}{I_{Tch,snk}}\right) \cong C_d \cdot 0.26974 \cdot 10^6$$

6.4 Old lamp management during run mode

During run mode, an old lamp can exhibit three different abnormal behaviors:

- Rectifying effect
- Over-current
- Hard switching event

6.5 Rectifying effect

The rectifying effect is related to a differential increase of the ohmic resistance of the two cathodes. The lamp equivalent resistance is therefore higher when the lamp current flows in one direction than in the other. The current waveform is distorted and the mean value of the lamp current is no longer zero. The EOL pin is the input of an internal window comparator that can be triggered by a voltage variation due to rectifying effect.

The reference of this comparator and the amplitude of the window can be set by connecting a suitable resistor to EOLP pin as indicated in following table:

Table 5. EOL window comparator configuration table

EOLP resistor range	Reference	Window amplitude (Wv)
22 k ÷ 27 k	V_{CTR}	+160 mV / -150 mV
75 k ÷ 91 k	2.5 V	240 mV
220 k ÷ 270 k	V_{CTR}	+ 250 mV / -240 mV
> 680 k	2.5 V	720 mV

The reference of this comparator can be set at a fixed voltage or at the same voltage as the CTR pin.

The fixed reference configuration (see *Figure 12*) can be used when the lamp is connected to ground, and requires two Zener diodes in order to shift the mean value of the lamp voltage to 2.5 V. The values of the two Zeners affect the symmetry of the intervention of the protection: the best symmetry is obtained choosing two values whose difference is equal to twice the reference voltage:

- $V_{UP} = V_{REF} + V_{Z2} + V_{F1} + W/2$
- $V_{DOWN} = V_{REF} - (V_{Z1} + V_{F2}) - W/2$
- $V_{UP} = - V_{DOWN}$
- $2\ V_{REF} = V_{Z1} - V_{Z2}$

Where V_{UP} and V_{DOWN} are the maximum allowed values of V_K

The tracking configuration (see *Figure 13*) is useful when the lamp is connected between choke and blocking capacitor in the block capacitor-to-ground configuration. In this configuration the voltage across the blocking capacitor is affected by the voltage ripple superimposed on the PFC output. Using a reference affected by the same ripple helps to reject it and avoid premature triggering of the comparator.

As soon as the comparator is triggered, a Tch cycle starts in order to improve the noise immunity.

Figure 12. End-of-life protection in lamp-to-ground configuration

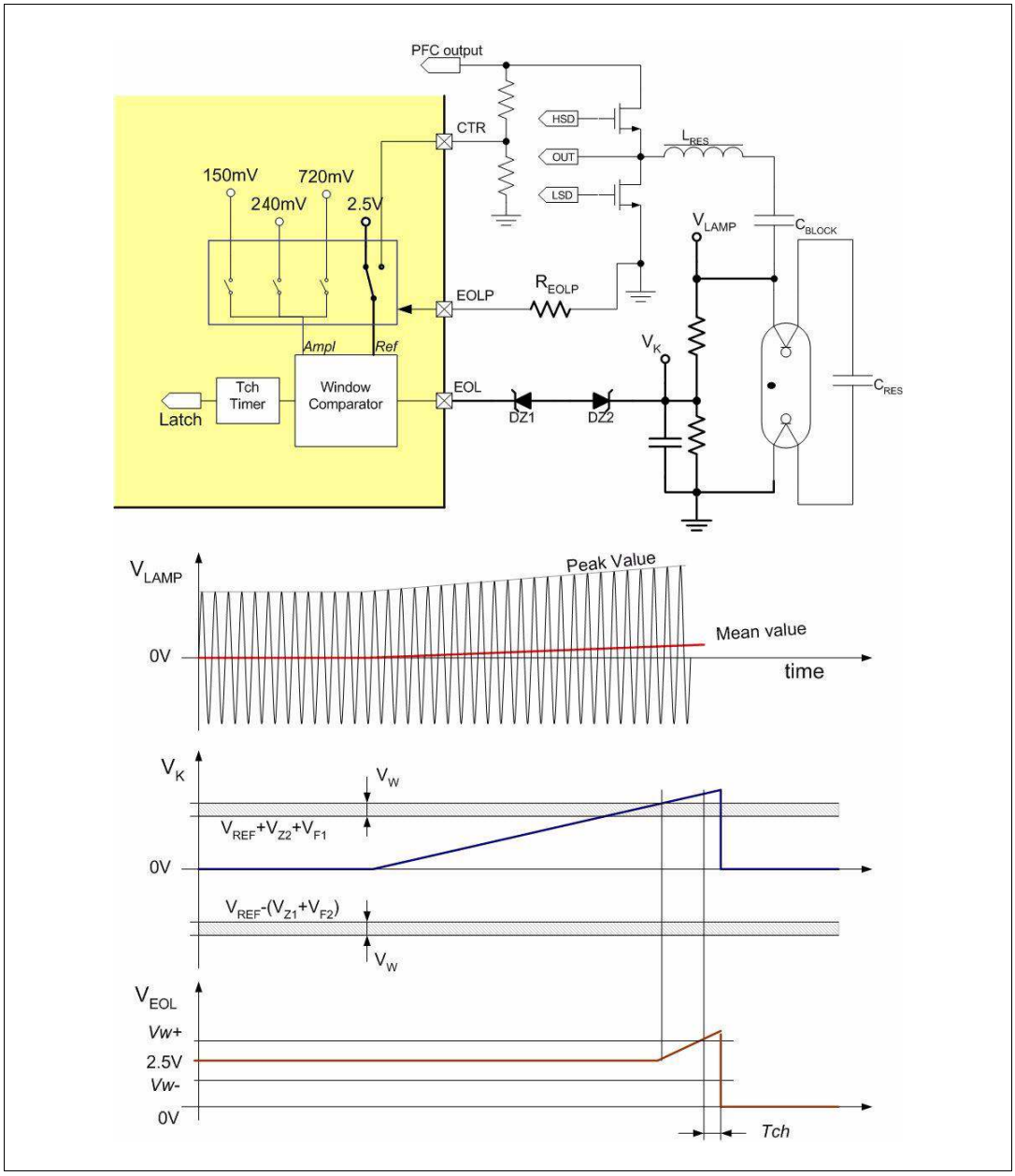
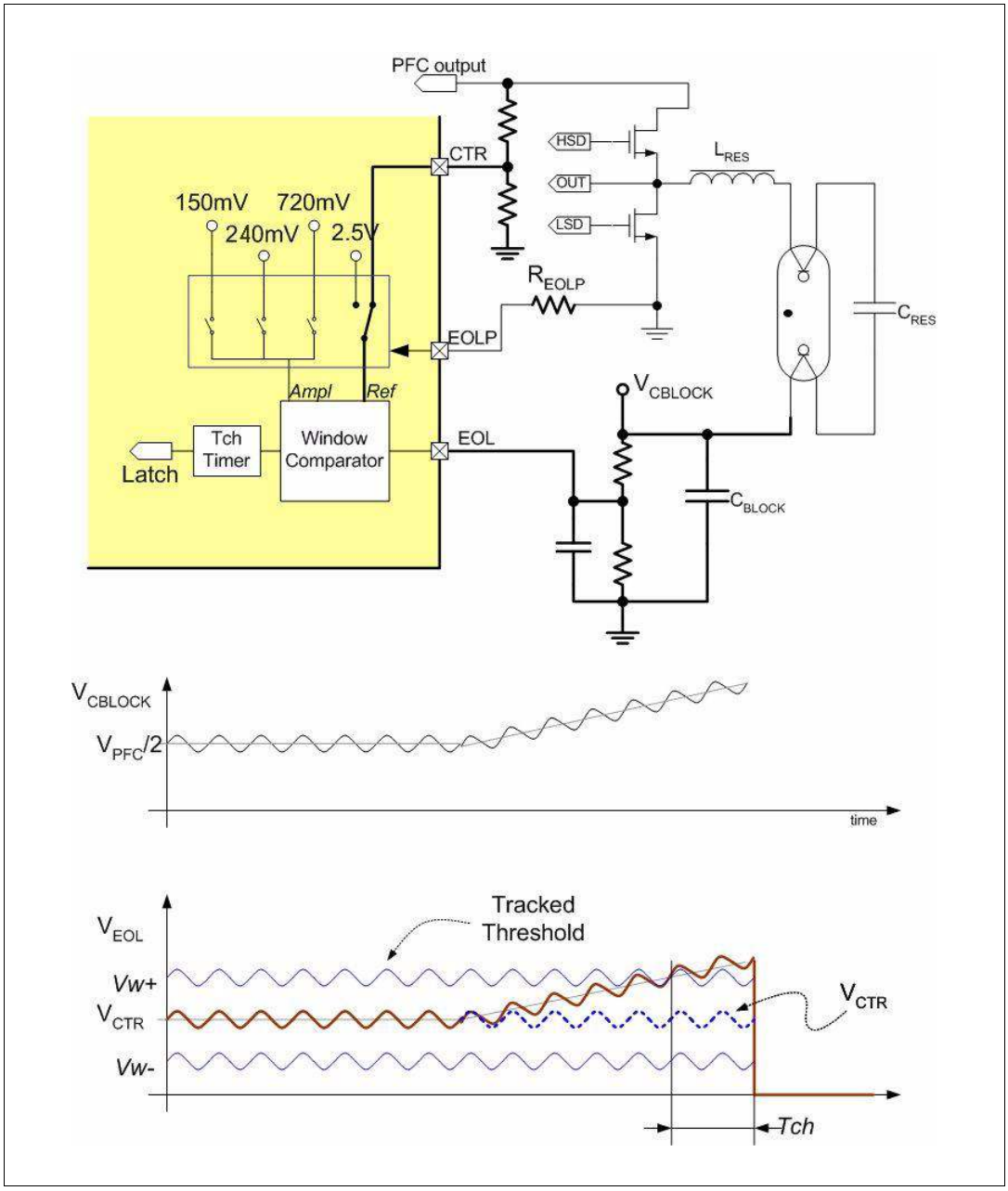


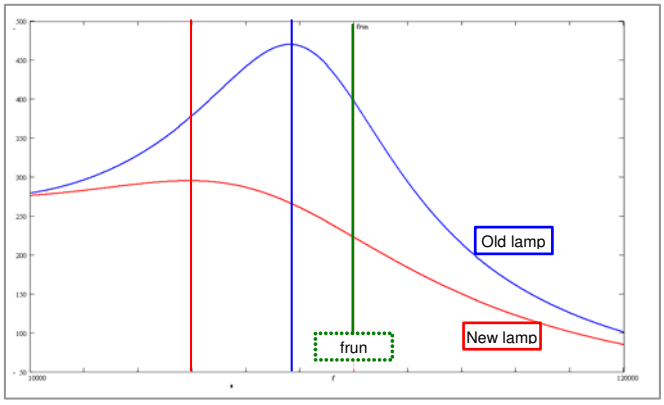
Figure 13. End-of-life protection in blocking capacitor-to-ground configuration



6.6 Over-current protection

The appearance of over-current and hard switching events are related to a symmetrical increase of the ohmic resistance of the two cathodes. The overall effect results in an increased equivalent resistance of the lamp and a subsequent modification of the resonance curve of the resonance network (see *Figure 14*).

Figure 14. Resonance curve modification due to lamp ageing



The increasing of the resonant peak causes over-current that is managed by the L6585DE in the same way as in ignition mode, but the limiting threshold and checking threshold are respectively 1.05 V and 0.82 V.

6.7 Hard switching protection

When F_{RUN} is equal to the peak of the resonance curve, the load seen by the half-bridge is purely resistive. In this case, zero voltage switching is no longer present and the MOSFET experiences high current spikes at turn on. The voltage at HBCS pin shows these peaks whose voltage value can be greater than 3 V with a duration that depends on how close the resonant frequency and the operating frequency are. Typical values go from 40 ns to around 200 ns. These spikes may overheat the MOSFETs but, if correctly detected, can prevent the risk of working below the resonance frequency (capacitive mode).

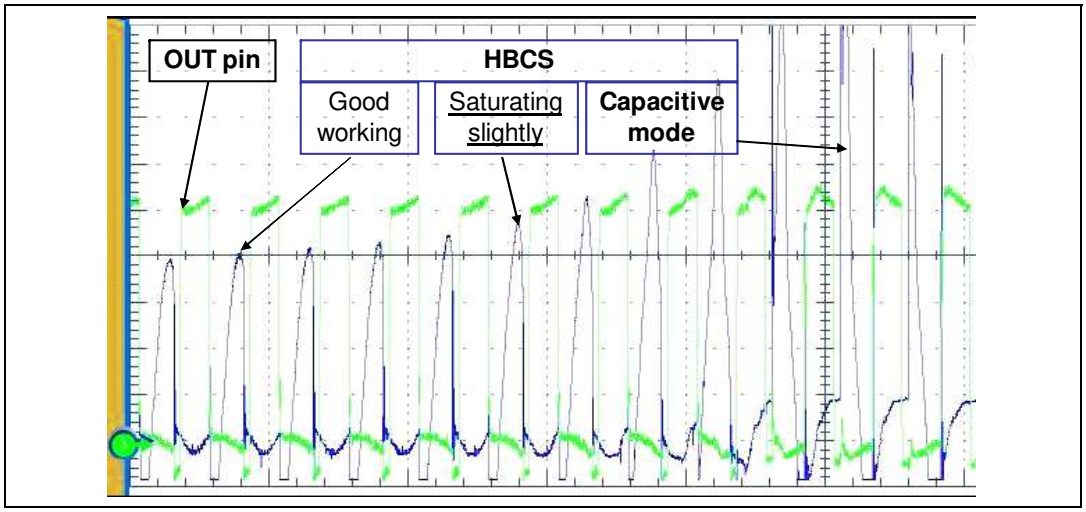
The L6585DE can detect these spikes by means of a 2.75 V threshold on HBCS pin, and a counter that shuts down the IC if 350 (typ.) subsequent spikes are detected.

This protection is blanked both during preheating and ignition.

6.8 Choke saturation protection

Ballast choke saturation implies that very high currents flow into resonance network and an almost instant modification of the resonance curve occurs in a way that the operating point lies immediately in capacitive mode. Steady operation in capacitive mode heavily damages the ballast.

Figure 15. Example of capacitive mode operation due to ballast choke saturation



Therefore, in ignition and run mode a comparator, connected to the HBCS pin, is active with a threshold respectively equal to 2.75 V and 1.6 V. It senses very high currents flowing in the ballast sense resistor and immediately latches the IC in low consumption mode. The width of the triggering spike is above 200 ns. This guarantees that, during run mode, hard switching events (typical duration between 40 ns and 100 ns) cannot trigger the comparator.

However, hard switching protection and anti-saturation protection are not perfectly independent. Regarding the pulse width we can indicate four different regions:

a) Spikes with a duration less than 40 ns: (noise region) no protection can be triggered.

b) Spikes with a duration between 40 ns and 100 ns: (HSw region) only hard switching protection will be activated after around 420 events.

c) Spikes with a duration between 100 ns and 200 ns: (uncertainty region) hard switching protection is activated, but also anti-saturation protection can be activated, which may result in a sort of early activation of hard switching protection or retarded activation of anti-saturation protection (in this case the saturation of the choke won't be deep).

d) Spikes with a duration longer than 200 ns: (ASP region) anti-saturation protection will certainly be activated at the first event.

Figure 16. Half-bridge current sense pulse detection areas

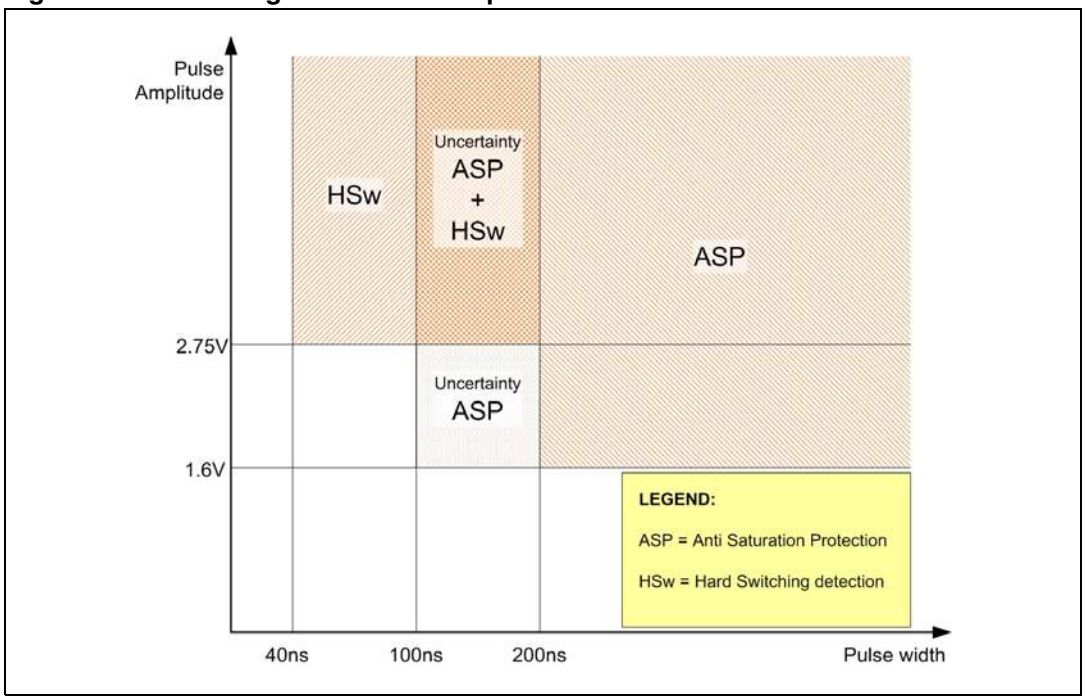


Table 6. Table of faults

Fault	Active during			Condition	IC behavior	Required action
	PH	Ign	Run			
Fault with immediate activation of latched operating mode						
Shutdown	✓	✓	✓	V_{CTR} < 0.75 V	- Drivers stopped - IC low consumption (Vcc clamped)	V_{CTR} > 0.75 V (IC restarts with PH sequence)
PFC feedback disconnection	✓	✓	✓	V_{CTR} > 3.4 V and V_{INV} < 1.2 V	- Drivers stopped - IC low consumption (Vcc clamped)	Board failure
Half bridge anti-saturation protection		✓	✓	Ignition: V_{HBCS} > 2.75 V Run mode: V_{HBCS} > 1.6 V	- Drivers stopped - IC low consumption Vcc clamped)	Turn off – turn on sequence
Fault with immediate activation of a non latched operating mode						
PFC dynamic over-voltage	✓	✓	✓	V_{CTR} > 3.4 V	- PFC driver stopped	Wait for output voltage reduction
PFC protection over-current	✓	✓	✓	V_{PFCCS} > 1.7 V	- PFC driver stopped	Wait for next starter event
Fault with timed activation of latched operating mode						
PFC static OVP	✓	✓	✓	V_{COMP} < 2.25 V	- PFC driver stopped - Tch cycle starts - At the end of cycle, if V_{COMP} < 2.25 V IC is latched	Check the mains voltage
Lamp end-of-life			✓	V_{EOL} outside allowed range (set by R_{EOLP})	- Tch cycle starts - At the end of the cycle if V_{EOL} is out of range the IC is latched	Replace the lamp with a new one
Lamp over-current		✓	✓	Ignition: V_{HBCS} > 1.6 V Run mode: V_{HBCS} > 1.05 V	- Frequency control activated and Reduced Tch Cycle (RTC) starts - At the end of RTC the threshold is reduced (1.05 V during ignition and 0.82 V during run mode) - If V_{HBCS}>reduced threshold IC is stopped	Replace the lamp with a new one
Lamp ageing causing hard switching			✓	V_{HBCS} > 2.75 V	- After 350 subsequent hard switching events IC is stopped	Replace the lamp with a new one

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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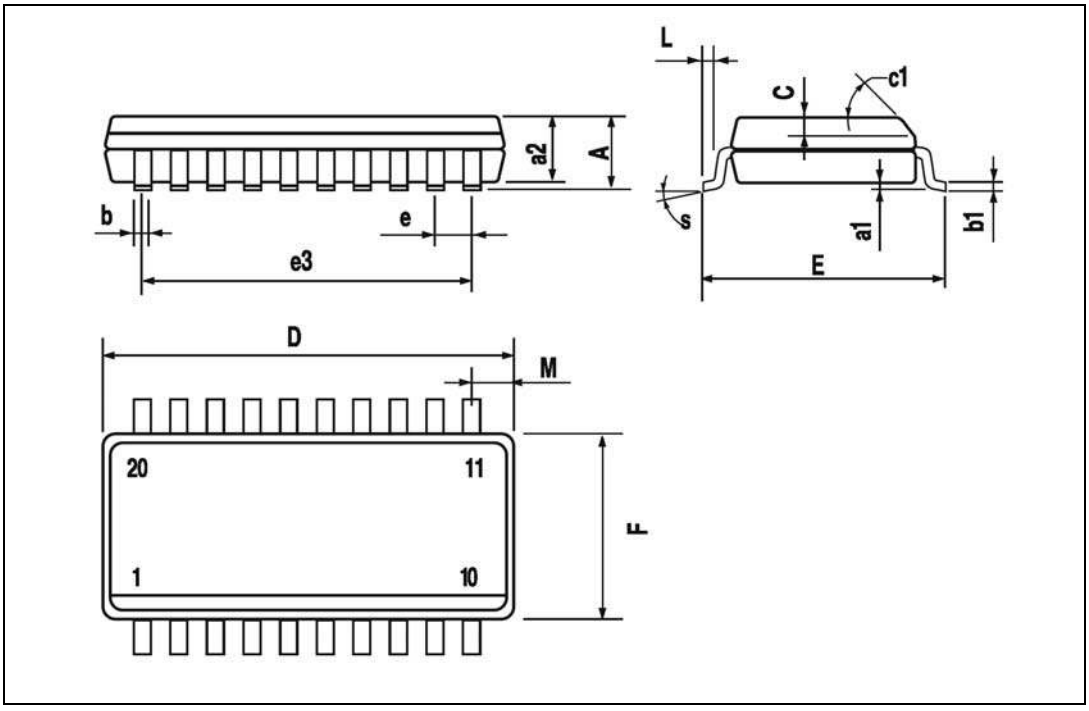
Table 7. SO-20 mechanical data

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

Figure 17. Package dimensions



8 Ordering information

Table 8. Order codes

Order codes	Package	Packaging
L6585DE	SO-20	Tube
L6585DETR	SO-20	Tape and reel

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Nov-2008	1	Initial release
10-Apr-2009	2	Updated *Table 1*,*Table 2*, *Table 3*, *Figure 4*

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