AS3900

27MHz Low Power Star Network Transceiver

1 General Description

The AS3900 is a low power FSK transceiver ideal for battery-operated short range devices (SRD) applications in which a limited amount of data (data rate up to 210 kbit/s) need to be transferred. The device can be configured as transceiver, transmitter only or receiver only system and operates in one channel in the worldwide ISM band at 27 MHz.

The frequency of the external oscillator determines the operating frequency. Use of 27 MHz is in particular advantageous for communication in close proximity of the human body due to the low absorption of the signal by tissue because of the low specific absorption rate at 27 MHz. The device incorporates a serial digital interface (SDI), which enables bidirectional communication with external system components.

The integrated real-time-clock, sophisticated wake-up functionality, and link manager enable current efficient control of all communication events and eliminate the need for an expensive microcontroller.

The AS3900 supports data transfer in burst mode (bidirectional, controlled by link manager), semi-continuous (bidirectional, controlled by microcontroller) and continuous mode (unidirectional, controlled by microcontroller) and requires only a small number of external components.

2 Key Features

- FSK transceiver
- Operating frequency 27.12 MHz (ISM - band)
- Integrated real-time-clock (RTC) based on 32.768kHz XTAL
- FM deviation selectable (±106 kHz, ±53 kHz)
- Data transfer in burst mode and (semi-)continuous mode
- Data rate adjustable to 26.5, 53, 106, 212 kbit/s
- Low average current consumption in Tx and Rx mode
- Output power adjustable to 0, +5, +10 dBm
- Integrated OOK based wake-up system
- Link manager for control of star network with up to 8 clients
- Bidirectional serial digital interface (SDI)

Main Characteristics

- Operating temperature range -40ºC to +85ºC
- Operating supply voltage 2.2V to 3.6V (Functional down to 2.0V)
- Rx current consumption 3.8 mA (typ.)
- Tx current consumption 4.9 mA@0dBm, 7.6 mA @10dBm
- Maximum output power 10 dBm (delivered to matching network and antenna)
- Receiver sensitivity –88 dBm @ 106 kbit/s
- Polling mode average current consumption typ. 2.5µA
- Power down current consumption max. 700nA
- Typ. communication range using small antenna 1.2m@0dBm, 2.5m@10dBm
- QFN 28 pin (5x5) package

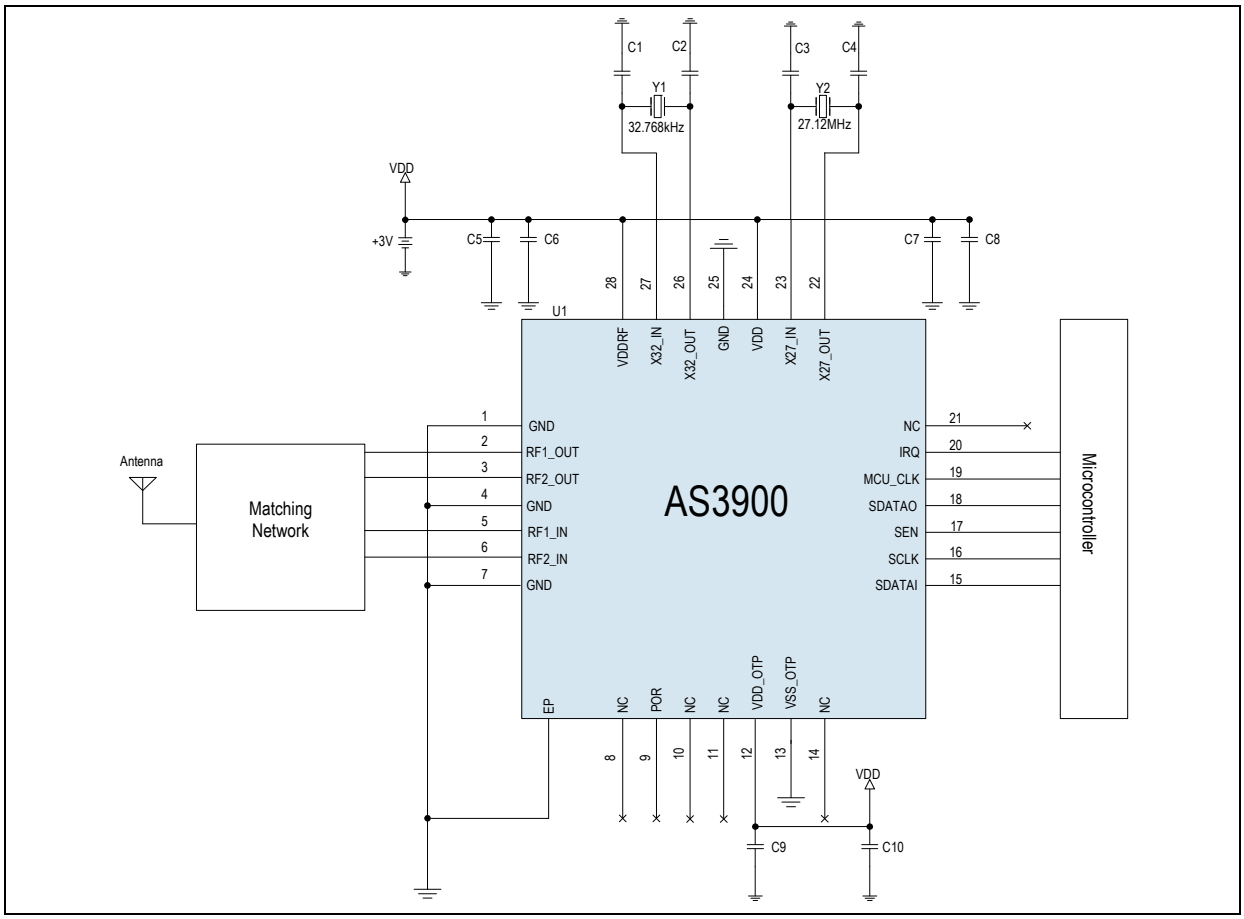
Additional Features

- Reliable pairing and synchronization of master and clients
- Automatic 16 bit CRC computation in burst mode
- Auto-acknowledgement and re-transmit
- Programmable timers to assign variable communication cycle times
- Reliable system start due to internal POR
- Programmable microcontroller clock frequency
- Separate interrupt request line
- Battery level detector
- Digital RSSI value accessible in register
- User programmable Identification with OTP memory (24 bits)

3 Applications

The AS3900 is ideal for reliable low-power short-range data exchange, data transfer among devices in close proximity of human body (Body Area Networks), simple control networks (home, industry), and interactive remote controls. A typical application can be designed in combination with a microcontroller, an antenna and a few additional passive components.

Figure 1. Typical Application Diagram of Low Power Star Network Transceiver AS3900



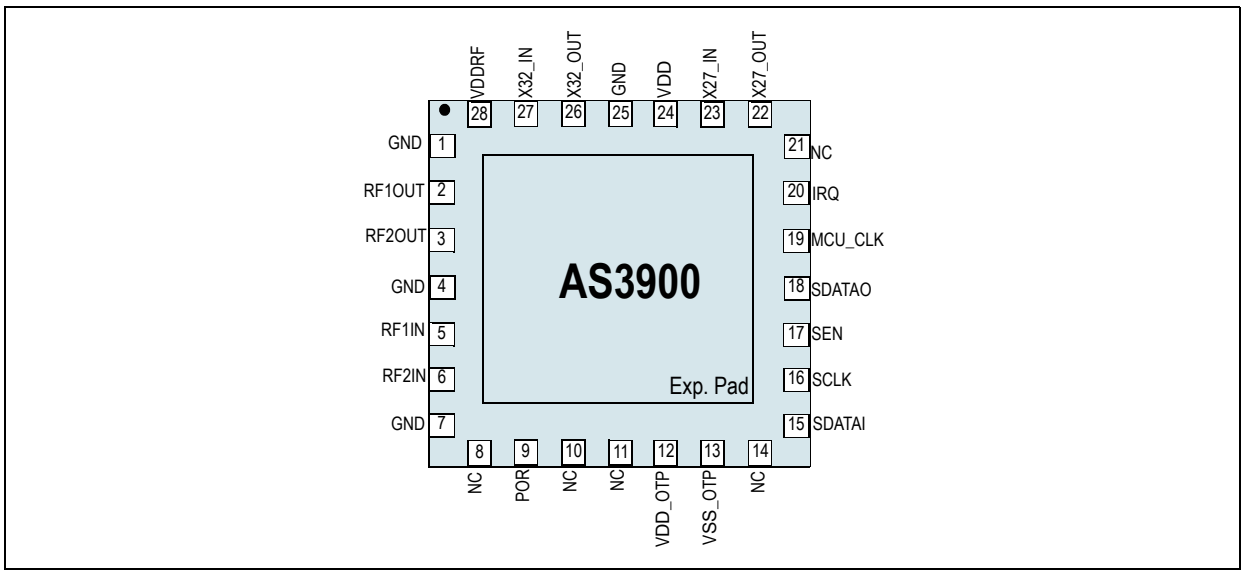
Abbreviations

ACK:	Acknowledgement
ACP:	Acknowledgement Plus Data
BER:	Bit Error Rate
CRC:	Cyclic Redundancy Check
FSK	Frequency Shift Keying
I/Q:	In-Phase/Quadrature
ISM	Industrial, Scientific and Medical
LNA	Low Noise Amplifier
MCU	Microcontroller
NAK	Negative Acknowledge Character
NAR	Negative Acknowledge Return
OOK	On Off Keying
OTP	One Time Programmable
PER	Packet Error Rate
PA	Power Amplifier
PRBS	Pseudorandom Binary Sequence
RSSI	Received Signal Strength Indication
POR	Power on Reset
REG	Register, MAIN Register
SREG	SHADOW Register
RTC	Real Time Clock
RF	Radio Frequency
RX	Receive – Receive Mode
SRD	Short Range Devices
TX	Transmit, -Transmit Mode
XREF	Reference Crystal Oscillator
XTAL	Crystal Oscillator

Contents

4 Pin Assignment

Figure 2. AS3900 Pin Assignment (Top View)



4.1 Pin Description

Table 1. QFN 28 pin Package

Pin Name	Pin Number	Pin Type	Description
GND	1	S	**Negative RF Supply Voltage.** Ground reference point for VDDRF.
RF1OUT	2	AO	**Transmitter Positive Output.** Analog Push/Pull Output of Power Amplifier for positive amplitude. Output Impedance can be programmed to 12.5Ω or 25Ω. Transmitter can be programmed to single ended or true-differential analog outputs.
RF2OUT	3	AO	**Transmitter Negative Output.** Analog Push/Pull Output of Power Amplifier for negative amplitude. Output Impedance can be programmed to 12.5Ω or 25Ω. Transmitter can be programmed to single ended or differential analog outputs. In single ended mode RF2OUT is connected to GND.
GND	4	S	**Negative RF Supply Voltage.** Ground reference point for RF outputs and inputs.
RF1IN	5	AI	**Receiver Positive Input**. Positive analog input of differential Low Noise Amplifier.
RF2IN	6	AI	**Receiver Negative Input.** Negative analog input of differential Low Noise Amplifier.
GND	7	S	**Negative RF Supply Voltage.** Ground reference point for RF outputs and inputs.
NC	8		Not connected. Leave the pin floating.
POR	9	DO	**Power On Reset output:** Digital Output that indicates hardware reset of the device. Reset Low: VDD > 1.35V
NC	10		Not connected. Leave the pin floating.
NC	11		Not connected. Leave the pin floating.
VDD_OTP	12	S	**Positive OTP Supply Voltage.** 2.2V to 3.6V for operation mode. For fuse mode apply a minimum supply voltage of 3.3V. Buffer capacitors of 10µF and 100nF are needed for fuse mode.

Table 1. QFN 28 pin Package

Pin Name	Pin Number	Pin Type	Description
VSS_OTP	13	S	**Negative OTP Supply Voltage**. Ground reference for VDD_OTP. Decouple point for buffer capacitors of VDD_OTP.
NC	14		Not connected. Leave the pin floating.
SDATAI	15	DI	**Serial Digital Interface DATA input.** Serial Data Input for writing registers. The bits are clocked in on the falling edge of SCLK.
SCLK	16	DI	**Serial Digital Interface Clock.** A serial clock provides the SCLK for accessing data from the AS3900. Write and read operation is provided by the SCLK.
SEN	17	DI	**Serial Digital Interface Enable.** CMOS digital input. Falling edges on SEN ends a read or write operation and frames the serial data transfer.
SDATAO	18	DO	**Serial Digital Interface DATA output.** Serial Data Output for reading registers. The bits are clocked out on the rising edge of SCLK and can be read from the microcontroller on the falling edge of SCLK.
MCU_CLK	19	DO	**Microcontroller Clock Output.** Programmable Clock for microcontroller that is derived from the 27MHz crystal oscillator. System frequency for microcontroller can be adjusted between 188kHz and 3.39MHz.
IRQ	20	DO	**Interrupt Output.** Digital CMOS Output for external interrupt input at microcontroller. If an interrupt condition is met a HIGH level is applied on the IRQ pin. The IRQ level is set to low level after the internal interrupt registers are read manually. An interrupt can be triggered on the rising edge of the IRQ pin.
NC	21		Not connected. Leave the pin floating.
X27_OUT	22	AO	**27MHz oscillator output.** Analog output for 27.12MHz crystal oscillator.
X27_IN	23	AI	**27MHz oscillator input.** Analog input for 27.12MHz crystal oscillator
V_{DD}	24	S	**Positive Digital Supply Voltage.** 2.2V to 3.6V. Decoupling capacitors (1µF, 100nF and 100pF) are recommended.
GND	25		**Negative Digital Supply Voltage.** Ground reference point for VDD. Decouple point for capacitors.
X32_OUT	26	AO	**32kHz oscillator output.** Analog output for 32.768kHz crystal oscillator.
X32_IN	27	AI	**32kHz oscillator input.** Analog input for 32.768kHz crystal oscillator
V_{DD}RF	28	S	**Positive RF Supply Voltage.** 2.2V to 3.6V. Decoupling capacitors (1µF, 100nF and 100pF) are recommended.

5 Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Detailed Description are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
DC supply voltage (V_{DD})	-0.5	5.0	V	
Input pin voltage(V_{IN})	-0.5	5.0	V	
Input current (latchup immunity) (I_{scr})	-100	100	mA	Norm: Jedec 78
ESD for digital pins (ESDD)	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
ESD for analog pins (ESDA)	±2.0		kV	Norm: MIL 883 E method 3015 (Human Body Model)
ESD for RF pins (ESDRF)	±1.5		kV	Norm: MIL 883 E method 3015 (Human Body Model)
Total power dissipation (P_t) (all supplies and outputs)		30	mW	TX: 8mA*3.6V=29mW
Storage temperature (T_{strg})	-55	125	ºC	
Package body temperature (T_{body})		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	

6 Electrical Characteristics

VDDRF=VDD=VDD_OTP= 2.2V to 3.6V; TAMB= -45 to +85ºC; Typical values at VDD=3.0V and TAMB=25ºC; Unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Operating Conditions						
VDDRF	Positive analog supply voltage	Functional down to 2.0V	2.2		3.6	V
GND	Negative analog supply voltage		0		0	V
VDD	Positive digital supply voltage	Functional down to 2.0V	2.2		3.6	V
GND	Negative digital supply voltage		0		0	V
VDD_OTP	Positive OTP supply voltage	Buffer Capacitor connected here for FUSE Mode. In Fuse Mode a minimum supply voltage of 3.3V is needed. Functional down to 2.0V	2.2		3.6	V
VSS_OTP	Negative OTP supply voltage	Buffer Capacitor connected here for FUSE Mode	0		0	V
A - D	Difference of supplies	VDDRF – VDD GNDRF – VSS	-0.1		0.1	V
f_{clk}	System clock frequency			27.12		MHz
Current Consumption						
I_{PD}	POWER-DOWN mode				700	nA
I_{SB}	STANDBY mode	Timers running Wakeup Receiver listens every 1s		2.5		µA
I_{SL}	SLEEP mode	Timers running no data transmission		1.8		µA
I_{WRX}	WAKEUP RX mode			2.5		mA
I_{WTX}	WAKEUP TX mode, 10dBm			5.1		mA
I_{RX}	RX mode			3.8		mA
I_{TX10}	TX mode, 10dBm			7.6		mA
I_{TX5}	TX mode, 5dBm			5.5		mA
I_{TX0}	TX mode, 0dBm			4.9		mA
DC/AC Characteristics for Digital Inputs and Outputs						
CMOS Input						
V_{IH}	High level input voltage		0.7 * VDD			V
V_{IL}	Low level input voltage				0.3 * DVDD	V
I_{LEAK}	Input leakage current				1	µA
CMOS Output						
V_{OH}	High level output voltage		VDD - 0.5			V
V_{OL}	Low level output voltage				GND + 0.4	V
C_L	Capacitive load				50	pF

6.1 Electrical System Specification

6.1.1 General

Table 4. General

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD	Supply voltage	operational	2.2	3.0	3.6	V
VDD	Supply voltage	functional	2.0			V

6.1.2 Modulation Method

Table 5. Modulation Method

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Modulation			FSK		
	Frequency range	27.12 MHz ISM Band ±163 kHz		26.957		MHz
				27.283		
BR	Bit rate	Values derived from 27.12 MHz		26.5		kbit/s
				53		kbit/s
				106		kbit/s
				212		kbit/s
FDev	Frequency deviation	Values derived from 27.12 MHz		±53		kHz
				±106		

6.1.3 Transmission Frame

Table 6. Transmission Frame

Symbol	Parameter	Condition	Min	Typ	Max	Units
TFS	Transmission Frame Size	Minimum Frame Size		9		bytes
		Maximum Frame Size		32		
TPre	Preamble			16		bits
TAddr	Address			24		bits
TDataL	Data Length Indicator			8		bits
TSynch	Synchronization			8		bits
TPayl	Transmission Frame Payload	Minimum Payload		0		bytes
		Maximum Payload		26		
	CRC16	CRC-CCITT (CRC-16)			16	bits

6.1.4 Receiver RX

Table 7. Receiver RX

Symbol	Parameter	Condition	Min	Typ	Max	Units
Sensitivity		PER (Packet Error Rate) = 1% TFS = 32 bytes				
	@ 26.5kbps Datarate f_dev = 106kHz	420Ω seen by LNA input		90		dBm
				20.5		µVrms
	@ 53kbps Datarate f_dev = 106kHz	420Ω seen by LNA input		88		dBm
				25.8		µVrms
	@ 106kbps Datarate f_dev = 106kHz	420Ω seen by LNA input		88		dBm
				25.8		µVrms
	@ 212kbps Datarate f_dev = 106kHz	420Ω seen by LNA input		79		dBm
				72.7		µVrms
Blocking		C = Sensitivity + 3dB		B[dB] = C[dBm] - I[dBm]		
DR = 53kbps, f_dev = 106kHz	0 MHz	Unmodulated interferer		-25		dB
	0 MHz	Modulated interferer		16		dB
	± 1MHz	Unmodulated interferer		-26		dB
	± 1MHz	Modulated interferer		-21		dB
DR = 106kbps, f_dev = 106kHz	0 MHz	Unmodulated interferer		-25		dB
	0 MHz	Modulated interferer		16		dB
	± 1MHz	Unmodulated interferer		-24		dB
	± 1MHz	Modulated interferer		-22		dB
DR = 212kbps, f_dev = 106kHz	0 MHz	Unmodulated interferer		-25		dB
	0 MHz	Modulated interferer		25		dB
	± 1MHz	Unmodulated interferer		-15		dB
	± 1MHz	Modulated interferer		-15		dB
	Maximum input signal			100		mVrms
	IP3	Measured at the balun input with two carriers of -82dBm		-69		dBm
RSSI		4 Bit linear, read from register				
	RSSI start			10		µVrms
	RSSI stop			150		µVrms
	RSSI resolution			10		µVrms
	current consumption			3.8		mA

6.1.5 Transmitter TX

Table 8. Transmitter TX

Symbol	Parameter	Condition	Min	Typ	Max	Units
	TX linear output power	Power delivered to the matching network including antenna		10		dBm
				5		dBm
				0		dBm
Current Consumption						
I_{TX}	Current consumption	No power delivered to antenna	1.6	2.3	2.9	mA
I_{TX10}	Operation current consumption	10 dBm power delivered to matching network @ 420Ω		7.6		mA
	Harmonic Level	With Evaluation Board (including PCB antenna)	Meets: ETSI EN 300 220-1 v1.3.1 Sept. 2001 FCC CFR47 Section 15.227, May 2007			

6.1.6 Wakeup RX

Table 9. Wakeup RX

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Sensitivity @ 96kbps On Off Keying	420Ω seen by Wakeup receiver input		30		µVrms
	Maximum Input Signal			10		mVrms
	Antenna impedance	With external matching network		420		Ω
	Current consumption		1.8	2.5	3.3	mA

6.1.7 RTC Crystal Oscillator 32.768 kHz

Table 10. RTC Crystal Oscillator 32.768 kHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Crystal accuracy (initial)	Overall accuracy			±120	p.p.m.
	Frequency			32.768		kHz
	Start-up Time	Crystal dependent		200		ms
	Duty cycle	Depends on XTAL properties	45	50	55	%
	Current consumption			600		nA

6.1.8 XREF Crystal Oscillator 27 MHz

Table 11. XREF Crystal Oscillator 27 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Crystal accuracy (initial + temp + ageing)				±120	p.p.m.
	Frequency			27.12		MHz
	Duty cycle		45	50	55	%
	Start-up time	22 clock cycles of 32kHz XTAL		671		µs
	Current consumption	Crystal and Pulling Capacitor dependent		340		µA

6.1.9 Battery Level Detector

Table 12. Battery Level Detector

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD	Operation Supply Voltage		1.9		3.6	V
V_{LS}	Low Supply Voltage Threshold	Hysteresis = ±40mV 4 bit Register selectable		1.98 2.18 2.39 2.57		V

6.1.10 Power-On-Reset Generator

Table 13. Power On Reset Generator

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD	Operation Supply Voltage		0.0		3.6	V
V_{PHS}	Power ON Threshold	Rising slope (0.3V/ms) of Supply Voltage		1.35		V

7 Typical Operating Characteristics

Figure 3. Blocking of Interferer vs Frequency (DR=106kbps, f_dev=106kHz)

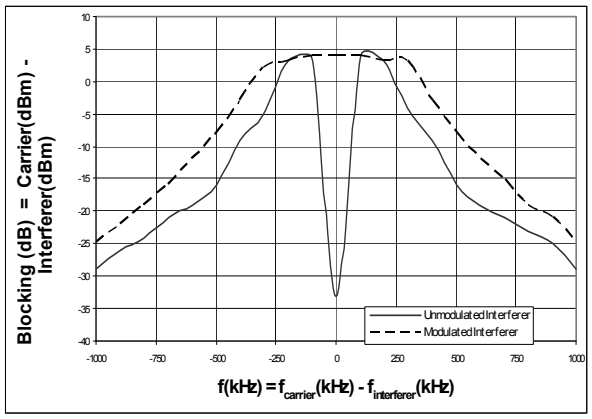


Figure 4. Blocking of Interferer vs Frequency (DR=53kbps, f_dev=106kHz)

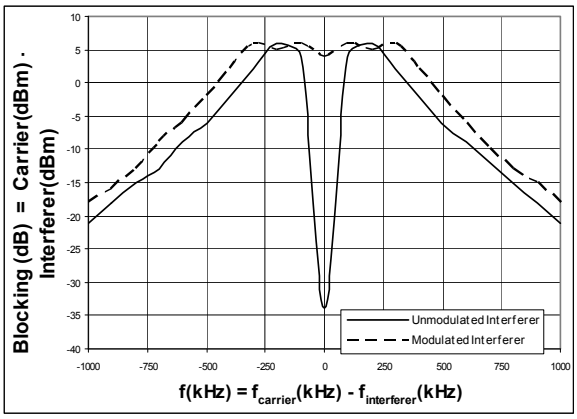


Figure 5. Supply Current vs. Impedance of Antenna+Matching Network (PA=differential, Rout=12.5Ohm, cont. Tx)

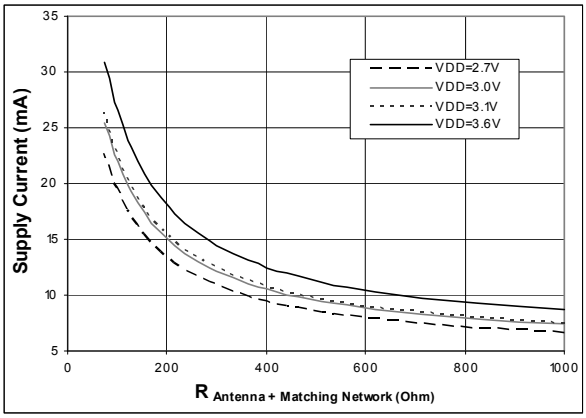


Figure 6. Output Power vs. Impedance of Antenna+Matching Network (PA=differential, Rout=12.5Ohm, cont. Tx)

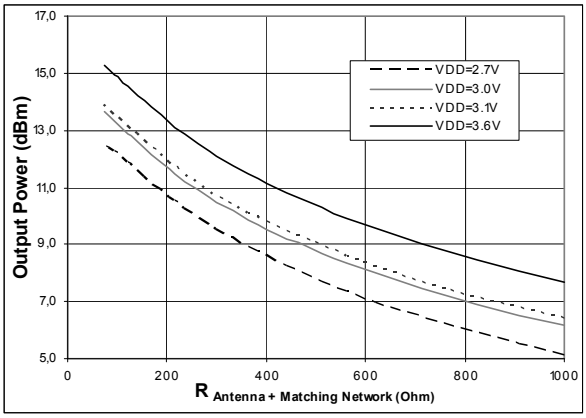


Figure 7. Output Power vs. Supply Voltage (PA=differential, R Ant+Matching=422Ohm, cont. Tx)

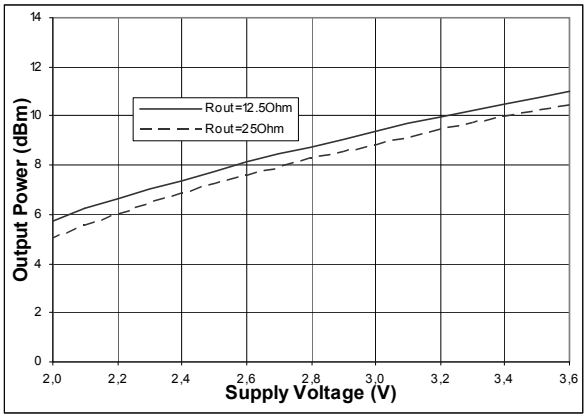
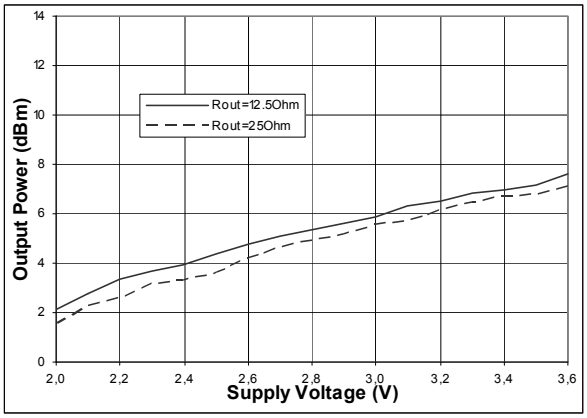


Figure 8. Output Power vs. Supply Voltage (PA=single ended, R Ant+Matching=422Ohm, cont. Tx)



8 Detailed Description

The AS3900 transceiver is an integrated solution of one receiver and one transmitter capable of supporting a bidirectional communication between one Master and up to eight Clients via the 27MHz ISM band. The AS3900 is designed to operate with a single 2.2V to 3.6V supply and consumes less than 3.8mA in receive mode and 7.6mA in transmit mode (10dBm). The device is even functional down to a supply voltage of 2.0V and has a built in battery level detector, that level can be read via the SDI interface.

The AS3900 provides an adjustable data rate of 26.5 kbps up to 212kbps and transmits an adjustable (via external matching circuitry) output power of maximal 10dBm. The transmission is done through a power amplifier that sends a Miller coded FSK modulated signal. A I/Q up mixer generates the modulated RF-signal based on the carrier of 27.12MHz. The deviation of the frequency shift can be set to ±106kHz or to ±53kHz in order to limit the allocated bandwidth in the ISM band. An integrated low pass filter cuts off additional interference frequencies.

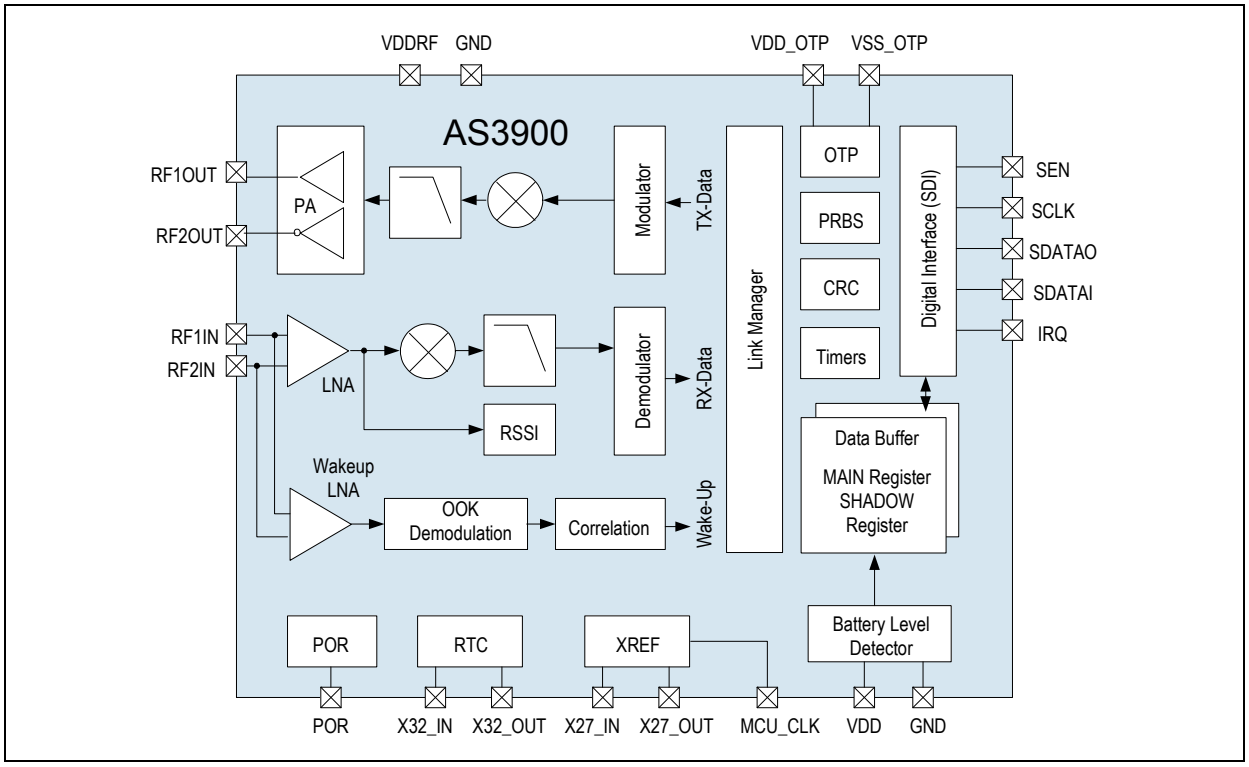
The analog outputs of the PA can be programmed as single ended or fully differentially, which doubles the transmitter output voltage level. In addition the output impedance of the PA can be selected between 25Ω and 12.5Ω. The output power is mainly determined by the applied output impedance of the antenna and the matching network.

The AS3900 features a zero-IF receiver. The receiver consists of a differential low noise amplifier (LNA) that amplifies the incoming RF signal. The actual received signal strength (RSSI) is measured and converted to a digital value that can be read via the serial data interface. Afterwards the incoming signal is down converted (I and Q) to the base band by the mixer. The I/Q signal is filtered and fed to the demodulator.

Furthermore the receiver consists of a Wakeup LNA. The amplified wakeup signal is demodulated and correlated with the OOK-pattern. This functionality guarantees very low power requirements ideal for battery-operated applications. The device is set to STANDBY mode and scans periodically for the ON OFF keying signal (OOK) with the Wakeup receiver, which only consumes an average current of 2.5µA. Once detected the AS3900 enters the normal RX mode.

A key feature of the AS3900 is the integrated Link Manager. The Link Manager controls all issues regarding the low level communication. It manages the link parameters and the timings in order to set-up and to maintain up to 8 communication links simultaneously. The link manager uses the integrated timers and the pseudorandom binary sequence (PRBS), to run the low level actions automatically. For reliable data transmission a 16 bit CRC block is integrated. Furthermore the transmitted data is Miller coded. Two crystal oscillators must be connected in order to generate the carrier of 27.12MHz and the time base for the timers (RTC), which is 32.768 kHz. The clock source for the MCU_CLK can be converted from the 32.768 kHz real-time clock or from the 27.12MHz carrier. The 4-wire SDI (Serial Data Interface) is used for configuration of the AS3900 and to serve the link manager. The SDI interface allows the access to the MAIN register as well as to the SHADOW register. The data for the RF transmission is saved into the data buffer at the Clients and can be collected at the Master that is again saved in the data buffer in the MAIN register. A simplified block diagram of the AS3900 is shown in Figure 9.

Figure 9. Block Diagram of Low Power Star Network Transceiver AS3900



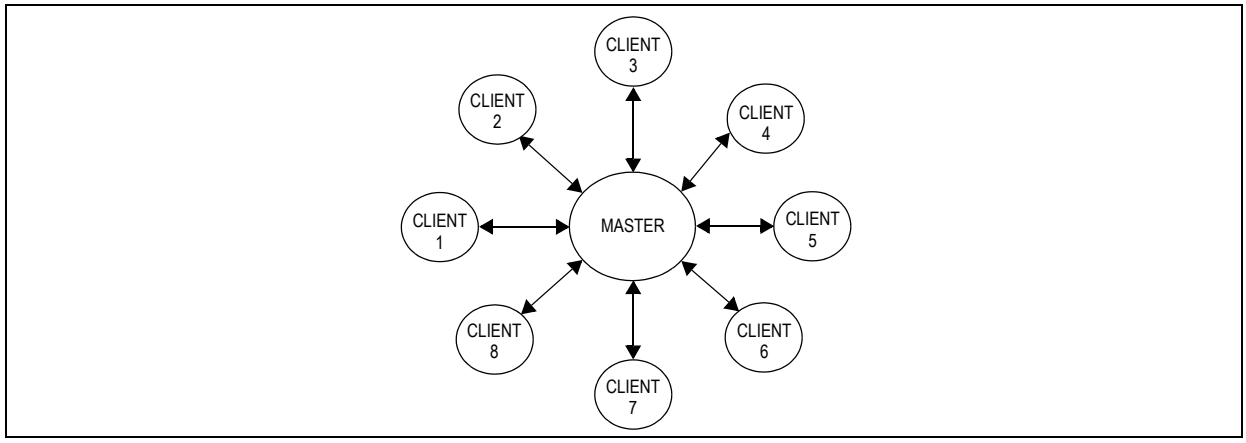
8.1 Network Management

The transceiver is optimized for short range, low data rate applications where low power consumption is very critical, and therefore the data is sent in short packages with higher data rate.

8.1.1 Network

The transceiver supports a star network consisting of one master and maximum 8 clients as presented in Figure 10. The master acts as a data processor and collector, the clients act as data producers. In one-way communication mode, a client sends a data package to a master and is not aware of lost packages. In two-way communication mode, a client sends a data package to a master, and waits an acknowledgement from the master. The master manages the parameters used for communication.

Figure 10. Star Network



8.1.2 Link Manager or Network Manager

The link manager has an essential role in receiving and transmitting of data in the star network. It manages the link parameters and the timings in order to set-up and to maintain up to 8 communication links simultaneously.

- Data transmission:
  The microcontroller (MCU) supplies data via SDI to an integrated TX data buffer from where the link manager takes the data, adds the needed network management bits (preamble, device ID, time code, and CRC), and enables the transmitter for transmitting the data package at the dedicated time slot.

- Data Reception:
  The link manager wakes up the receiver at the dedicated time slot. It checks the CRC of the payload data and if that is correct, it removes all network management bits and stores the data to a RX data buffer. The link manager gives an interrupt to the MCU, which can then retrieve data via SDI.

8.1.3 Principle of Communication

The data communication between the Master and the Client proceeds in the following way:

The MCU, via the serial data interface, writes the payload data into the data buffer of the AS3900. The link manager takes this data from the registers and adds the header for the network management. Preamble, Client ID, Timing Information, and CRC are added to the data, which takes 51 Bytes. The 192 bits (24 bytes) of data can be transmitted within one frame. The total maximum size is 75 Bytes (51 bytes header + 24 bytes data). The Client sends this packet at a certain time slot that is allocated for this Client. The timing information is part of every frame. Master and Client are re-synchronized automatically by using this timing information.

The Master opens the receive window at the allocated time slot and receives the packet. Therefore the link manager wakes up from sleep mode at this timeslot and turns on the RX mode (LNA is active). Afterwards the packet is checked for transmission errors with the 16 bit CRC check. If no error occurred the link manager removes the header and forwards the payload data to the data buffer. If the transmission is finished the MCU is informed via the interrupt line (IRQ). All settings can be changed in the register maps. Main and Shadow Register availability depends on operation mode.

8.2 Operating Modes

The following different operation modes are supported by the AS3900. These operating modes are entered automatically by the link manager and need not to be set manually. The device enters these modes depending on the current status of the communication. All operating modes require different current consumptions.

8.2.1 Power-down

Power-down mode is entered after connecting the battery. The POR signal is provided at the POR pin and registers will have their default values. The lowest current consumption is achieved in this mode. No clock is provided at MCU_CLK pin (the MCU must have other CLK source). The ENABLE pin LOW is needed to switch to Power-down (DATAO pin is set to High Impedance). Make sure to apply LOW level on the SDI-Interface to avoid leakage currents via the digital lines.

8.2.2 Standby

No active communication (idle mode), no connection (no synchronization) established between master and client, SDI is operational. Wakeup Timer and 32 kHz oscillator are running. Wakeup receiver is switched on periodically. Clock can be provided at MCU_CLK pin (divided 27MHz clock or 32 kHz clock). A Clock Interface Mode selection is required.

8.2.3 Sleep

This mode is active between communication time slots without data transmission. The timer (cycle time) indicate next active communication time slots. Timers and 32kHz oscillator are active in this mode.

8.2.4 Pairing

Permanent pairing: The device ID of the Clients are permanently stored in the Master (can be overwritten).

Temporary pairing: The device ID of the Clients are not permanently stored. The exchange of communication parameters is done for each temporary session.

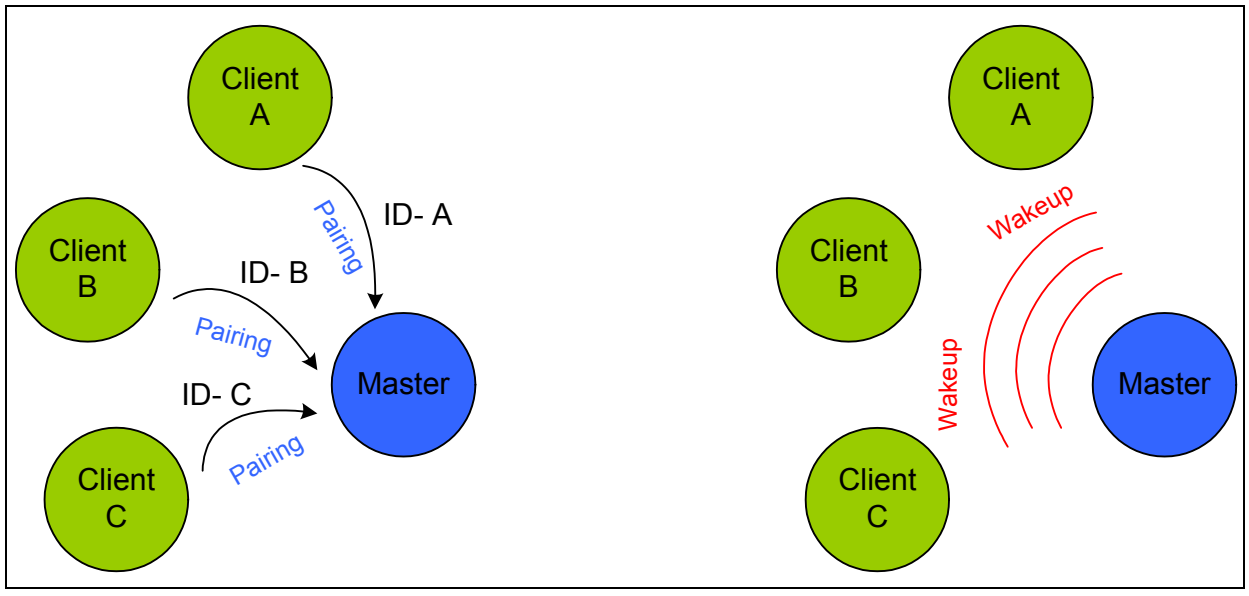
Note: It is important to note that the Pairing procedure must be executed in a clean RF environment. All Clients need to be close to the Master.

8.2.5 Wakeup

After a Wakeup sequence is received, the exchange of time code is performed and master is synchronized to client time base.

Applying wakeup means, Client (Master) is set to Wakeup receive mode for short time with a long wakeup interval. Master (Client) transmits long enough wakeup sequence to catch the receiving window of the Client (Master) or the Master is set to Wakeup receive mode for long time to catch the transmitted Client Wakeup sequences. Once the Client (Master) is woken up, it turns out of Sleep Mode and the time base is synchronized.

Figure 11. Pairing and Wakeup Principle



8.2.6 Data Transmit/Receive

The transmission is usually operated timer controlled in data packet mode. Packets can be sent bidirectional from 8 possible Clients to the Master. The Clients send their packets periodically selected by the cycle time. The AS3900 is also able to provide a not timer controlled bidirectional fast package mode, a timer controlled one way package mode and a not timer controlled one way streaming mode. The device features auto-acknowledgement as well as automatic retransmit of lost data.

The following different communication types are possible:

- One-way or bidirectional data transmission
- Timer controlled or not timer controlled transmission

8.3 Link Manager

8.3.1 Establishing Network

In order to build up a star network the connections between the Master and all available Clients must be established.

8.3.1.1 Permanent Pairing

The first arrangement of the star-network is associated with the keyword “Pairing”. Basically the ID of the available Clients are transmitted to the Master, because first all Clients are unknown for the Master. This is accomplished by sending a Wakeup signal from the Master to the Clients, so that all Clients exit from standby-mode. All Clients are woken up and answer after a random delay with the first data packet that includes the unique identification number (ID). The Master receives the packets from the different Clients after random time delays (set by MCU). After MCU verification the ID’s are stored in the Master’s ID registers.

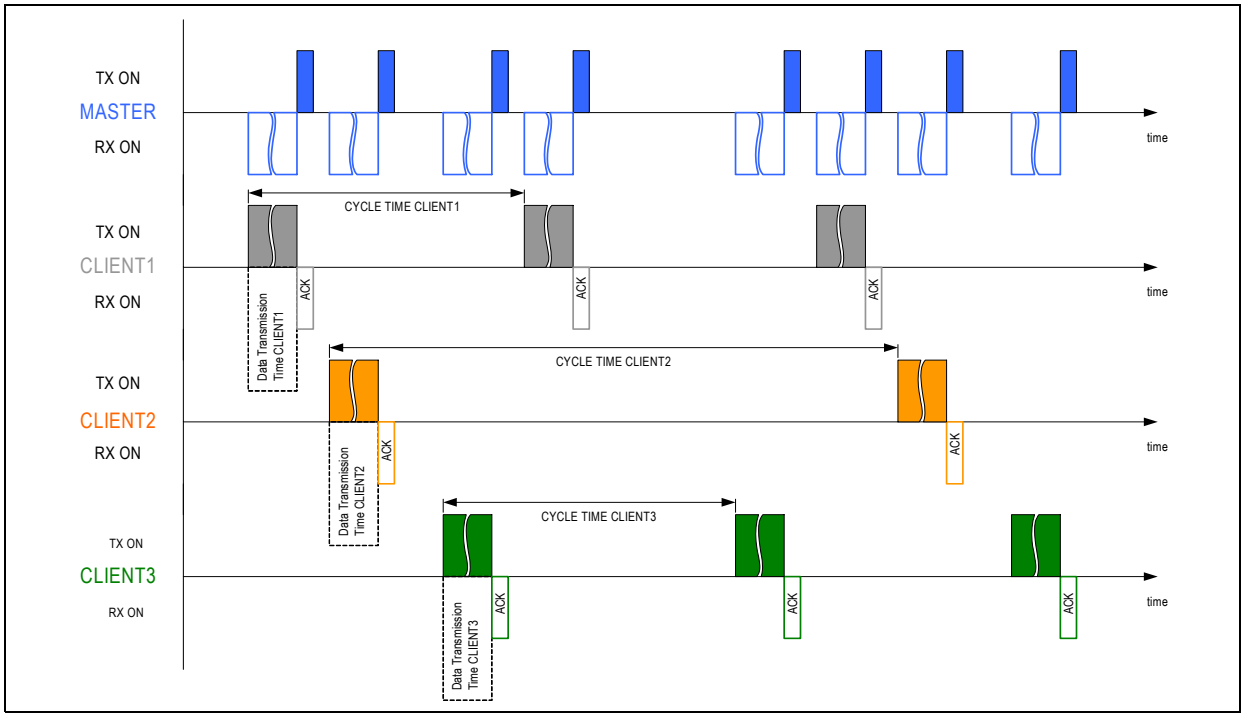
After that the Clients are paired to the Master and switched to Power-down mode. See detailed description in 8.6 Pairing.

8.3.1.2 Wakeup and Data Transmit/Receive

For transmitting data it is necessary to follow the listed procedure. First all Clients have to be set to Standby mode (periodically listen for Wakeup signal). Then the Master sends a “Wakeup” signal to exit all Clients from Standby mode. With this wakeup signal, all Clients are synchronized and send the timing information to the Master. Once synchronized, the whole communication is controlled by the Link manager in Auto-acknowledge mode. See detailed description in chapter 8.7 Transmission Modes.

The communication between the Master and up to eight Clients is timer controlled. Figure 8 shows the communication between 1 Master and 3 Clients. The cycle time is adjustable via the register map. The data rate and the frequency deviation must be the same for all members of the star network.

Figure 12. Time Division Multiplexing Principle



8.3.2 Handling the Link Manager

In general there are three different actions to operate the link manager.

- Setting register
- Sending direct commands
- Handling interrupts

8.3.2.1 Setting Registers

The AS3900 has a MAIN register with 82bytes and a SHADOW register with 22 bytes. All configuration registers are readable and writable and can be directly accessed via their register address. The registers are non volatile as long as the supply voltage is not decreased below the specified minimum level of 2.0V. The two registers contain blocks for configuration, bits for setting direct commands, status bits, an ID table, different data buffers as well as an interrupt table.

The complete register maps are directly addressable via the SDI interface that features:

- Reading of a single register byte
- Reading of register data with auto-incrementing address
- Writing of a single register byte
- Writing of register data with auto-incrementing address

8.3.2.2 Sending Direct Commands

The AS3900 can be directed via direct Commands that are executed via the SDI interface. With the direct Commands often used features of the device can be activated or deactivated. Some of the commands can also be accessed via the register maps.

8.3.2.3 Handling Interrupt

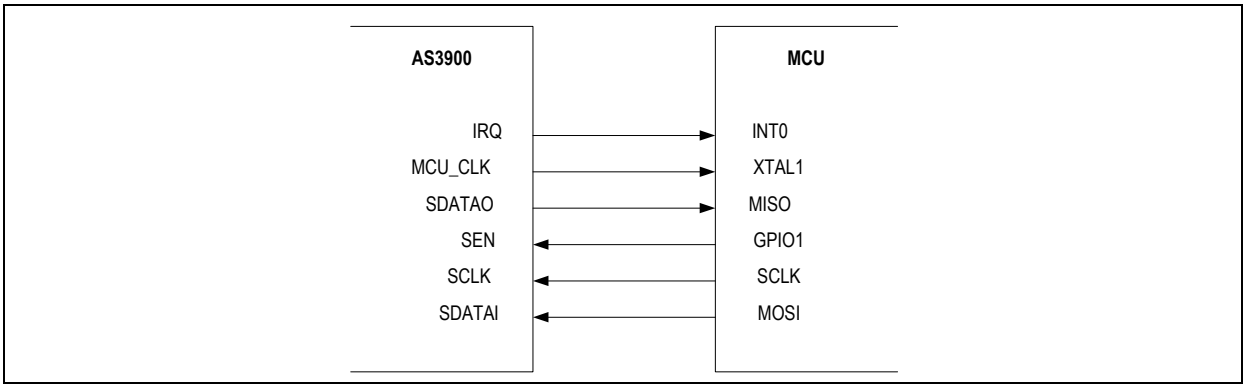
Different interrupts are set by the link manager according to certain events in the interrupt registers (in the MAIN register). 16 possible interrupt sources can be enabled or disabled by the use of the Interrupt Mask Register.

If one of the enabled interrupt conditions is met, the AS3900 apply a HIGH level on the IRQ pin. The IRQ level is set to LOW level after reading the interrupt register. The MCU reads the interrupt register to distinguish between the different interrupt sources. The interrupt registers are reset automatically after reading.

8.4 Digital Interface

The interface is used for the serial communication between the Microcontroller and the AS3900.The maximum operation frequency of the Serial Data Interface (SDI) is 2MHz. The Interrupt Interface (IRQ) provides a CMOS compatible HIGH level at the occurrence of an interrupt. This level will be set to LOW if one of the interrupt registers is read. In active modes of the AS3900, a register selectable frequency is provided at the pin MCU_CLK. A typical connection to the MCU is shown in Figure 13

Figure 13. Microcontroller Interface



8.4.1 SDI Operation Mode Bits

In general there are 3 modes that can be selected by A7 and A6. A5 to A0 contains the register address of the selected register. D7 to D0 contain one byte that can be written or read from the selected address. A Write and Read cycle can be covered with 2 bytes, a Command cycle within 1 byte operation. An Enable LOW pulse indicates the end of all possible modes.

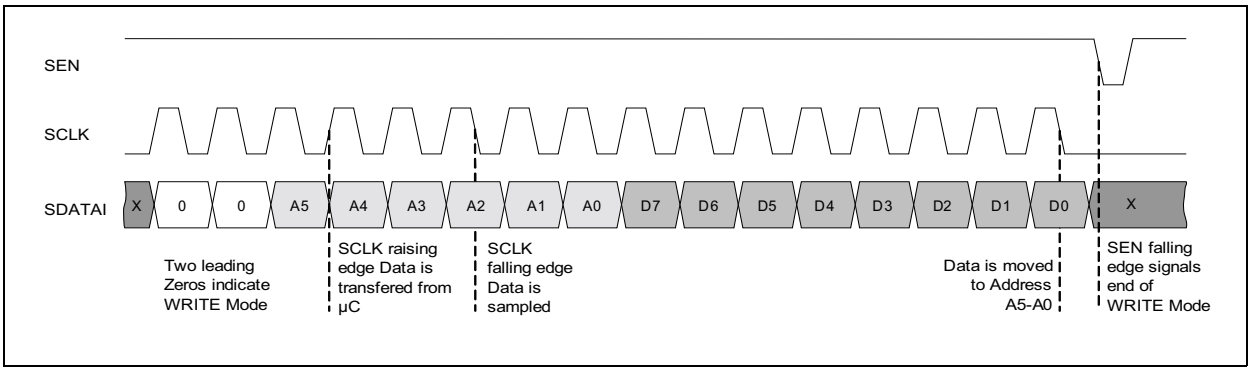
Table 14. SDI Operation Patterns

Mode	Mode Pattern								Mode related Data							
	Mode		Register Address						Register Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Mode	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Read Mode	0	1	x	x	x	x	x	x	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Spare Mode	1	0														
Command Mode	1	1	C5	C4	C3	C2	C1	C0								

8.4.2 Writing of Data to Addressable Registers (WRITE Mode)

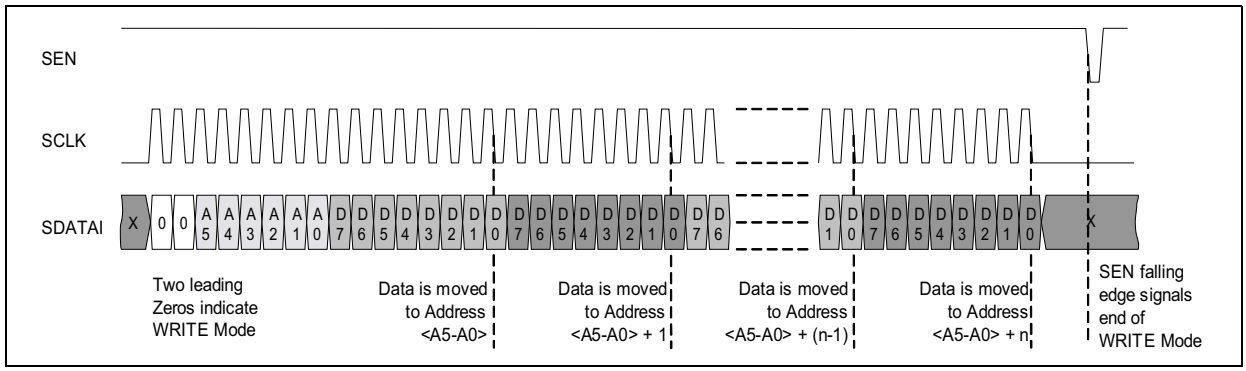
DATAI is sampled at the falling edge of SCLK as shown in the following diagrams. An Enable LOW pulse indicates the end of the WRITE command after register has been written. The following example shows a write command.

Figure 14. Writing of a Single Byte (falling edge sampling)



Due to the limited range of the Register Address of 6 bits (A5 to A0), only the register 0x00 to 0x3F are directly addressable. All other registers (0x3F to 0x51 in the MAIN register) can only be accessed via the auto-incrementing Write cycle. The auto-incrementing Write cycle can be applied by remaining SEN to HIGH and providing further clock cycles on SCLK (falling edges).

Figure 15. Writing of Register Data with Auto-incrementing Address



8.4.3 Reading of Data from Addressable Registers (READ Mode)

DATAI is sampled at the falling edge of SCLK, consequently, data to be read from the microcontroller are driven by the AS3900 (SDI slave) at the transfer edge and sampled by the microcontroller (SDI master) at the sampling edge of SCLK.

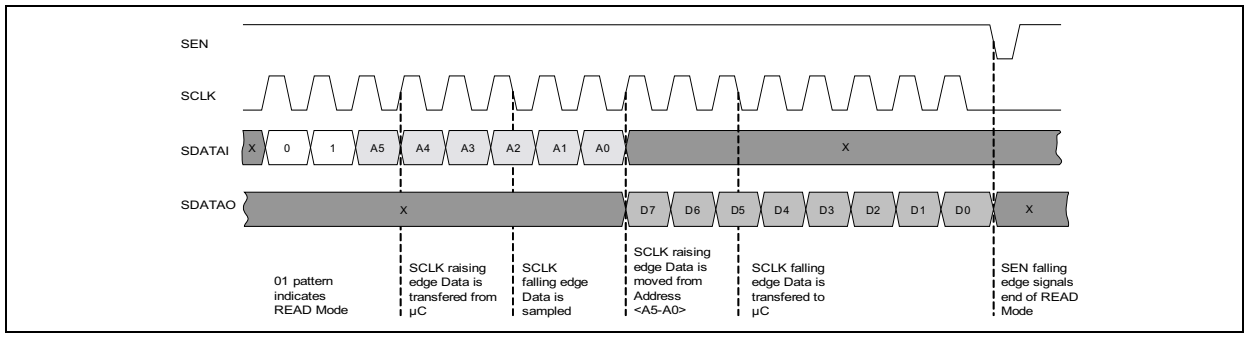
An Enable LOW pulse has to be performed after register data has been transferred in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

The command control Byte for a read command consists of a command code and an address. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SDI slave to the master, always from the MSB to the LSB. To transfer bytes from consecutive addresses, SDI master has to keep the SDI enable signal high and the SDI clock has to be active as long as data need to be read from the slave.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave samples it on the next SDI clock edge. Each bit of the data section of the frame has to be driven by the SDI slave on the SDI clock transfer edge and the SDI master on the next SDI clock edge samples it. If the read access is interrupted (by de-asserting the SDI enable signal), data provided to the master is consistent to given address, but it is only the register content from MSB to LSB. If more SDI clock cycles are provided, the data remains consistent and each data byte belongs to the given or incremented address.

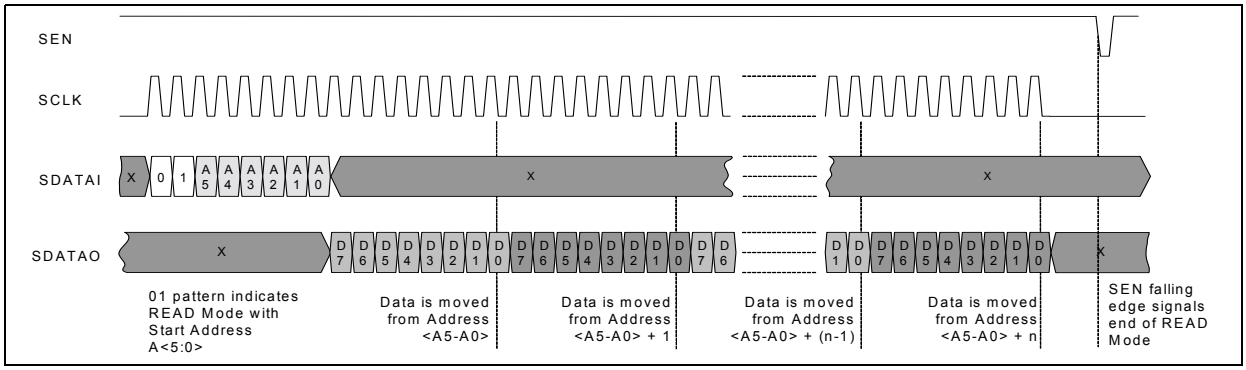
In the following figures two examples for a read command (without and with address self-increment) are given.

Figure 16. Reading of a Single Register Byte



Due to the limited range of the Register Address of 6 bits (A5 to A0) for reading a single Byte, only the register 0x00 to 0x3F are directly addressable. All other registers (0x3F to 0x51 in the MAIN register) can only be accessed via the auto-incrementing Read cycle. The auto-incrementing Read cycle can be applied by remaining SEN to HIGH and providing further clock cycles on SCLK (falling edges).

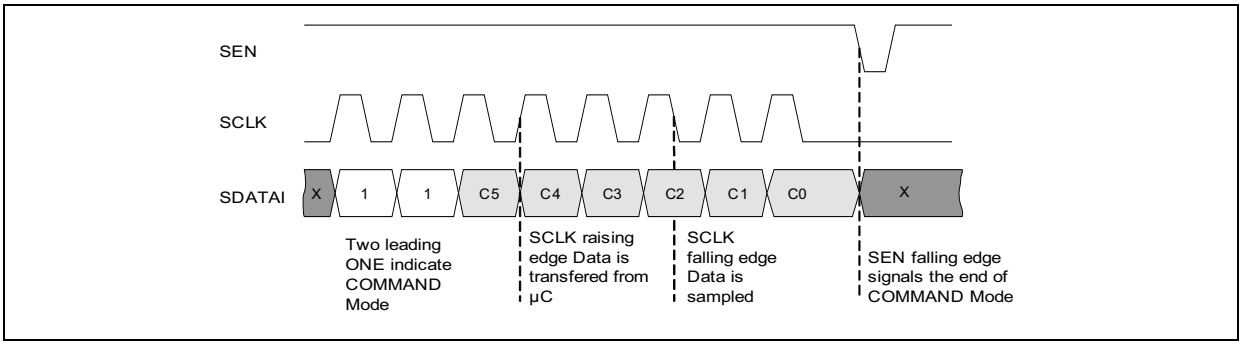
Figure 17. Reading of Register Data with Auto-incrementing Address



8.4.4 Send Single COMMAND byte

Command mode is entered if the SDI read is started with two leading ONE. After the COMMAND mode code (11), the further mode (e.g. DATA_TRANSMIT) could be provided from the MSB to the LSB or <C5-C0>. If <C5-C0> = 0 no mode change (used for Load Transmitting Data).

Figure 18. Single COMMAND byte



A full command to change the Operation Mode of the AS3900 has a length of only 8 bit followed by an SEN LOW pulse. The AS3900 offers the following direct commands.

Table 15. Direct Commands

Command Name	MODE Pattern (com. bits)						MODE Description
	C5	C4	C3	C2	C1	C0	
CHIP_RESET	0	0	0	0	0	0	Software reset, takes 2ms to load PROM
IRQ_CLEAR	0	0	0	0	0	1	Clear all interrupt registers
WAKE_TX	0	0	0	1	0	0	Starts the wake-up call sequence, composed of OOK
TRANSMIT	0	0	0	1	0	1	Initiates Tx sequence (depends on communication mode selected)
SCAN	0	0	0	1	1	0	Master enters Rx mode for 1s or longer, if 'longscan' bit is set
PROM_COPY	0	0	1	0	0	0	bank=1; copies the data from PPROM dprom registers REG 0x08 … 0x0A to register id0 in REG 0x08 … 0x0A
PROM_FUSE	0	0	1	0	0	1	bank=1, fuseen=1; starts the PPROM fuse procedure
PROM_LOAD	0	0	1	0	1	0	bank=1; load the fuse bits to PPROM registers
PROM_RST	0	0	1	0	1	1	bank=1; resets the PPROM modes
MAIN_BANK	0	1	0	0	0	0	Change selected bank to MAIN register
SHADOW_BANK	0	1	0	0	0	1	Change selected bank to SHADOW register
POWER_OFF	0	1	0	0	1	0	pwr bit off; clears all modes and stops timers; exceptions for bits osc32f, reff, osc27f
POWER_ON	0	1	0	0	1	1	pwr bit on
WAKE_RX_OFF	0	1	0	1	0	0	Wake_rx bit off
WAKE_RX_ON	0	1	0	1	0	1	Wake_rx bit on
STREAM_OFF	0	1	0	1	1	0	Stream bit off
STREAM_ON	0	1	0	1	1	1	Stream bit on
CLEAR_TIMER_0	1	0	0	0	0	0	Deactivate timing system 0
CLEAR_TIMER_1	1	0	0	0	0	1	Deactivate timing system 1
CLEAR_TIMER_2	1	0	0	0	1	0	Deactivate timing system 2
CLEAR_TIMER_3	1	0	0	0	1	1	Deactivate timing system 3
CLEAR_TIMER_4	1	0	0	1	0	0	Deactivate timing system 4

Table 15. Direct Commands

Command Name	MODE Pattern (com. bits)						MODE Description
	C5	C4	C3	C2	C1	C0	
CLEAR_TIMER_5	1	0	0	1	0	1	Deactivate timing system 5
CLEAR_TIMER_6	1	0	0	1	1	0	Deactivate timing system 6
CLEAR_TIMER_7	1	0	0	1	1	1	Deactivate timing system 7
CLEAR_TIMER_ALL	1	0	1	0	0	0	Deactivate all timing systems

8.4.5 Read Received Data

After successfully receive of the data the interrupt line is set.

- The microcontroller reads the interrupt register (with this read the IRQ line is reset).
- The microcontroller reads the ADDRESS (ID) to which sensor the data belongs.
- The microcontroller reads the DATALEN register.
- With this read the received DATA is transferred to the SDI output register and clocked out by means of the SDI Clock (SCLK).

8.4.6 Interrupt Interface Description

If an interrupt condition is met a HIGH level is applied to the IRQ pin. The IRQ level is set to LOW level after reading the Interrupt registers.

The microcontroller than reads the interrupt register to distinguish between different interrupt sources. The interrupt sources could be enabled or disabled by the use of the Interrupt Mask Registers. The Interrupt Mask Register defines which interrupt leads to a LOW to HIGH transition of the IRQ line.

Figure 19. Interrupt Operation

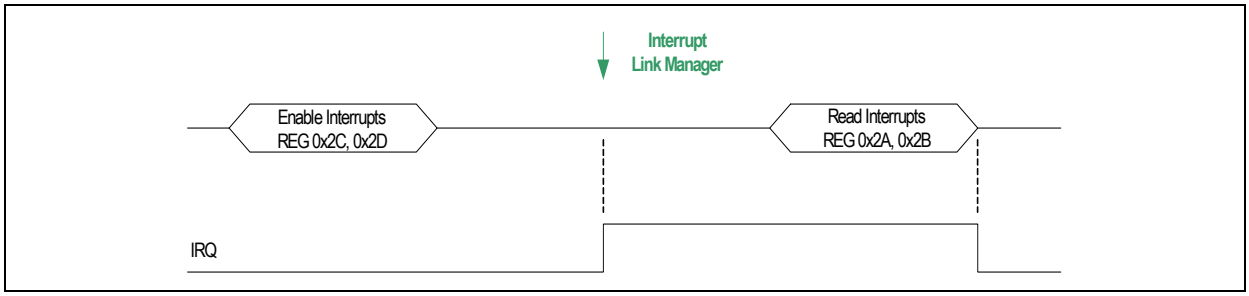


Table 16. Interrupt Electrical Interface Description

Name	Signal	Signal Level	Description
IRQ	Digital Output	CMOS	Interrupt Output pin (max Load = 10pF)

Table 17. Table of Interrupts

MAIN Reg. Addr#	Interrupt name	Int bits bit	Interrupt Description
0x2A	scan_end	[7]	One second scanning has been finished (if not enlarged with longscan bit)
	dat_rtx	[6]	Indicates that data was received and is ready to be read
	wake_call	[5]	For client to send transmit command
	stream_end	[4]	In client mode it indicates new data should be written into send register. In master mode it indicates end of transmission
	wrong_id	[3]	Activated if ID is not in the ID list
	wrong_crc	[2]	Activated if CRC error occurs
	timer_irq	[1]	Always activated if one of the irq<7:0>, REG 0x28<7:0> is activated
	Reserved	[0]	Reserved
0x2B	txend	[7]	Activated after last bit of CRC is transmitted
	txstart	[6]	Activated after last bit of PREAMBLE was transmitted
	rxend	[5]	Activated after the whole data was received
	rxstart	[4]	Activated after PREAMBLE was received
	nar_rtx	[3]	Activated after NAR was received or transmitted
	nak_rtx	[2]	Activated after NAK was received or transmitted
	acp_rtx	[1]	Activated after ACP was received or transmitted
	ack_rtx	[0]	Activated after ACK was received or transmitted

Table 18. Table of Interrupt Mask Registers

MAIN Reg. Addr#	Interrupt Mask name	Mask bits bit	Interrupt Mask Description
0x2C	msk_scan_end	[7]	Mask interrupt: scan_end
	msk_dat_rtx	[6]	Mask interrupt: dat_rtx
	msk_wake_call	[5]	Mask interrupt: wake_call
	msk_stream_end	[4]	Mask interrupt: stream_end
	msk_wrong_id	[3]	Mask interrupt: wrong_id
	msk_wrong_crc	[2]	Mask interrupt: wrong_crc
	msk_timer_irq	[1]	Mask interrupt: timer_irq
	Reserved	[0]	Reserved
0x2D	msk_txend	[7]	Mask interrupt: txend
	msk_txstart	[6]	Mask interrupt: txstart
	msk_rxend	[5]	Mask interrupt: rxend
	msk_rxstart	[4]	Mask interrupt: rxstart
	msk_nar_rtx	[3]	Mask interrupt: nar_rtx
	msk_nak_rtx	[2]	Mask interrupt: nak_rtx
	msk_acp_rtx	[1]	Mask interrupt: acp_rtx
	msk_ack_rtx	[0]	Mask interrupt: ack_rtx

Note: It is important to note that the enabling/disabling of the timers via REG 0x01<7:0> require a double readout of the interrupts REG 0x2A, 0x2B to release the IRQ line again.

8.4.7 Microcontroller Clock Interface

The output frequency is derived from the 27MHz crystal oscillator. The division ratio is defined by register settings. To enable or disable the clock output set the Clock Mode register bit. Additional different operation modes for the output could be set by Clock Mode register bits. For more information on the operation modes of the clock output see Table 20. Clock Interface Modes.

Table 19. Clock Interface Electrical Description

Name	Signal	Signal Level	Description
MCU_CLK	Buffered Digital Output	CMOS	Buffered slope controlled clock output Maximum Load = 50pF

Table 20. Clock Interface Modes

#	Mode	Mode (bit)		Clock Mode Description
		CM7	CM6	
1	MCUclk_Off	0	0	No clock is provided to pin MCU_CLK. Output Level is set to LOW.
2	MCUclk_32K	0	1	32kHz is always provided to pin MCU_CLK except in POWER DOWN Mode
3	MCUclk_27M	1	0	A division ratio of 27MHz is provided to pin MCU_CLK in all active modes except in SLEEP and POWER DOWN Mode. For division ratio (see Clock Division Ratios)
4	MCUclk_32K/27M	1	1	In active modes (RX or TX active) a division ratio of 27MHz is provided to pin MCU_CLK. In SLEEP Mode 32kHz is set. POWER DOWN Mode switches off the MCU_CLK output.

Table 21. Clock Division Ratios

Division ratio	Pattern (com. bits)				Mode Description
	mcdr[3]	mcdr[2]	mcdr[1]	mcdr[0]	Derived from 27.12MHz
8	0	0	0	0	3.39MHz
12	0	0	0	1	2.26MHz
12	0	0	1	0	2.26MHz
18	0	0	1	1	1.50MHz
16	0	1	0	0	1.69MHz
24	0	1	0	1	1.13MHz
24	0	1	1	0	1.13MHz
36	0	1	1	1	753kHz
32	1	0	0	0	847kHz
48	1	0	0	1	565kHz
48	1	0	1	0	565kHz
72	1	0	1	1	376kHz
64	1	1	0	0	423kHz
96	1	1	0	1	281kHz
96	1	1	1	0	281kHz
144	1	1	1	1	188kHz

8.5 Wakeup Procedure

In general the Wakeup is introduced in order to handle two different challenges:

- Wakeup Clients that are in Standby Mode. Clients in standby consume a small amount of power from the battery
- Exchange actual time code (Cycle time, random pointer) and synchronize all Clients with the Master

The Client (Master) is set to Wakeup receive mode for short time with a long wakeup interval. Master (Client) transmits long enough wakeup sequence to catch the receiving window of the Client (Master) or the Client is set to Wakeup receive mode for long time to catch the transmitted Master Wakeup sequences. If the Client (Master) receives a Wakeup sequence the link manager triggers the wake_call interrupt.

The Link Manager needs to be instructed via the direct **COMMANDS** and via **REGISTER** settings. The MCU is informed of the current status via **INTERRUPTS**, which need to be read out as soon as an external interrupt on the IRQ line appears.

8.5.1 Wakeup Receive Mode

The Wakeup Receive Window can be set to:

- Sampling: The Wakeup Receive Window is turned on for a fixed time of 250µs and turned off again for the remaining cycle time. The cycle time for the receive window can be set by the wakecyc bits in REG 0x04<2:4>. The ON interval itself is fixed to 250µs. The current consumption is defined by the ON to OFF ratio of the Wakeup receiver.

8.5.2 Wakeup Transmit Mode

Transmitting a Wakeup Signal means that the PA applies an OOK Signal (On Off Keying), in order to wakeup the Master (Client). The OOK pattern is a 27MHz signal that is ON OFF modulated with 96kHz. The following parameters for this OOK signal can be configured:

- Wakeup Transmitter On time: The Wakeup call can be applied between 125ms up to 1s in REG 0x04<1:0>.
- Longwake TX: The Wakeup call can be applied as long as the longwake_tx bit is set in REG 0x04<5>.

The Wakeup transmit mode shows a Wakeup procedure initialized by the Master. The Client samples for the Wakeup signal periodically. The figure shows the Wakeup procedure.

Figure 20. Wakeup Transmit Mode

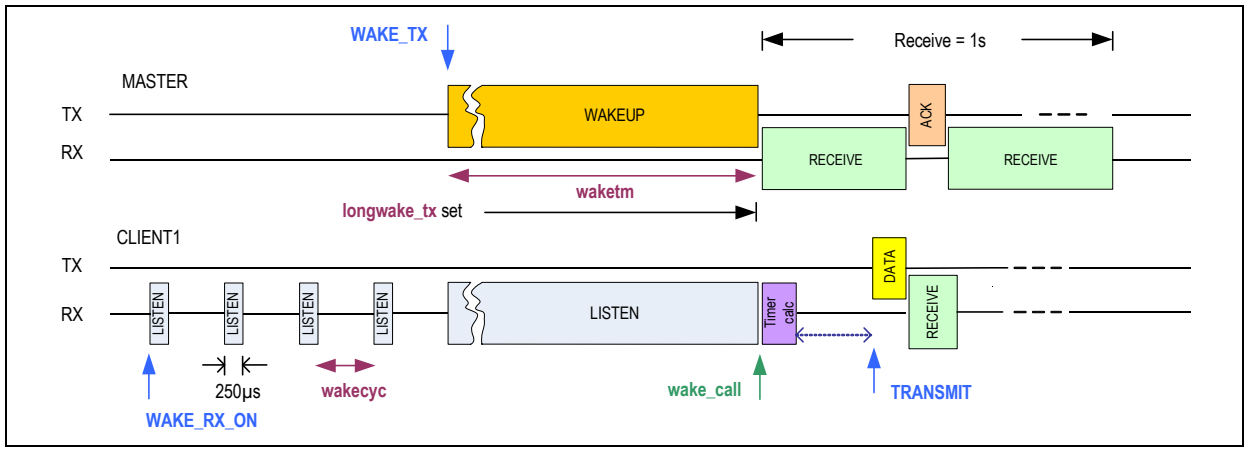


Table 22. Wakeup Procedure Initialized by the Master

Step	Master	Client
1		Client wakeup receiver listens during periodic time windows. This action is started by MCU with the command WAKE_RX_ON. The duration of wakeup listening is hardwired to 250µs and the wakeup listening cycle-time is defined by the wakecyc bits, REG 0x04<4:2>.
2	The Master starts the wakeup call with the command WAKE_TX The duration of the call is defined by the waketm bits, REG 0x04<1:0> (for MCU defined wakeup call duration the long wake_tx bit, REG 0x04<5> has to be used).	

Table 22. Wakeup Procedure Initialized by the Master

Step	Master	Client
3		If the wakeup receiver of the client detects a wakeup Signal (OOK pattern) the wakeup detection stays active as long as the OOK pattern is received. The wakeup detection mode is left after the OOK pattern goes low or the wakeup activity lasts for more than 3 wake cycle periods (happens if longwake_tx bit on master side is set). If the activity was terminated due to the reason that the wakeup signal is not received longer, the wake_call interrupt is set. The MCU on Client side has to calculate a random delay (less than 1sec).
4	When the wakeup call is finished the Master switches automatically the FSK receiver on for 1sec (the 1sec could be bypassed from the MCU by forcing the longscan bit REG 0x03<6> to HIGH). During this listening time, the Clients transmit randomly their first data. (if any of the Clients were already connected before, the timer based communication is suspended)	
5		After the delay time expires, the Client MCU loads data to dbuf register REG 0x38-0x51, data length to the dlen register REG 0x37<4:0> and starts the first transmission via the command TRANSMIT.
6	The received packets from different Clients contain a Preamble, the ID, Timing information (Cycle time and random pointer), data length, and data and CRC information. The exchange of the actual time code is terminated by an automatic acknowledgement (ACK).	

8.6 Pairing

8.6.1 Procedure

Pairing is a procedure where the Clients send their device IDs to the Master. The pairing procedure need to be started by the MCU. Common data-rate, frequency deviation and communication mode must be configured in the MAIN Register of all devices which have to be paired. After successful pairing, the device identification number is stored to the first free ID-table position at the Master and the pairing bit at the Client needs to be set.

The Pairing procedure is usually done permanently and initialized by the Master. The AS3900 is also able to provide the Pairing initialized by the Client and can also be just temporarily. The following table gives an overview about the provided Pairing features of the AS3900:

Table 23. Pairing Procedure

Pairing Procedures	Description
Client initiates permanent Pairing	Master is set to receive mode and listens during periodic time windows for a Wakeup Call from the Client. The Clients sends the Wakeup Call in order to wakeup the Master and transmits the first data packet. The Master wakes up and receive the first data packet that ID is checked. If the ID is not already in the ID-Table of the Master and the CRC is correct, the new ID will be inserted. After a handshake with the Client (acknowledgement), both nodes pass into Standby Mode again.

Table 23. Pairing Procedure

Pairing Procedures	Description
Master initiates permanent Pairing	Client is set to receive mode and listens during periodic time windows for a Wakeup Call form the Master. The Master transmits the Wakeup Call in order to wakeup the Clients. After the Wakeup and a random delay the Client starts the first transmission. The Master verifies the received Client ID and compares it to the existing IDs in the ID-table. If the ID is new and the CRC is correct, the ID is inserted. After a handshake with the Client (acknowledgement), both nodes pass into Standby Mode again.
Temporary Pairing	An existing network data transmission is already established. A second Master wants to listen to the data communication of a special Client. The second Master is set to receive mode and listens for Clients that are transmitting data. New IDs are added to the ID-table and the timing system is adopted (cycle time, bit rate …). The procedure is identical to “Master initiated Pairing” except that no Wakeup call and no handshake are done.

The following chapter describes the permanent Pairing that is initiated by the Master. All other pairing procedures are described in an appropriate application note.

Note: It is important that for the Pairing procedure all Timers need to be disabled. Set REG 0x02 to 0.

8.6.2 Master Initializes Pairing (wakeup) Procedure

Before any paring action could be started the MCU has to load the following configuration registers.

Table 24. Configuration Registers

Client / Master	Register Bits	Register	Register Bank	Comments
Client	wakecyc	0x04<4:2>	Main	Wakeup detection interval time
	wake_rx	0x00<2>	Main	Activates wakeup detection mode
Master	val_id	0x08… 0x1F	Main	List of allowed devices IDs to connect (or written via SDI after MCU decision)
	waketm	0x04<1:0>	Main	Wakeup call duration
Client	cyctim0	0x0C<7:5>	Shadow	Cycletime, period between two TX operations is only defined by the Client. To be synchronized to the Master this information is included in the data frame.
	rndpt0	0x0C<4:0>	Shadow	Random pointer of part of the period between two TX operations. Is only defined by the Client. To be synchronized to the Master this information is included in the data frame.
	TX_data	0x08… 0x1F	Main	Data in TX register will be appended to the ID and cycle time information. Client payload data can be any information
Master/Client	bitrate	0x06<1:0>	Main	Defines data rate for the communication, need to be the same for Master and Client

The Pairing Master shows the pairing procedure that is initialized by the Master. The Sensors (=Clients) are set into receive mode. The Master transmits a Wakeup Signal (OOK-Pattern) for one second. Afterwards the Sensors are activated and send after a random time a data frame with 5 bytes payload to tell the Master its ID. The random time is usually derived from the fixed programmed ID and calculated by the MCU of the Sensor. The Master switches to receive mode after sending the Wakeup Signal, in order to listen for Sensor data. If data from a Client is received, the ID is stored into the ID-Table (applied by the MCU of the Master). The Master sends a SYNC frame and waits for an acknowledgement (ACKN). The Master RX stays on and waits for the next Sensor data. If all Sensors are permanently paired all nodes switch to Standby Mode again.

The following sequence explains the operations that need to be done by the MCU at the Master and Client.

Figure 21. Pairing Master

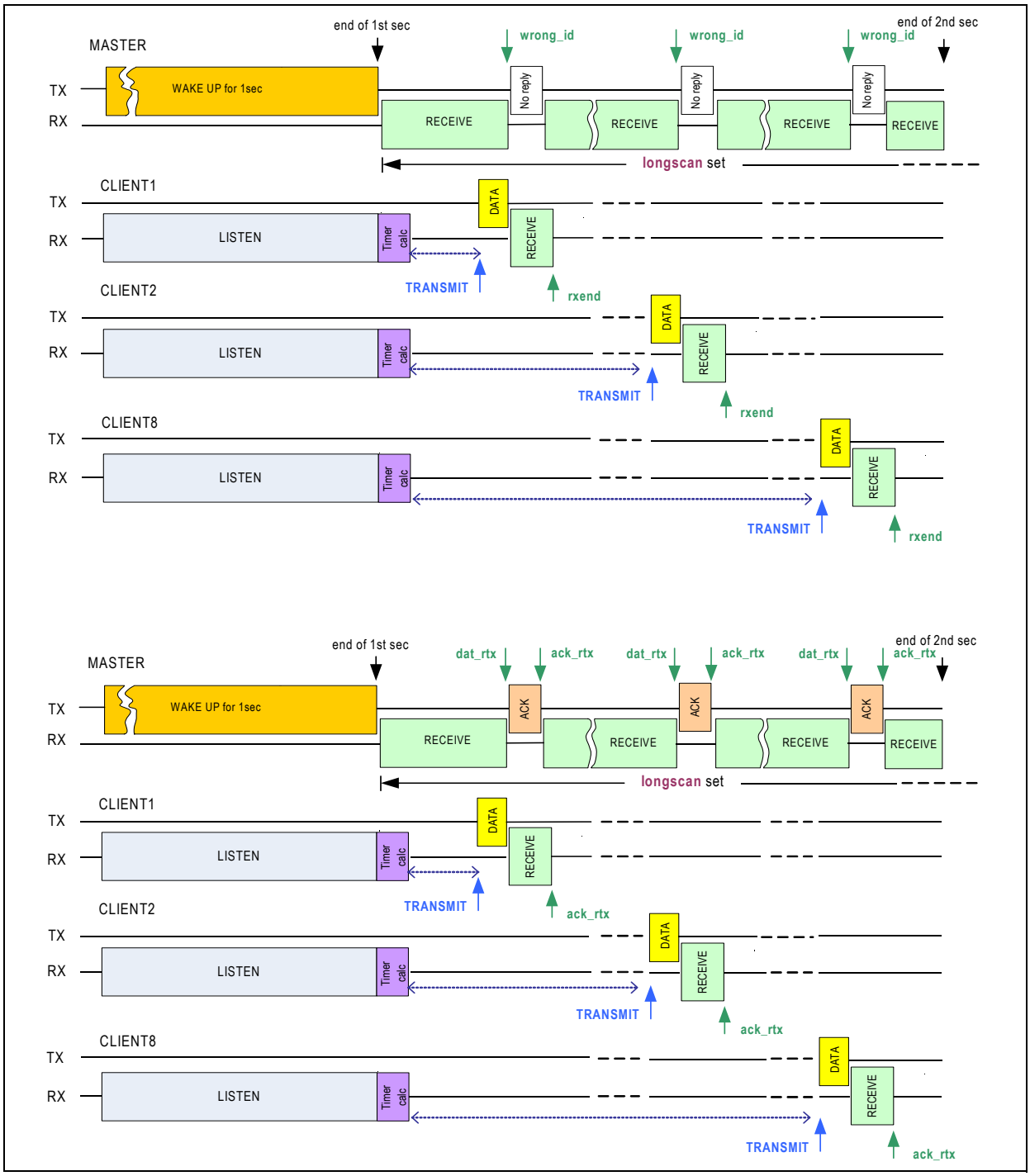


Table 25. Pairing Communication

Step	Master	Client
1	All Timers are disabled at the Master via the REG 0x01<7:0>. The Master starts the Wakeup procedure as described. When the wakeup call is finished the Master switches automatically the FSK receiver on for 1sec. During this listening time, the Clients transmit randomly their first data.	
2		After the MCU defined delay time expires, the Client starts the first transmission via the command TRANSMIT.
3a	Master verifies the received client ID by comparing it to its ID list REG 0x08-0x1F. If the ID was found, the internal timing system for this Client is updated (immediately after the ID is received) with the cycl_time and random pointer rndpt, received from the Client. If the CRC is correct, the ACK is sent back to signal the Client that it has been accepted. Interrupt dat_rtx is set and the MCU could read the data.	
4a		After the data is transmitted, the Client enters the receive mode for a dedicated time waiting for the ACK pattern. If ACK was received the interrupt ack_rtx is generated and the transmit command is terminated. Client goes to Standby Mode until the next wakeup cycle event, because all timers are disabled for the pairing procedure.
3b	If the received ID is correct but CRC error occurs, no ACK will be sent and the timer for this client is not started because no information for cycle time and RNG-pointer is available.	
3c	If the received ID can not be found in ID list REG 0x08 to 0x1F and the reception was successful (CRC is O.K.) the interrupt wrong_id is set, but no ACK is sent to the client. The MCU reads the ID from the id_new register REG 0x34 to 0x36. If the ID is confirmed (by MCU) then the MCU writes the new ID via SDI to the ID list REG 0x08 to 0x1F and the Client is accepted at the next wake up call.	
3d	If the received ID is not confirmed by the MCU, no ACK is sent to the Client even if the Client tries to connect again.	
3e	If the received ID belongs to a client that has already an activated data transmission, nothing is changed.	
4bcde		If the client do not receive an ACK (within the dedicated time slot), the transmit command is not terminated. If no ACK is received the receiver is switched of and the interrupt rxend is generated. The Client MCU can then repeat the TRANSMIT command after a certain delay.

8.7 Transmission Modes

After the successful Pairing procedure, the ID-table of the Master REG 0x08 to 0x1F is filled with valid addresses of different Clients in the surrounding field. All participants of the network are determined after the pairing procedure.

The transmission is usually accomplished time division multiplexed (timer controlled) via the packet mode. Packets can be send bidirectional from the 8 possible Clients to the Master. The AS3900 is also able to provide a not timer controlled bidirectional fast package mode, a timer controlled one way package mode and a not timer controlled one way streaming mode. The following table gives an overview about the provided transmission modes of the AS3900:

Table 26. Transmission Modes

Transmission Modes	Direction	Method	Description
Packet mode	Bidirectional	Timer controlled	Eight possible Clients start to transmit a packet synchronously to the applied timing information. The Master has stored the timing information for each Client that wakes up the FSK receiver from Sleep mode at certain point of times. This mode is very efficient and power saving. Incoming packages are checked for a valid ID and the data is loaded into the data registers. The communication is terminated by a handshake. The Master can add to each acknowledgement 4 bytes of data for the Client (ACP).
Packet mode	One way	Timer controlled	Only one Client starts to transmit a packet that contains the ID and the timing information (cycle time, random pointer).The Master opens the receive window according to the stored timing system and compares the IDs. A synchronization of the timers is performed and the incoming data is loaded into the data registers which can be read out by the MCU.
Fast packet mode	Bidirectional	Not Timer controlled	Only one Client starts to transmit a packet asynchronously. The Master is in permanent receive mode and waits for incoming packages. After comparison of the ID with the ID-table the incoming data is loaded into the data registers. The communication is usually terminated by an acknowledgement (ACK). The Master can add to each acknowledgement 4 bytes of data for the Client (ACP).
Streaming mode	One way	Not Timer controlled	Only one Client is allowed for this operation, which ID is stored in the Masters ID-table. The Client starts to transmit the maximum number of data packets (26 bytes) asynchronously. The Master is in continuous receive mode, ready to receive all packets.

The different transmission modes can be set by an appropriate configuration in REG 0x00:

Table 27. Selection Transmission Modes

		7	6	5	4	3	2	1	0
		ma_sen	osc32f	timdis	unidir	stream	wake_rx	pwr	bank
Bidirectional Packet Mode	0x00	x	x	0	0	0	x	1	x
One Way Packet Mode		x	x	0	1	0	x	1	x
Fast Packet Mode		x	x	1	0	0	x	1	x
Streaming Mode		x	x	1	1	1	x	1	x

The following chapter describes the bidirectional packet mode that is timer controlled. All other transmission modes listed above are described in an appropriate application note.

8.7.1 Packet mode – Bidirectional – Timer Controlled

Figure 22. Acknowledgement

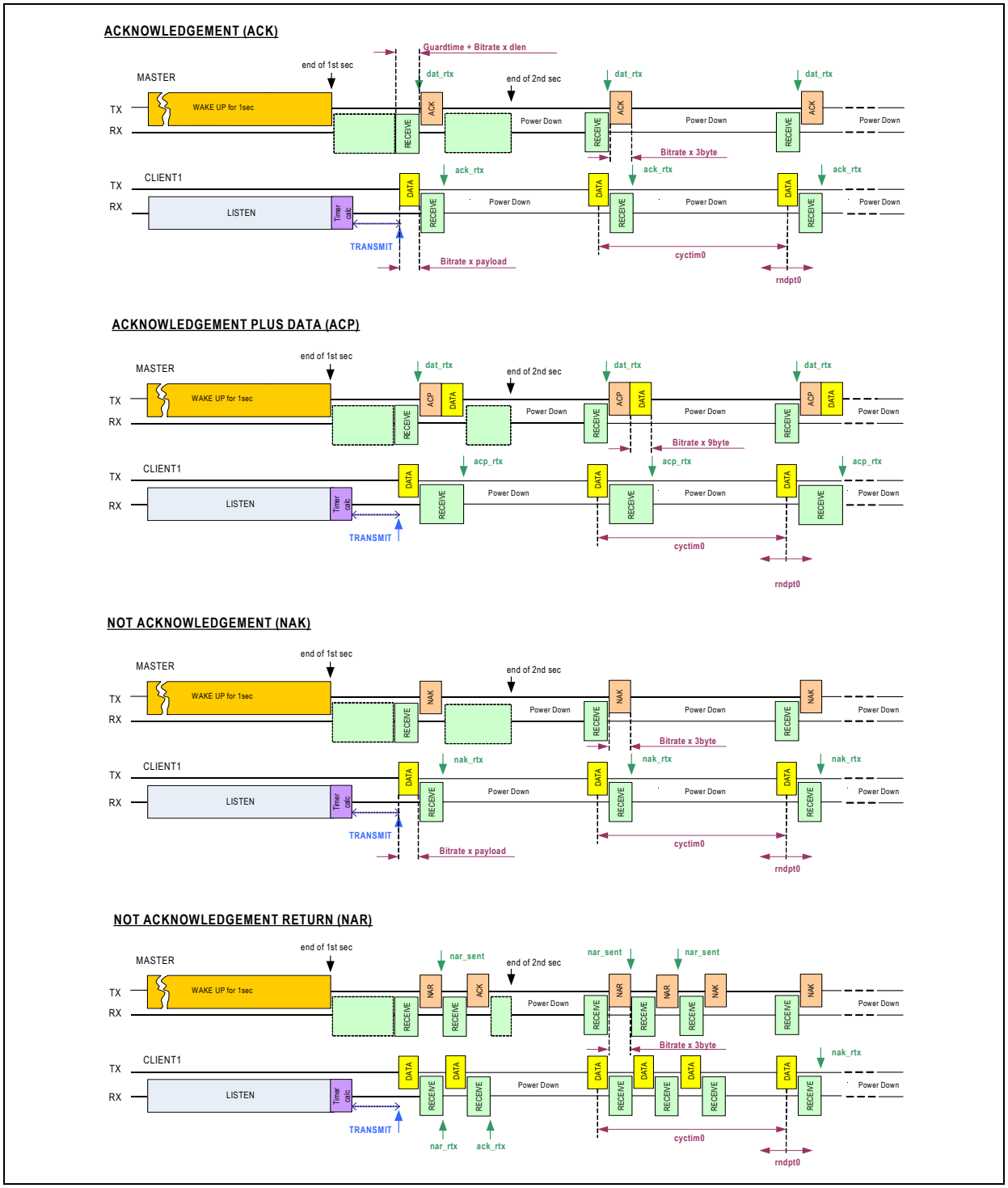


Table 28. Communication

Step	Master	Client
1	All Timers are enabled at the Master via the REG 0x01<7:0>. The Master starts the Wakeup procedure as described in chapter 11.4. When the wakeup call is finished the Master switches automatically the FSK receiver on for 1sec. During this listening time, the Clients transmit randomly their first data. With the first data all timing information is exchanged and stored in the master's timing table in SREG 0x0C to 0x13.	
2		The Client timer is enabled via the REG 0x01<0>. MCU writes the data into the dbuf register REG 0x38 to 0x51 and the payload data length to the dlen register REG 0x37<4:0> via SDI. This has to be performed in the time window between the finish of the last communication and before next.
3		The enabled timer starts the transmit sequence and the interrupt txstart is set. When the ID is transmitted (at the start of transmit) the synchronization pulse is sent to the timing unit to start the new time interval (cycle time)
4	The timing system, dedicated to each client in the master's timing table, wakes up the FSK receiver from the Sleep Mode before the expected receive time expires (with guard time, all timer interrupts are active). The guard time depends on the previous history of communication and is adjusted automatically. The receive window is defined by the dedicated bitrate and the payload data length dlen.	
5a ACK	Master receives the data from the client; after the ID is received it is compared with the ID of the expected client (defined ID and timing unit). If the ID is matching the synchronization pulse is given to the timing block to perform the timing synchronization. The ID is shifted to the id_new registers REG 0x34 to 0x36, data length is stored in the dlen bits, REG 0x37<4:0> and data is shifted to the dbuf register, REG 0x38 to 0x51. At the end of the data packet the interrupt dat_rtx is generated. One 32kHz clock cycle after the final data is received the master is switched from the receive mode to the transmit mode in order to start an ACK transmission. After the end of ACK transmission the system is powered down (only timer units running). The communication error counter (cesX) for the according Client is cleared.	
6a ACK		One 32kHz clock cycle after end of the data transmission the Client switches to receive mode awaiting ACK. The wait duration is defined by the datarate. After ACK is received the interrupt ack_rtx is set and the IC is powered down. The next data communication is started automatically with the next timer iteration. The communication runs until the timer0 is cleared via the command CLEAR_TIMER0. The communication error counter (ces0) is cleared

Table 28. Communication

Step	Master	Client
5b ACP	Same as 5a, but in case the acp2 bit, REG 0x33<7> is set, data transmission from the Master to the Clients is possible. The address of the Client can be selected by the sid2<2:0> bits in REG 0x33<6:4> that corresponds to the timing unit (0-7) which has triggered the receive action. The ACP code is sent with the appended 32 bit data from register dabuf in REG 0x2F to 0x32. The communication error counter (cesX) for the according Client is cleared.	
6b ACP		Same as 6a, but if the ACP is received, the data followed by the ACP code is routed to dabuf register in REG 0x2F to 0x32 and the interrupt acp_rtx is set (IRQ activated). The MCU can read the 32 bit ACP data from register dabuf and decide what to do with. The communication error counter (ces0) is cleared.
5c NAK	If the received Client ID is incorrect and/or the CRC is wrong no dat_rtx interrupt is generated. The Master switches to transmit mode and sends NAK (not-acknowledge), if the number of narmax in REG 0x03<1:0> is set to 0 the interrupt nak_rtx is set. The communication error counter cesX in REG 0x14 to 0x17 is increased for the according Client. If one Client exceeds the limit of the communication error counter cesmax in REG 0x02<2:0>, the affected timer is turned off in REG 0x01.	
6c NAK or Error		Same as 6a, if NAK is received, nak_rtx interrupt is generated (IRQ.is set). The communication error counter ces0 is increased for this Client in REG 0x14<2:0>. Also in case there is response but data can not be identified it is handled as NAK and the communication error counter ces0 is increased.
5d NAR	If the Client ID matches with the expected ID the synchronization pulse is sent to the related timer unit, but if the CRC is wrong no dat_rtx interrupt is generated. The Master switches to transmit mode and sends NAR (not-acknowledge with re-transmit request), if the number of NAR (re-transmits) is set to a non-zero value in register bits narmax in REG 0x03<1:0>. The nar_sent interrupt is generated for the MCU. The cesX counter is not changed. The Master switches back to receive mode and waits for data retransmission from the same Client.	
6d NAR		Same as 6a, if NAR is received and narmax in REG 0x03<1:0> is nonzero, a nar_rtx interrupt is generated, afterwards the transmit mode is switched on and the old data is retransmitted. If narmax = 0 the interrupt nar_rtx is generated but no retransmit is initiated.
5d, 6d NAR-Repeat NAK	During the retransmit the timer is not re synchronized (initial synchronization is not changed due to re-transmit). If the receive is successful ACK is sent. If there is CRC error NAR is sent, if the number of consecutive retransmits does not exceed the value in the narmax register. If this number is exceeded, NAK is send instead of NAR and the communication error counter cesX is increased for the affected Client.	During the retransmit the timer is not re-synchronized (initial synchronization is not changed due to retransmit). If the transmission was successfully, ACK will be received and the current data transmission is terminated (as in point 6a). If there was a CRC error and narmax is not exceeded yet, another retransmit cycle is started. If NAK is received the communication error counter ces0 is increased

Table 28. Communication

Step	Master	Client
5e no reply	If there is no successful reception, even no matching ID could be identified, the Master does not re-synchronize the timer and no reply will be send to the client. The communication error cesX is increased and the guard time is increased due to the not successful synchronization. The guard time is defined by the bits pretm in REG 0x02<7:5>. No reply also occurs in the retransmit mode, if the ID is not identified as known.	
6e no reply		The Client is waiting for any reply, but after the dedicated time (datarate x 3byte) the receive mode is terminated and the communication error counter ces0 is increased, due to no reply.

8.7.2 Scan Procedure

Another possibility to exchange or update the actual time codes (Cycle time, random pointer) of the Clients are the scan modes. A typical application of these scan modes are Clients that are taken out of range and want to be reconnected again.

The scan modes allow the Master to listen for incoming signals by opening the receive window of the LNA for a certain time. Two scan modes can be applied:

- Scan: The LNA Receive Window is turned on for 1s. The device is in receive-mode and consumes 2.2mA supply current. The 1s scan can be applied by the direct command SCAN.
- Long scan: The LNA Receive Window is turned on as long as the longscan bit is set in REG 0x03<6>. The device is in receive-mode and consumes 2.2mA supply current.

Figure 23. Reconnecting Client / Updating Actual Time Base

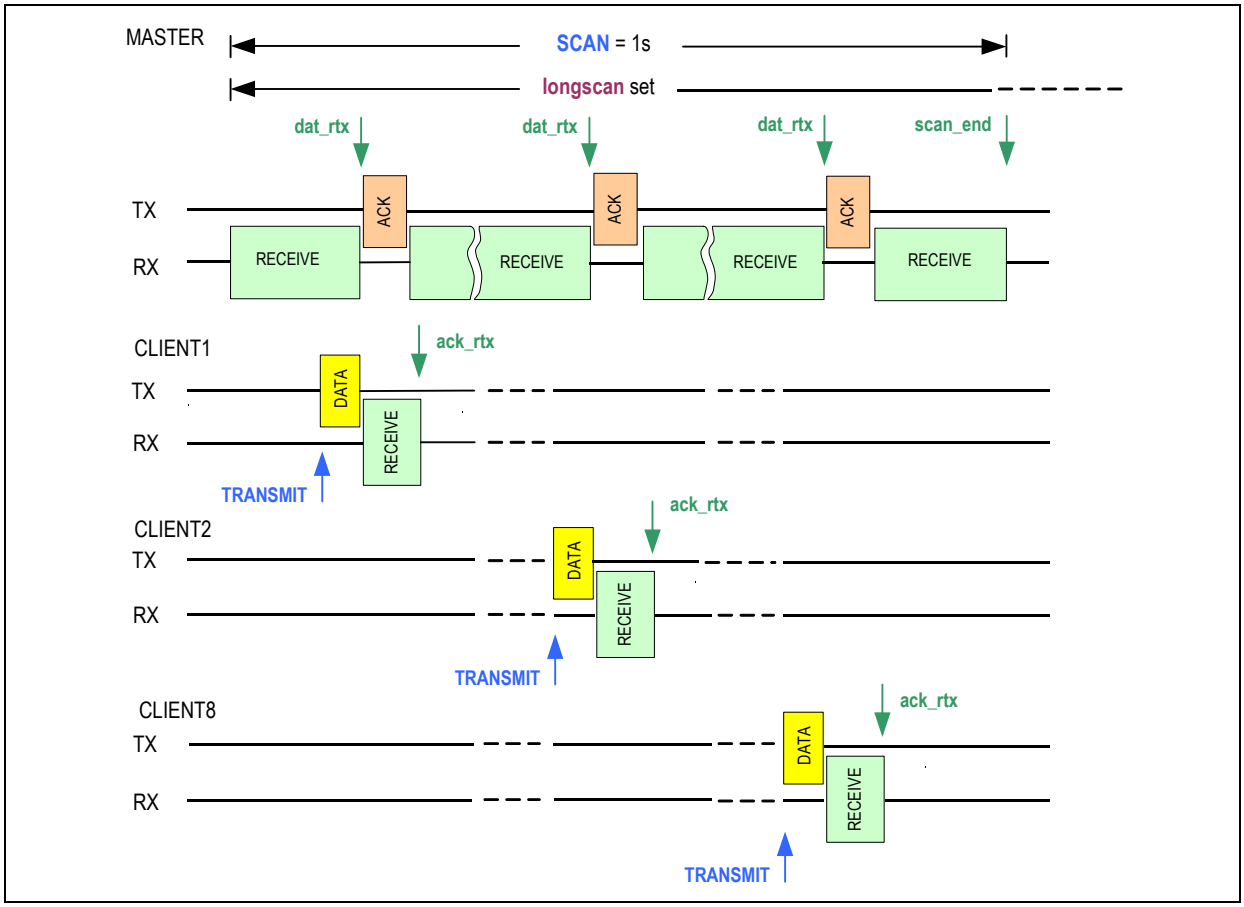


Figure 24. Pairing Clients via Longscan

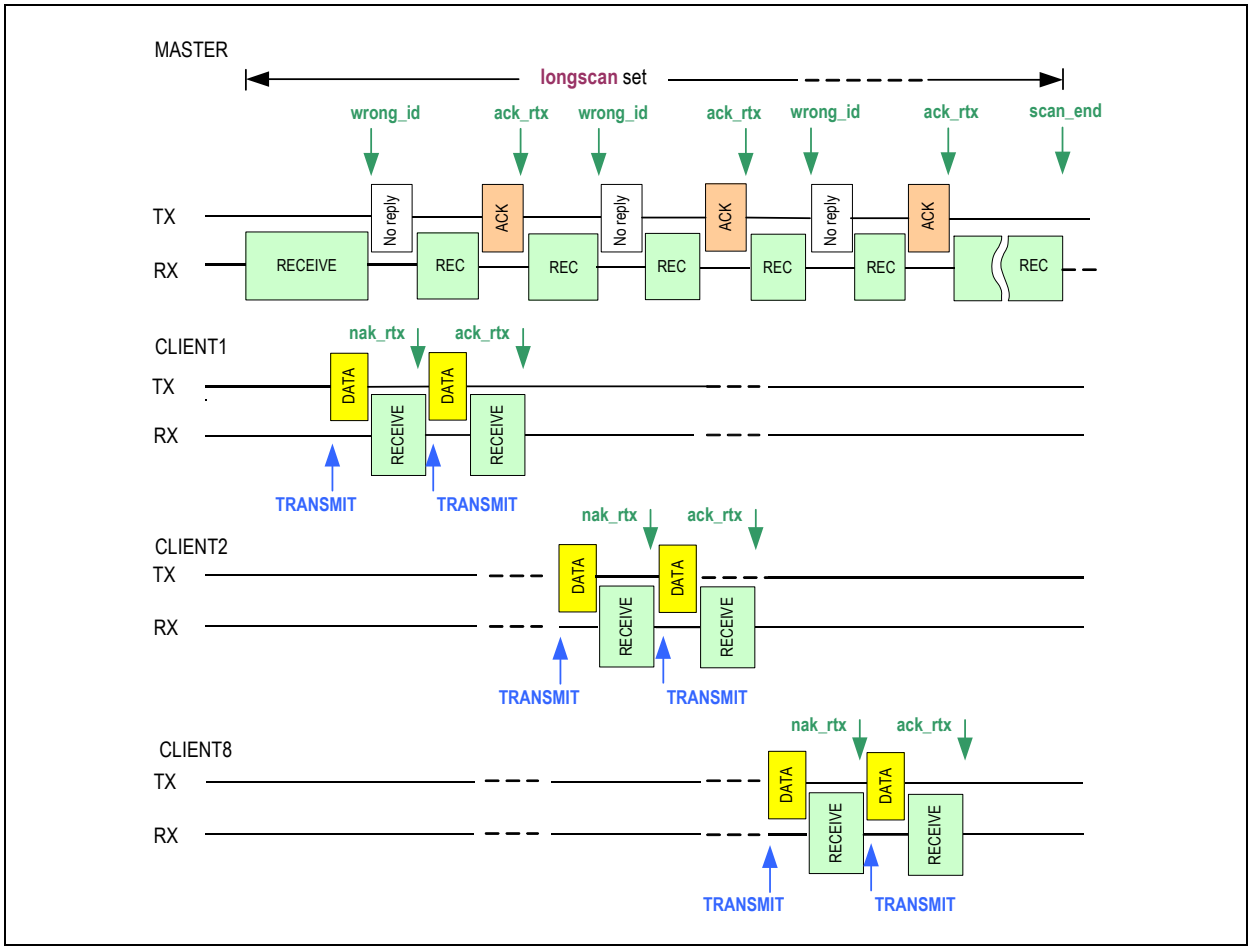


Table 29. Scan / Reconnect / Pair Clients

Step	Master	Client
1	The Master opens the LNA Receive Window for 1s via the command SCAN. This Window can be prolonged by setting bit longscan in REG 0x03<6>. The timers for the Clients need to be enabled via the REG 0x01<7:0>.	
2		The Client timer is enabled via the REG 0x01<0> and continuously send packets based on its time base. The communication error counter need to be disabled, otherwise the Client timer would stop. The Client transmit one packet via the command TRANSMIT.
3a	Master verifies the received client ID by comparing it to its ID list REG 0x08-0x1F. If the ID was found, the internal timing system for this Client is started (immediately after the ID is received) with the cycl_time and random pointer rndpt, received from the Client. If the CRC is correct, the ACK is sent back to signal the Client that it has been accepted. Interrupt dat_rtx is set and the MCU could read the data.	
4a		After the data is transmitted the Client enters the receive mode for the dedicated time (datarate x 3byte). If ACK was received the interrupt ack_rtx is generated and the transmit command is terminated.

Table 29. Scan / Reconnect / Pair Clients

Step	Master	Client
3b	If the received ID can not be found in ID list REG 0x08 to 0x1F and the reception was successful (CRC is O.K.) the interrupt dat_rtx is set, but no ACK is sent to the client. The MCU reads the ID from the id_new register REG 0x34 to 0x36. If the ID is confirmed (by MCU) then the MCU writes the new ID via SDI to the ID list REG 0x08 to 0x1F.	
4b		After the data is transmitted the Client enters the receive mode for the dedicated time (datarate x 3byte). If ACK was not received the interrupt ack_rtx is not generated. The Client transmit again data via the command TRANSMIT. The procedure is repeated at Step 2.

8.8 Data Frames

8.8.1 Frame Structure for Timer Controlled Packet Mode

This Frame structure is always used during Pairing and Binding Modes. The maximum data length is 24 bytes and has to be reflected in the data length value given in the data length byte. ID, Cycle time and Random Generator Pointer are user defined.

Table 30. Frame Structure

Preamble	ID	Cycle-time/ RGN-pointer	data length	data	CRC
MSB	→ data transmission direction →				LSB
16 bits	24 bits	4 + 4bits	8 bits	data from TX register maximum 192 bits	16 bits

Table 31. Frame Structure Description

Name	Length (bytes)	Value (Hex)	Register
Preamble	2 bytes	0x0017	not accessible
ID	3 bytes	user defined (PPROM programmable)	Main Register Bank REG 0x08, 0x09, 0x0A
Cycle time	4 bits	user defined; taken from the register in the client chip	Shadow Register Bank, SREG 0x0C<7:5>
RNG pointer	4 bits	user defined; taken from the register in the client chip	Shadow Register Bank, SREG 0x0C<4:0>
Data length	5 bits	user defined	Main Bank REG 0x37<4:0>
Status Bits	3 bits	user defined	Main Bank REG 0x37<7:5>
Payload data	0 – 24 bytes	user defined	REG 0x38 (MSB) to REG 0x51 (LSB)
CRC (CRC16)	2 bytes	calculated from payload data	Not accessible

The frame structure for all other transmission modes (streaming mode, not timer controlled modes etc.) are different and are described in the appropriate application notes.

8.8.2 Frame Structure for ACKNOWLEDGE (ACK)

After data was received successfully (correct ID and no CRC error) ACK will be send.

Table 32. Frame Structure

Preamble	ACK
16 bits	8bits

8.8.3 Frame structure for ACKNOWLEDGE with appended data (ACP)

This mode is used to send 4 bytes data (REG 0x2F, 0x30, 0x31, 0x32) from the Master to the Client. The transmission only takes place if the data in these data registers is nonzero. The received data is stored in the same Client registers REG 0x2F, 0x30, 0x31, 0x32 and could be read by the MCU.

After data was received successfully (correct ID and no CRC error) by the Master ACP will be send else NAK or NAP are send.

Table 33. Frame Structure

Preamble	ACP	data	CRC
16 bits	8bits	32 bits (REG 0x2F, 0x30, 0x31, 0x32)	16 bits

8.8.4 Frame Structure for NOT-ACKNOWLEDGE (NAK)

After any data error at reception time window (incorrect ID and / or CRC error) NAK will be send.

Communication error counter will be increased. Communication will be terminated after communication error counter limit cesmax in REG 0x02<2:0> will be exceeded. The cesmax at the Master is the limit for all available Clients. The actual communication error count of each Client is stored in SREG 0x14 to 0x17. If different communication error limits are requested for the different Clients, it is possible to offset the cesX value for the separate Clients in SREG 0x14 to 0x17.

Table 34. Frame Structure

Preamble	NAK
16 bits	8bits

8.8.5 Frame Structure for NOT-ACKNOWLEDGE and Data Retransmit (NAR)

After a CRC data error at reception time window (correct ID and CRC error) NAR will be send.

NAR error counter in REG 0x03<1:0> will be increased. After NAR error counter exceeds the maximum, NAK will be send and the Communication counter is increased. After the client receives NAR, immediately the data is retransmitted and the client NAR error counter will be increased.

Table 35. Frame Structure

Preamble	NAR
16 bits	8bits

8.9 Configuration Registers

All configuration registers are readable and writable. The registers are arranged as addressable bytes. The configuration register settings do not alter during Power down mode as long as the minimum supply voltage requirements are met. The bank bit at ADDRESS 0x00 bit<0> defines the Main (bit value = 0) or the Shadow (bit value = 1) Register Bank.

8.9.1 Main Register Bank (ADDRESS 0x00 bit<0>=0)

Table 36. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Register Address	7	6	5	4	3	2	1	0
0x00	ma_sen	osc32f	timdis	unidir	stream	wake_rx	pwr	bank
0x01	entm<7:0>							
0x02	pretm<2:0>			reserved		cesmax<2:0>		
0x03	reserved	longscan	reserved	osc27f	reserved		narmax<1:0>	
0x04	fuseen	reserved	longwake_tx	wakecyc<2:0>			waketm<1:0>	
0x05	mcs<1:0>		reserved		mcdr<3>			
0x06	reserved					dev<2>	bitrate<1:0>	

Table 36. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Register Address	7	6	5	4	3	2	1	0
0x07	lowbatsel_tx	lowbatval_tx	reserved					
0x08 - 0x0A	id0<23:0>							
0x0B - 0x0D	id1<23:0>							
0x0E - 0x10	id2<23:0>							
0x11 - 0x13	id3<23:0>							
0x14 - 0x16	id4<23:0>							
0x17 - 0x19	id5<23:0>							
0x1A - 0x1C	id6<23:0>							
0x1D - 0x1F	id7<23:16>							
0x20	reserved				rssi_on	reserved		
0x21	reserved			bat<1:0>		singl	half	fzero
0x22	reserved							
0x23	tx_en	Lbat_ok	reserved		rssi<3:0>			
0x24 - 0x26	reserved							
0x27	active<7:0>							
0x28	irq<7:0>							
0x29	reserved							
0x2A	scan_end	dat_rtx	wake_call	stream_end	wrong_id	wrong_crc	timer_irq	reserved
0x2B	txend	txstart	rxend	rxstart	nar_rtx	nak_rtx	acp_rtx	ack_rtx
0x2C	msk_scan_end	msk_dat_rtx	msk_wake_call	msk_stream_end	msk_wrong_id	msk_wrong_crc	msk_timer_irq	msk_timer_stpd
0x2D	msk_txend	msk_txstart	msk_rxend	msk_rxstart	msk_nar_rtx	msk_nak_rtx	msk_acp_rtx	msk_ack_rtx
0x2E	reserved							
0x2F - 0x32	dabuf<31:0>							
0x33	acp2	sid2<2:0>			iit	sid<2:0>		
0x34 - 0x36	idnew<23:0>							
0x37	user_status2	user_status1	user_status0	dlen<4:0>				
0x38 - 0x51	dbuf<207:0>							

8.9.2 Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Table 37. Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Register Address	7	6	5	4	3	2	1	0
0x08 - 0x0A	dprom<23:0>							
0x0B	reserved							
0x0C	cyctim0<2:0>			rndpt0<4:0>				
0x0D	cyctim1<2:0>			rndpt1<4:0>				
0x0E	cyctim2<2:0>			rndpt2<4:0>				
0x0F	cyctim3<2:0>			rndpt3<4:0>				
0x10	cyctim4<2:0>			rndpt4<4:0>				
0x11	cyctim5<2:0>			rndpt5<4:0>				
0x12	cyctim6<2:0>			rndpt6<4:0>				
0x13	cyctim7<2:0>			rndpt7<4:0>				
0x14	reserved	ces1<2:0>			reserved	ces0<2:0>		
0x15	reserved	ces3<2:0>			reserved	ces2<2:0>		
0x16	reserved	ces5<2:0>			reserved	ces4<2:0>		
0x17	reserved	ces7<2:0>			reserved	ces6<2:0>		
0x18 - 0x1D	reserved							

8.9.3 Detailed Description

The complete register map is divided into 2 maps. The MAIN register consists of 82 bytes and the SHADOW register of 22 register. The MAIN register can be accessed by clearing the bank bit in REG 0x00<0> or via the direct command MAIN_BANK. The SHADOW register can be accessed by setting the bank bit in REG 0x00<0> or via the direct command SHADOW_BANK. All bytes are readable and writable via the SDI interface in Client and Master mode.

Note: It is important to note, that the REG 0x3F to 0x51 in the MAIN register are only accessible by auto-incrementing the address. All other registers are directly addressable.

8.9.3.1 Main Register Bank (ADDRESS 0x00 bit<0>=0)

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
Control Register section					
0x00	ma_sen	[7]	R/W	Master / Client selector	
				0	Client
				1	Master
	osc_32	[6]		Enable for 32kHz oscillator manually	
				0	Disabled
				1	Enabled
	timdis	[5]		Timer disable	
				0	Enabled
				1	Disabled
	unidir	[4]		Select unidirectional transceiver mode	
				0	Bidirectional
				1	Unidirectional
	stream	[3]		Stream mode control	
				0	Disabled
				1	Enabled
	wake_rx	[2]		Wakeup receiver enable	
				0	Disabled
				1	Enabled
	pwr	[1]		Power enable	
				0	OFF
				1	ON
	bank	[0]		Bank selection bit	
				0	Main Bank selected
				1	Shadow Bank selected

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x01	entm	[7:0]	R/W	Timer enable bits for Master and Client	
				In Master mode: 8 Client timers	
				00000001	Enable Timer for Client 0
				00000010	Enable Timer for Client 1
				00000100	Enable Timer for Client 2
				00001000	Enable Timer for Client 3
				00010000	Enable Timer for Client 4
				00100000	Enable Timer for Client 5
				01000000	Enable Timer for Client 6
				10000000	Enable Timer for Client 7
				11111111	Enable all Timers
				In Client mode: 1st timer is Client timer	
				00000000	Disabled
				00000001	Enabled
0x02	pretm<2:0>	[7:5]	R/W	NAR operation mode; guard times for master timer	
	reserved	[4:3]		reserved	
	cesmax<2:0>	[2:0]		Limit for communication error counter for Master and Client	
				000	Errors ignored
				001	1 error allowed
				...	...
				111	7 errors allowed
0x03	reserved	[7]	R/W	reserved	
	longscan	[6]		Enables the permanent pairing / binding mode. The scanning for transmitting Clients is started as long as longscan is set. A transition from 1 to 0 stops binding also when time of binding is shorter than 1 sec	
				0	Disabled, pairing / binding duration is 1 sec
				1	Enabled; pairing / binding mode as long as bit is 1
	reserved	[5]		reserved	
	osc27f	[4]		Enable for 27MHz oscillator manually, only needed for FUSE mode	
	reserved	[3:2]		reserved	
	narmax	[1:0]		Maximum limit of transmission repeats in NAR mode for Master	
				00	No retransmit
				01	1 retransmit
				10	2 retransmit
				11	3 retransmit

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x04	fuseen	[7]	R/W	Poly-PROM fuse mode enable	
				0	Disabled
				1	Enabled
	reserved	[6]		reserved	
	longwake_tx	[5]		Wakeup Transmitter ON-time for Master and Client	
				0	ON for the time set by register waketm<1:0>
				1	ON as long as value of longwake_tx is 1
	wakecyc<2:0>	[4:2]		Wakeup cycle setup; Client (Master) wakeup receiver ON interval	
				000	every 1/16 sec (62.5 ms)
				001	every 1/8 sec (125 ms)
				010	every 1/4 sec (250 ms)
				011	every 1/2 sec (500 ms)
				100	every 1 sec (1000 ms)
				101	every 2 sec (2000 ms)
				110	every 4 sec (4000 ms)
				111	every 8 sec (8000 ms)
	waketm	[1:0]		Wakeup transmitter ON time setting Master (Client) wakeup call duration	
				00	1/8 sec (125 ms)
				01	1/4 sec (250 ms)
				10	1/2 sec (500 ms)
				11	1 sec (1000 ms)

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x05	mcs<1:0>	[7:6]	R/W	Micro controller clock setting at pin MCU_CLK	
				00	OFF
				01	32768 Hz
				10	27MHz divided by mcdr<3:0> settings at active modes
				11	27MHz divided by mcdr<3:0> settings at active modes, 32768 Hz between active modes
	reserved	[5:4]		reserved	
	mcdr	[3:0]		Divider setting Micro controller clock at pin MCU_CLK (clock duty cycle 50%) Clock source is the 27MHz crystal	
				0000	8 (8)
				0001	12 (3*4)
				0010	12 (3*4)
				0011	18 (3*3*2)
				0100	16 (16)
				0101	24 (3*8)
				0110	24 (3*8)
				0111	36 (3*3*4)
				1000	32 (32)
				1001	48 (3*16)
				1010	48 (3*16)
				1011	72(3*3*8)
				1100	64 (64)
				1101	96 (3*32)
				1110	96 (3*32)
				1111	144 (3*3*16)
0x06	reserved	[7:3]	R/W	reserved	
	dev<2>	[2]		Select deviation frequency (setting for the nominal crystal frequency of 27.12MHz) for Master and Client	
				0	Deviation = ± 106 kHz
				1	Deviation = ± 53 kHz
	bitrate<1:0>	[1:0]		Transmission bitrate (setting for the nominal crystal frequency of 27.12MHz) for Master and Client	
				00	26.5 kbit per sec
				01	53 kbit per sec
				10	106 kbit per sec
				11	212 kbit per sec

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x07	lowbatsel_tx	[7]	R/W	Select control of transmitted battery status value source for Master and Client	
				0	Analog value (inverted output register bat_ok)
				1	Digitally faked set value (output register is lowbatval_tx)
	lowbatval_tx	[6]		Value of faked battery status for Master and Client (only valid if lowbatsel_tx = 1)	
				0	Battery OK
				1	Battery LOW
	reserved	[5:0]		reserved	
0x08	id0<23:0>	[7:0]	R/W	**1st Client ID** for the Master mode / Client ID for the Client mode	
0x09					
0x0A					
0x0B	id1<23:0>	[7:0]	R/W only in Master mode	**2nd Client ID** for the Master mode	
0x0C					
0x0D					
0x0E	id2<23:0>	[7:0]	R/W only in Master mode	**3rd Client ID** for the Master mode	
0x0F					
0x10					
0x11	id3<23:0>	[7:0]	R/W only in Master mode	**4th Client ID** for the Master mode	
0x12					
0x13					
0x14	id4<23:0>	[7:0]	R/W only in Master mode	**5th Client ID** for the Master mode	
0x15					
0x16					
0x17	id5<23:0>	[7:0]	R/W only in Master mode	**6th Client ID** for the Master mode	
0x18					
0x19					
0x1A	id6<23:0>	[7:0]	R/W only in Master mode	**7th Client ID** for the Master mode	
0x1B					
0x1C					
0x1D	id7<23:0>	[7:0]	R/W only in Master mode	**8th Client ID** for the Master mode	
0x1E					
0x1F					
0x20	reserved	[7:4]	R/W	reserved	
	rssi_on	[3]		RSSI any time the receiver is active	
				0	Disabled
				1	Enabled
	reserved	[2:0]		reserved	

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x21	reserved	[7:6]	R/W	reserved	
	f200	[5]		Filter upper frequency limit selection from 165kHz to 210kHz. Need to be manually set if datarate is set to 212kbps for Master and Client.	
				0	Datarate less than 212 kbit/sec
				1	Datarate 212 kbit/sec
	bat<1:0>	[4:3]		Battery level with hysteresis of ±40mV for Master and Client	
				00	Threshold 2.0V
				01	Threshold 2.2V
				10	Threshold 2.4V
				11	Threshold 2.6V
	singl	[2]		Disables second output driver and shorts pin RF2OUT to GND for Master and Client	
				0	Disabled
				1	Enabled
	half	[1]		Power Amplifier Output Impedance at pin RF1OUT and RF2OUT	
				0	Output Impedance is 12.5 Ω
				1	Output Impedance is 25.0 Ω
	fzero	[0]		Forces both Power Amplifier Outputs to GND. The short also happens automatically during OOK modulation in the signal OFF period.	
				0	Disabled
				1	Enabled
0x22	reserved	[7:0]	R	reserved	

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x23	reserved	[7]	R	reserved	
	Lbat_ok	[6]		Signals that the battery voltage is higher than the level defined by bat<1:0>. (only valid if lowbatsel_tx = 0)	
				0	BATTERY Low
				1	BATTERY OK
	reserved	[5:4]			reserved
	rssi	[3:0]		4 bit RSSI code of current Master – Client connection	
				0000	0 µVrms
				0001	10 µVrms
				0010	20 µVrms
				0011	30 µVrms
				0100	40 µVrms
				0101	50 µVrms
				0110	60 µVrms
				0111	70 µVrms
				1000	80 µVrms
				1001	90 µVrms
				1010	100 µVrms
				1011	110 µVrms
				1100	120 µVrms
				1101	130 µVrms
				1110	140 µVrms
				1111	150 µVrms
0x24 - 0x26	reserved		reserved		
Interrupt Bits					
0x27	active	[7:0]	R	Indication bits for actual active Timers of Master and Client In Master mode: 8 Client timers	
				00000001	Timer for Client 0 is running
				00000010	Timer for Client 1is running
				00000100	Timer for Client 2 is running
				00001000	Timer for Client 3 is running
				00010000	Timer for Client 4 is running
				00100000	Timer for Client 5 is running
				01000000	Timer for Client 6 is running
				10000000	Timer for Client 7 is running
				11111111	Timers for all Clients are running
				In Client mode: 1st timer is Client timer	
				00000000	Timer at Client is stopped
				00000001	Timer at Client is running

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description
0x28	irq	[7:0]	R	Timer sub-interrupt indicating timed interrupts for transceiver, or-ed to interrupt bit1 in interrupt register 0x2A (cleared when read)
0x29	reserved	[7:0]		reserved
0x2A	scan_end	[7]	R	Interrupt: 1 second scanning has been finished, if not prolonged with longscan bit
	dat_rtx	[6]		Interrupt: indicates that data was received and is ready to be read
	wake_call	[5]		Interrupt: Wakeup signal has been identified. For Client (Master) to send transmit command
	stream_end	[4]		Interrupt: in Client mode it indicates new data should be written into send register, in Master mode it indicates end of transmission
	wrong_id	[3]		Interrupt: activated if ID is not in the ID list
	wrong_crc	[2]		Interrupt: activated if CRC error occurs
	timer_irq	[1]		Interrupt: always activated if one of the irq<7:0>, REG 0x28<7:0> is activated
	reserved	[0]		reserved
0x2B	txend	[7]	R	Interrupt: activated after last bit of CRC is transmitted
	txstart	[6]		Interrupt: activated after last bit of PREAMBLE was transmitted
	rxend	[5]		Interrupt: activated after the whole data was received
	rxstart	[4]		Interrupt: activated after PREAMBLE was received
	nar_rtx	[3]		Interrupt: activated after NAR was received or transmitted
	nak_rtx	[2]		Interrupt: activated after NAK was received or transmitted
	acp_rtx	[1]		Interrupt: activated after ACP was received or transmitted
	ack_rtx	[0]		Interrupt: activated after ACK was received or transmitted
0x2C	msk_scan_end	[7]	R/W	Mask interrupt: scan_end
	msk_dat_rtx	[6]		Mask interrupt: dat_rtx
	msk_wake_call	[5]		Mask interrupt: wake_call
	msk_stream_end	[4]		Mask interrupt: stream_end
	msk_wrong_id	[3]		Mask interrupt: wrong_id
	msk_wrong_crc	[2]		Mask interrupt: wrong_crc
	msk_timer_irq	[1]		Mask interrupt: timer_irq
	msk_timer_stpd	[0]		Mask interrupt: timer_stpd
0x2D	msk_txend	[7]	R/W	Mask interrupt: txend
	msk_txstart	[6]		Mask interrupt: txstart
	msk_rxend	[5]		Mask interrupt: rxend
	msk_rxstart	[4]		Mask interrupt: rxstart
	msk_nar_rtx	[3]		Mask interrupt: nar_rtx
	msk_nak_rtx	[2]		Mask interrupt: nak_rtx
	msk_acp_rtx	[1]		Mask interrupt: acp_rtx
	msk_ack_rtx	[0]		Mask interrupt: ack_rtx
0x2E	reserved	[7:0]		reserved

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description	
0x2F	dabuf<31:0>	[7:0]	R/W	Acknowledge Data sent from Master (sending 4 bytes) received by the Client in ACP mode	
0x30					
0x31					
0x32					
0x33	acp2	[7]	R/W	Enable bit indicating that data2 (dabuf<31:0>) should be sent. This bit is cleared after dabuf was sent	
				0	Disabled
				1	Enabled
	sid2<2:0>	[6:4]	R	Short client ID for ACP where the data2 (dabuf<31:0>) should be sent	
	iit	[3]		idnew is identical to data in ID list at location sid<2:0>	
	sid	[2:0]		Short client ID related to idx<23:0> where x = 0,1,2,3,4,5,6,7	
Data Frame related Bytes					
0x34	idnew<23:0>	[7:0]	R/W	ID of newly detected Client at Pairing mode	
0x35					
0x36					
0x37	user_status2	[7]	R/W	Client Status bit 2: value is user defined	
	user_status1	[6]	R/W	Client Status bit 1: value is user defined	
	user_status0	[5]	R/W	Client Status bit 0: value is user defined	
	dlen	[4:0]	R/W	Decided data length for client / received client data length in master mode	

Table 38. Main Register Bank (ADDRESS 0x00 bit<0>=0)

Address	Register Name	Bit	Type	Description
0x38	dbuf<207:0>	[7:0]	R/W	Payload Data (max 26 bytes) MSB of the Payload Data is always dbuf<207> (REG 0x38<7>)
0x39				
0x3A				
0x3B				
0x3C				
0x3D				
0x3E				
0x3F			R/W (only accessible with auto-incrementing routine)	
0x40				
0x41				
0x42				
0x43				
0x44				
0x45				
0x46				
0x47				
0x48				
0x49				
0x4A				
0x4B				
0x4C				
0x4D				
0x4E				
0x4F				
0x50				
0x51				

8.9.3.2 Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Table 39. Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Register	Name	Bit	Type	Description	
0x08	dprom<31:8>	[7:0]	R/W		Physical PolyProm register<31:8> in the PPROM block Initial device ID, stored into location id0<23:0> after hardware POR or direct command PROM_FUSE, PROM_LOAD, PROM_COPY, CHIP_RESET.
0x09					
0x0A					
0x0B	reserved	[7:0]	R	reserved	

Table 39. Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Register	Name	Bit	Type	Description	
0x0C	cyctim0<2:0>	[7:5]	R/W	Cycle time can be set in Client mode, Cycle time for 1st Client for the Master	
				000	every 1/16 sec (62.5 ms)
				001	every 1/8 sec (125 ms)
				010	every 1/4 sec (250 ms)
				011	every 1/2 sec(500 ms)
				100	every 1 sec(1000 ms)
				101	every 2 sec(2000 ms)
				110	every 4 sec(4000 ms)
				111	every 8 sec(8000 ms)
	rndpt0<4:0>	[4:0]		Random number pointer for 1st client	
0x0D	cyctim1<2:0>	[7:5]	R Timing table for Master	Cycle time for 2nd Client for the Master	
	rndpt1<4:0>	[4:0]		Random number pointer for 2nd client	
0x0E	cyctim2<2:0>	[7:5]		Cycle time for 3rd Client for the Master	
	rndpt2<4:0>	[4:0]		Random number pointer for 3rd client	
0x0F	cyctim3<2:0>	[7:5]		Cycle time for 4th Client for the Master	
	rndpt3<4:0>	[4:0]		Random number pointer for 4th client	
0x10	cyctim4<2:0>	[7:5]		Cycle time for 5th Client for the Master	
	rndpt4<4:0>	[4:0]		Random number pointer for 5th client	
0x11	cyctim5<2:0>	[7:5]		Cycle time for 6th Client for the Master	
	rndpt5<4:0>	[4:0]		Random number pointer for 6th client	
0x12	cyctim6<2:0>	[7:5]		Cycle time for 7th Client for the Master	
	rndpt6<4:0>	[4:0]		Random number pointer for 7th client	
0x13	cyctim7<2:0>	[7:5]		Cycle time for 8th Client for the Master	
	rndpt7<4:0>	[4:0]		Random number pointer for 8th client	
0x14	reserved	[7]	R/W Error Table for Master	reserved	
	ces1<2:0>	[6:4]		Actual Communication Error count of 2nd client	
				000	Last packet received successfully
				001	1 packet incorrectly received
				...	...
				111	7 packets incorrectly received
	reserved	[3]		reserved	
	ces0<2:0>	[2:0]		Actual Communication Error count of 1st client	

Table 39. Shadow Register Bank (ADDRESS 0x00 bit<0>=1)

Register	Name	Bit	Type	Description
0x15	reserved	[7]	R/W Error Table for Master	reserved
	ces3<2:0>	[6:4]		Actual Communication Error count of 4th client
	reserved	[3]		reserved
	ces2<2:0>	[2:0]		Actual Communication Error count of 3rd client
0x16	reserved	[7]	R/W Error Table for Master	reserved
	ces5<2:0>	[6:4]		Actual Communication Error count of 6th client
	reserved	[3]		reserved
	ces4<2:0>	[2:0]		Actual Communication Error count of 5th client
0x17	reserved	[7]	R/W Error Table for Master	reserved
	ces7<2:0>	[6:4]		Actual Communication Error count of 8th client
	reserved	[3]		reserved
	ces6<2:0>	[2:0]		Actual Communication Error count of 7th client
0x18 - 0x1D	reserved	[7:0]		reserved

8.10 Feature Description

This chapter describes how to apply certain features of the device.

8.10.1 One Time Programmable Memory (OTP)

The OTP is 4 times a 8bit (32bits) poly fuse based PROM. This is an austriamicrosystems IP-block called PPROM. It is described in a separate documents P2PROM_rev1.322 and PPROM_appl_note_C.

The ID data has to be written into the Shadow Register Bank REG 0x08, 0x09, 0x0A.

8.10.1.1 Write to the OTP register

To enable the Write mode the device must be turned on with the command POWER_ON. Set the fuseen bit in REG 0x04<7> and switch to the SHADOW register with the command SHADOW_BANK. The data (e.g. ID) that should be programmed must be written via SDI into the Shadow Register Bank register dprom in REG 0x08 to 0x0A. These are already the physical PPROM registers, which are ready to be programmed.

8.10.1.2 Programming of the OTP

To enable the programming, the bit bank, REG 0x00<0>, bit fuseen, REG 0x04<7>, bit pwr, REG 0x00<1> and the bit osc27f, REG 0x03<4> have to be set to 1. With the command PROM_FUSE pulse, the programming of the OTP is executed. After 2 ms the automatic fusing will be ended. To verify the correct programming reset the chip by disconnecting the power supply of the AS3900. After powering the chip again, the values read from the ID0 register must be the same as the programmed ones.

8.10.1.3 Read the Fuses

To enable the Read mode the bit bank, REG 0x00<0>, bit pwr, REG 0x00<1> and the bit osc27f, REG 0x03<4> must be set to 1. With the command PROM_LOAD pulse the values of the fuses are loaded to the register dprom, REG 0x08 to 0x0A after 0.8ms. After reading the same values are loaded to the ID0 register.

8.10.1.4 Read the Fuses and Load to ID0 Register

To enable this mode the bit bank, REG 0x00<0> must set 1. With the command PROM_COPY pulse the values of the fuses are loaded to the register dprom, REG 0x08 to 0x0A and the values from the registers dprom are copied to the Main Register Bank register ID0, REG 0x08 to 0x0A.

The same procedure is performed with the POR Signal automatically.

8.10.2 Communication Error Counter (cesmax)

The communication error counter can be enabled, in order to automatically turn off the communication to a lost Client. This feature allows the automatic disabling of the Timer at Master and/or Client side.

If the actual communication error count of one Client cesX in register SREG 0x14 to 0x17 reaches the maximum allowed communication errors set in cesmax in REG 0x02<2:0>, the according Timer is turned off.

At the Master, the dedicated Client Timer goes inactive that can be read out via the register activeTimers in REG 0x27. This register needs to be polled. It is only possible to set one limit for the communication error counter cesmax for all available Clients at the Master. The only possibility to set individual limits for the different Clients is, to set an initial value at the actual communication error count cesX in the SHADOW register. An error would increase the cesX field starting from the initial value, which allows the disabling of the dedicated Timer at fewer counts.

At the Client, the Timer goes inactive that is signaled when the activeTimer0 is reset to '0'. REG 0x27<0> is set to 0.

The communication error counter can be disabled by setting cesmax to 0x00 in register REG 0x02<2:0> at the Clients and at the Master. If some Clients are lost, the Master does not stop its transmission at the dedicated time slots.

The following table summarizes the changing of the cesX (cesX stands for ces0, ces1 … ces7):

Table 40. Actual Communication Error Count cesX

Reply	Master: cesX in SREG 0x14 to 0x17	Client: ces0 in SREG 0x14<2:0>
ACK	cesX is cleared, set to zero	ces0 is cleared, set to zero
ACP	cesX is cleared, set to zero	ces0 is cleared, set to zero
NAK	cesX is increased	ces0 is increased
NAR	cesX is not changed	ces0 is not changed
No reply	cesX is increased	ces0 is increased

8.10.3 Cycle Time and Random Pointer

The Cycle time defines the starting point of the dedicated time slot. The cycle time can be set individually at the Client in REG 0x0C<7:5>. This individual cycle time is included in every packet send to the Master. This timing information is stored into the timing table of the Master in REG 0x0C to 0x13.

The cycle time can be fixed or varied by the pseudo random pointer. If the pseudo random pointer in REG 0x0C<4:0> is set to 0 the cycle time is constant. A different value leads to a random variation of maximal ±30% of the cycle time. This feature reduces the likelihood of a collision. If the random pointer is used, each Client should use a different one. Otherwise the shift of the cycle time would be the same, because the algorithm behind is the identically for each Client (pseudo random). The random pointer is included in the timing information of each packet and is stored automatically in the Masters timing table in register REG 0x0C to 0x13<4:0>.

The length of the time slot is defined by the data rate multiplied by the frame size. The frame mainly depends on the payload that can be set by dlen in register REG 0x37<4:0>. The data rate is defined in REG 0x06<1:0>.

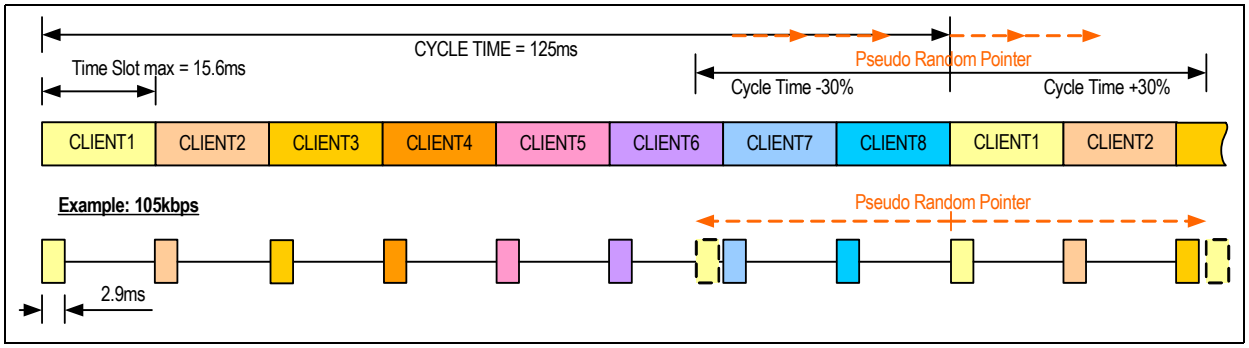
The following example shows the timing separation with 8 Clients. Therefore a cycle time of 125ms for each Client was set, resulting in a maximum time slot of 15.6ms. The actual allocated time slot is defined by:

$$Timeslot = 8, \frac{(dlen + 11 ByteHeader + 3 ByteACK)}{bitrate}$$

(EQ 1)

This equals for the maximum payload of 24 bytes and a bit rate of 105kbps to an allocated time slot of 2.9ms. As seen in the figure all packets are static. Using the random pointer results in spontaneously changing the time slot, as denoted for Client 1 (yellow packets).

Figure 25. Battery Level Indicator



8.10.4 Battery Level Indicator

The AS3900 has an integrated battery level detection, which is realized with an analog comparator. The actual battery level is compared to a reference voltage that can be set via the SDI interface. The reference voltage can be selected between 2.6V to 2.0V in REG 0x21<1:0>, and has a hysteresis of ±40mV. The output of the comparator can be selected inverted analog or digital faked output signal via lowbatsel_tx in REG 0x07<7>. Depending on this setting the comparator output bit is routed to lowbatval_tx in REG 0x07<6> or Lbat_ok in REG 0x23<6>.

The comparator can only indicate if the reference level is lower or higher than the actual battery level. In order to get the correct level of the battery, the reference voltage needs to be set to a lower value via the SDI interface, if the output signal of the comparator indicates battery = LOW.

With this algorithm the reference level is always updated and reflects the actual battery level that can be read out in REG 0x21<1:0>.

8.10.5 Output Power Selection

The AS3900 has a kind of integrated class D power amplifier that output power can be changed by changing the load impedance seen by the PA. Furthermore the output power can be varied by the switching from differential output to single ended mode.

8.10.5.1 Single Ended / Differential

In single ended mode the second output RF2OUT is always tight to GND. Only RF1OUT delivers an RF-signal close to VDD with a frequency of the crystal oscillator. This adjustment can be set via the single bit in the REG 0x21<2>.

In differential mode RF1OUT is switched to VDD and RF2OUT is switched to GND for the first cycle. For the second cycle RF1OUT is switched to GND and RF2OUT is switched to VDD. In differential mode the output voltage between RF1OUT and RF2OUT is approximately twice the VDD.

Note: It is important to note that the PA switches their output automatically to GND during the AS3900 is in receive mode (LNA is turned on). It is possible to set the PA outputs manually to GND via the bit fzero in REG 0x21<0>.

8.10.5.2 Output Impedance

The output impedance Rout can be set to 25Ω or 12.5Ω. Rout describes the sum of both output stages (RF1OUT and RF2OUT) and limits the current that drives the antenna and matching network. The output impedance can be changed by the bit half in REG 0x21<1>. Rout was implemented to prevent the AS3900 from burning, if the outputs of the PA are shorted.

8.10.5.3 Calculation of the load impedance for a desired output power

The output power can be calculated as following using the PA differentially:

$$P(dBm) = 10,\log\left(\frac{(U_{ANT+MATCH_{RMS}})^2}{R_{ANT+MATCH}\times 1mW}\right)$$

Where:

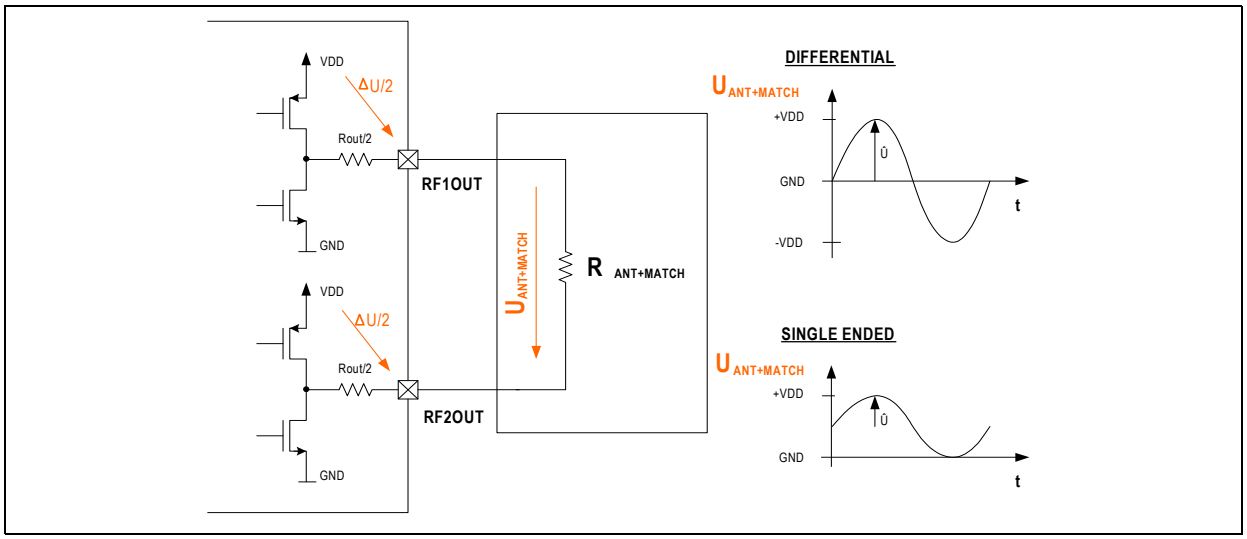
$$U_{ANT+MATCH_{RMS}} = \frac{VDD-\Delta U}{\sqrt{2}}$$

$$U \cong 0,1V$$

In differential mode peak is equal to VDD, in single ended mode peak is equal to VDD/2.

Note: It is important to note that the overall emitted power of the PA is mainly defined by the VDD and the impedance of the antenna itself. The Rout of the PA gives only a minor change to the emitted power.

Figure 26. Power Amplifier



The following example demonstrates the calculation of impedance of the antenna and matching network ($R_{ANT+MATCH}$) for a specified output power:

Conditions: VDD= 3V, Differential output mode, 10dBm is the desired output power.

$$P(mW) = 10^{\frac{P(dBm)}{10}} = 10mW$$

$$R_{ANT+MATCH} = \frac{U_{ANT+MATCH_{RMS}}{}^2}{P} = \frac{\left(\frac{VDD-\Delta U}{\sqrt{2}}\right)^2}{P} = \frac{\left(\frac{3V-0.1V}{\sqrt{2}}\right)^2}{10mW} = 420\Omega$$

8.10.6 RSSI

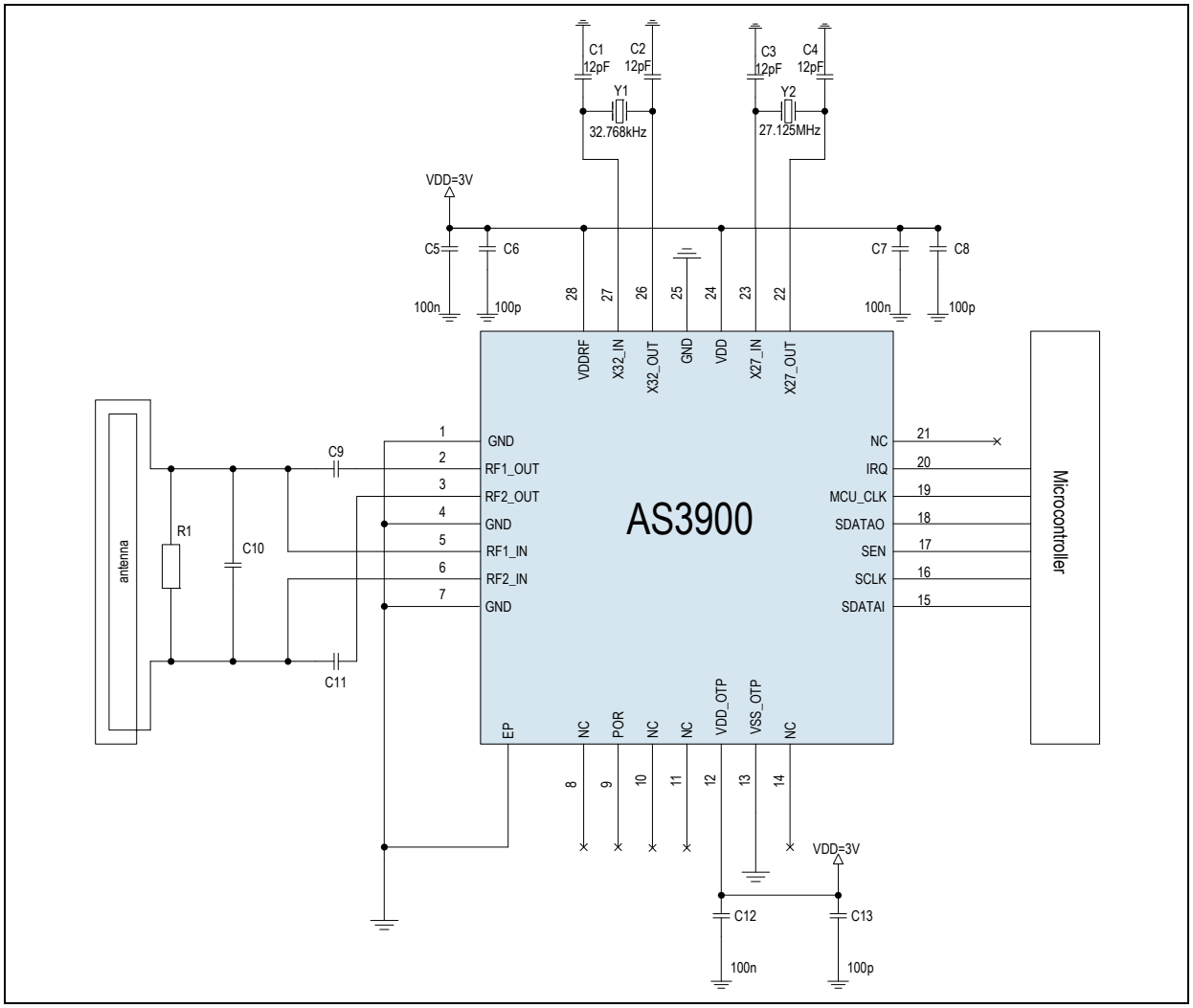
The AS3900 has an integrated received signal strength indication field (RSSI) that can be used by the Master to identify the signal strength to all available Clients. If this block is turned on via the rssi_on bit in REG 0x20<3>, the actual signal strength can be read from REG 0x23<3:0>. The rssi field provides a digital value for signal strength between 0µVrms and 150µVrms.

The rssi field is valid for the Client that communicates currently with the Master, which can be identified via the sid in REG 0x33<2:0>.

9 Application Information

The AS3900 is capable to operate with a few external components. The typical application circuit is shown in Figure 27. The system consists of the AS3900 Block, the MCU and an antenna.

Figure 27. AS3900 Application diagram



9.1 Microcontroller

The integrated link manager takes over a huge workload for the RF communication. The microcontroller takes over the high level communication like the control of the RF link. The SDI interface of the AS3900 allows connection of a standard 3-wire SPI interface. Only the SEN line needs to be handled manually by a GPIO. The levels of the I/O lines of the MCU must match with the supply voltage range of the AS3900. Otherwise the internal overvoltage protection circuit could get activated. As system frequency the MCU_CLK can be used, that reduces the BOM of the MCU. An external interrupt input at the MCU is necessary in order to control the link manager.

9.2 Crystal Oscillators

Two external crystal oscillators are needed for the application, which need two external loading capacitors (C1-C4). The loading capacitor values depend on the total load capacitance CL, specified for each crystal. The total load capacitance that is seen between the crystal terminals should be equal to the specified CL, so that the crystal oscillates at the specified frequency. The crystal oscillators need to fulfill the accuracy specification of ±120ppm. A small SMD crystal is used in the demo board.

Table 41. Recommended Crystal Oscillators

Crystal	Part Number	Frequency	Accuracy	Load capacitance	Dimensions (L/W/T)	Manufacturer
Y1	CC7V-TA1	32.768kHz	±20ppm	9pF	1.5x3.2x0.9mm	Micro Crystal
Y2	FA-128R	27.12MHz	±15ppm	8pF	2.0x1.6x0.5mm	Epson Toyocom

9.3 Power Supply

Due to fast switching of internal blocks of the AS3900, the power supply pins need to be buffered by decoupling capacitors. These capacitors guarantee a low impedance supply line over a wide frequency range. Fast transient currents are supplied by these decoupling capacitors and avoid voltage spikes on the supply. A parallel circuit of 1µF, 100nF, 100pF capacitors is recommended on all supply pins (VDDRF, VDD, VDD_OTP). Small-sized X5R or X7R ceramic capacitors are recommended.

Note: VDD_OTP is only needed in fuse mode, and requires 3.6V for burning the internal fuses. Otherwise VDD_OTP need not be connected.

9.4 Antenna

As at 27MHz the wavelength is several meters it would be very challenging to implement an electromagnetic antenna with acceptable performances (2m communication range) and small dimensions (some cm), therefore the loop antenna based on magnetic coupling would be preferred.

This design consists of the design of the following antennas:

- PCB (1 or 2 layers) loop antenna: Dimensions: half credit card. Expected range >2m
- Ferrite core antenna: Samples from different coil manufacturer are already available. Expected range >1m
- Capacitive coupling antenna: The resonator consists of SMD discrete components, but PCB patches are used for capacitive coupling with metal or human body. Expected range is some cm but becomes very big as long as the body or metal is in the proximity of the patches
- Pseudo SMD electric antenna: A λ/4 antenna is wound to a coil but acts totally electric.

9.5 Tuning Circuit

Each antenna needs to be tuned for the 27.12MHz ISM band. Usually a parallel resonance circuit is applied. The inductance of the loop antenna is brought into resonance by C10. R1 defines the quality factor Q. C9 and C11 are decoupling capacitors that are mandatory because in receive mode the PA is shorted to GND.

For C9, C10 and C11 small-sized ceramic capacitors are recommended. COG ceramic capacitors are recommended as they retain capacitance over wide range of voltage and temperature.

More information regarding the antenna design its tuning circuits are available in the antenna application note. The AS3900 demo board features a PCB loop antenna with a parallel resonance tuning circuit.

The AS3900 requires following external components.

Table 42. External Components

Num	Component	Value	Description	Note
1	C1, C2	12pF	COG, 50V, 0603, Ceramic capacitor ±5%	Loading Capacitor for 32.768kHz Crystal C1,C 2max = 36pF
2	C3, C4	12pF	COG, 50V, 0603, Ceramic capacitor ±5%	Loading Capacitor for 27.12MHz Crystal C3, C4max = 36pF
3	C5, C7,C12	100nF	X7R, 25V, 0603, Ceramic capacitor ±10%	Supply Voltage de-coupling capacitor
4	C6, C8, C13	100pF	X7R, 25V, 0603, Ceramic capacitor ±10%	Supply Voltage de-coupling capacitor
5	C12	10µF	X5R, 16V, 0805, Capacitor ±10%	OTP Fuse Mode only
6	C9, C11	10pF to 47pF	COG, 50V, 0603, Ceramic capacitor ±5%	PA decoupling capacitor; antenna dependant

Table 42. External Components

Num	Component	Value	Description	Note
7	C10	10pF to 470pF	COG, 50V, 0603, Ceramic capacitor ±5%	Resonance capacitor; antenna dependant
8	R1	1kΩ to ∞	0.01W, 0603, resistor	Resistor for quality factor; antenna dependant
9	Y1	32.768kHz	32.768kHz fundamental mode crystal ±120ppm overall tolerance	Crystal Oscillator for internal timers
10	Y2	27.12MHz	27.12MHz fundamental mode crystal ±100ppm overall tolerance	Crystal Oscillator for carrier frequency

10 Package Drawings and Markings

The product is available in a QFN 28 pin package.

Figure 28. AS3900 Package Diagram

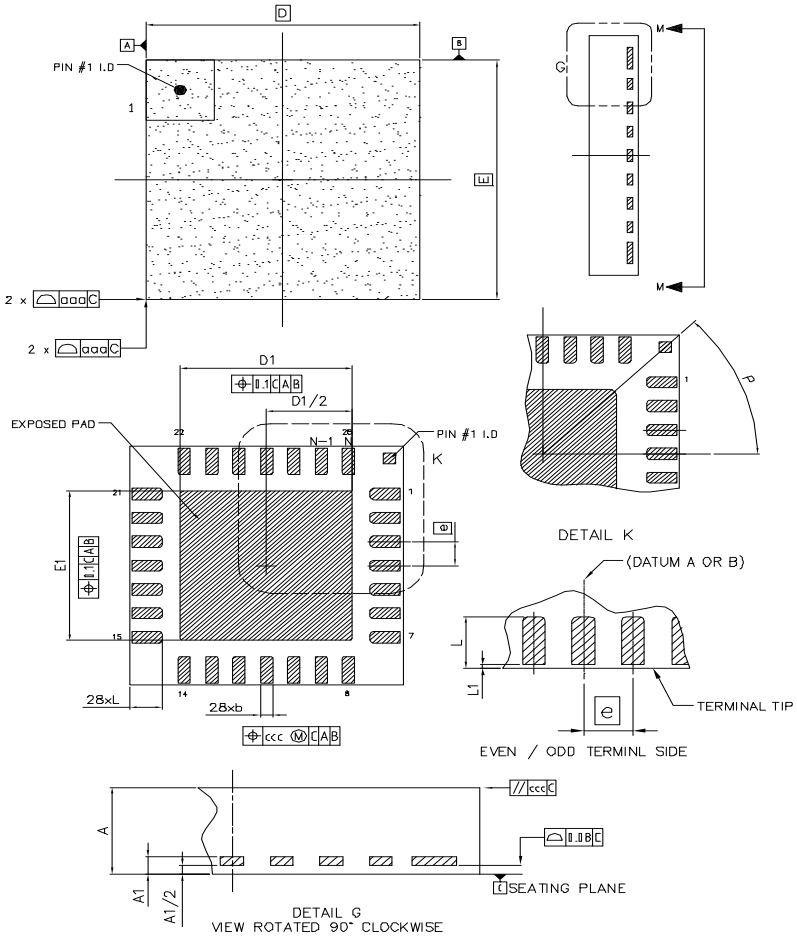


Table 43. Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.80		1.00	e		0.50 BSC	
A1		0.203 REF		L	0.50	0.60	0.75
b	0.18	0.23	0.30	L1			0.10
D		5.00 BSC		P		45° BSC	
E		5.00 BSC		aaa		0.15	
D1	3.04	3.14	3.24	cccc		0.10	
E1	3.04	3.14	3.24				

Note: All dimensions are in Millimeters and angles in Degrees

Dimensioning and Toleranceing confirm to ASME Y14.5M-1994

Dimension b applies to metalized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge to 0.1mm is acceptable.

11 Ordering Information

Table 44. Ordering Information

Ordering Code	Type	Marking	Delivery Form[1]	Delivery Quantity
AS3900-BQFT	QFN 5x5 28LD	AS3900	7 inches Tape&Reel	1000 pcs

1. Dry Pack Sensitivity Level =3 according to IPC/JEDEC J-STD-033A for full reels.

Note: All products are RoHS compliant and Pb-free.
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For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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