87C196LA-20 MHz CHMOS 16-bit Microcontroller

Automotive

Advanced Information Datasheet

Product Features

- Up to 20 MHz operation
- 24 Kbytes of on-chip OTPROM
- 768 bytes of on-chip register RAM
- Register-to-register architecture
- Peripheral transaction server (PTS) with high-speed, microcoded interrupt service routines
- Six-channel/10-bit A/D with sample and hold
- High-speed event processor array
  - —Six capture/compare channels
  - —Two compare-only channels
  - —Two 16-bit software timers
- Full-duplex serial I/O port with dedicated baud-rate generator
- Enhanced full-duplex, synchronous serial I/O port (SSIO)
- Programmable 8- or 16-bit external bus
- Selectable clock doubler with programmable clock output signal
- SFR register that indicates the source of the last reset
- Design enhancements for EMI reduction
- Oscillator failure detection circuitry
- Watchdog timer (WDT)
- -40° C to +125° C ambient temperature
- 52-pin PLCC package

Notice: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 272806-004
August 2004

Advance Information Datasheet

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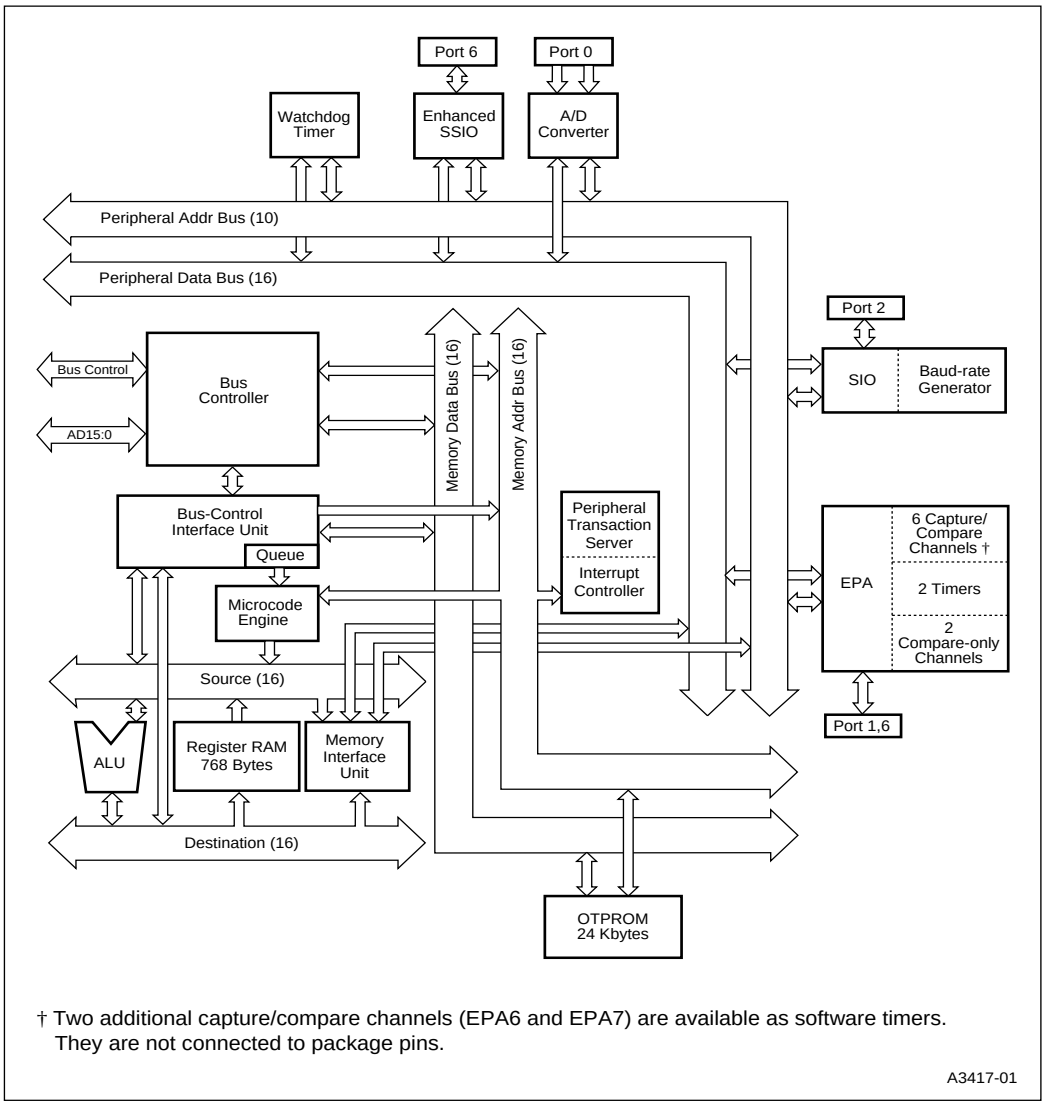
1.0 Introduction

The 87C196LA is a high-performance 16-bit microcontroller. The 87C196LA is composed of a high-speed core with the following peripherals: an asynchronous/synchronous serial I/O port (8096 compatible) with a dedicated 16-bit baud-rate generator; an additional synchronous serial I/O port with full duplex master/slave transceivers; a six-channel A/D converter with sample and hold; a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities; six modularized, multiplexed high-speed I/O for capture and compare (called event processor array) with 200 ns resolution and double buffered inputs; and a sophisticated, prioritized interrupt structure with programmable peripheral transaction server (PTS). The clock doubler circuitry and oscillator output signal enable a 4 MHz resonator to achieve the same internal clock speed as a more costly 8 MHz resonator in previous applications. This same circuitry can drive other devices where a separate resonator was required in the past. Another cost-savings feature is the fact that the I/O ports are driven low at reset, avoiding the need for pull-up resistors.

Figure 1. 87C196LA Block Diagram



† Two additional capture/compare channels (EPA6 and EPA7) are available as software timers. They are not connected to package pins.

A3417-01

2.0 Nomenclature Overview

Figure 2. Product Nomenclature

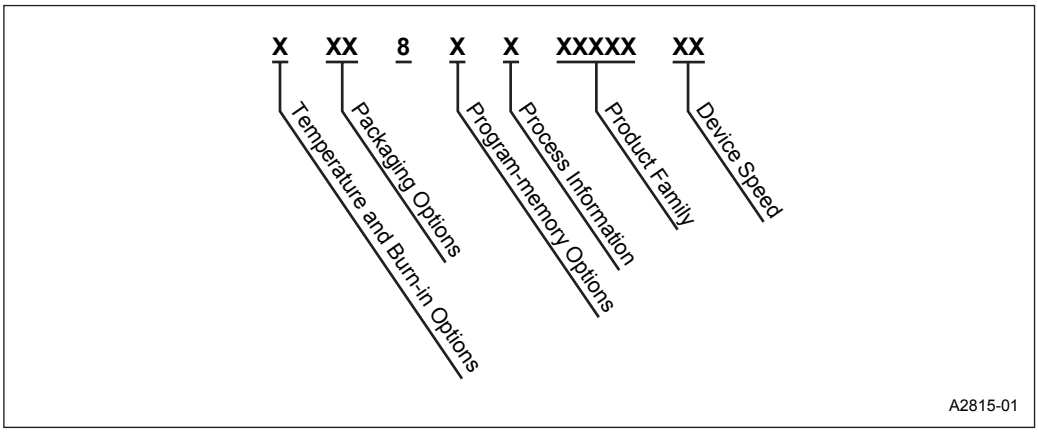


Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	x	Automotive operating temperature range (-40°C to 125°C ambient) with Intel standard burn-in.
Packaging Options	x	PLCC
Program-memory Options	7	OTPROM
Process Information	C	CHMOS
Product Family	196L*x*	8XC196L*x* family of products
Device Speed	20	20 MHz

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

3.0 Pinout

Figure 3. 87C196LA 52-pin Package

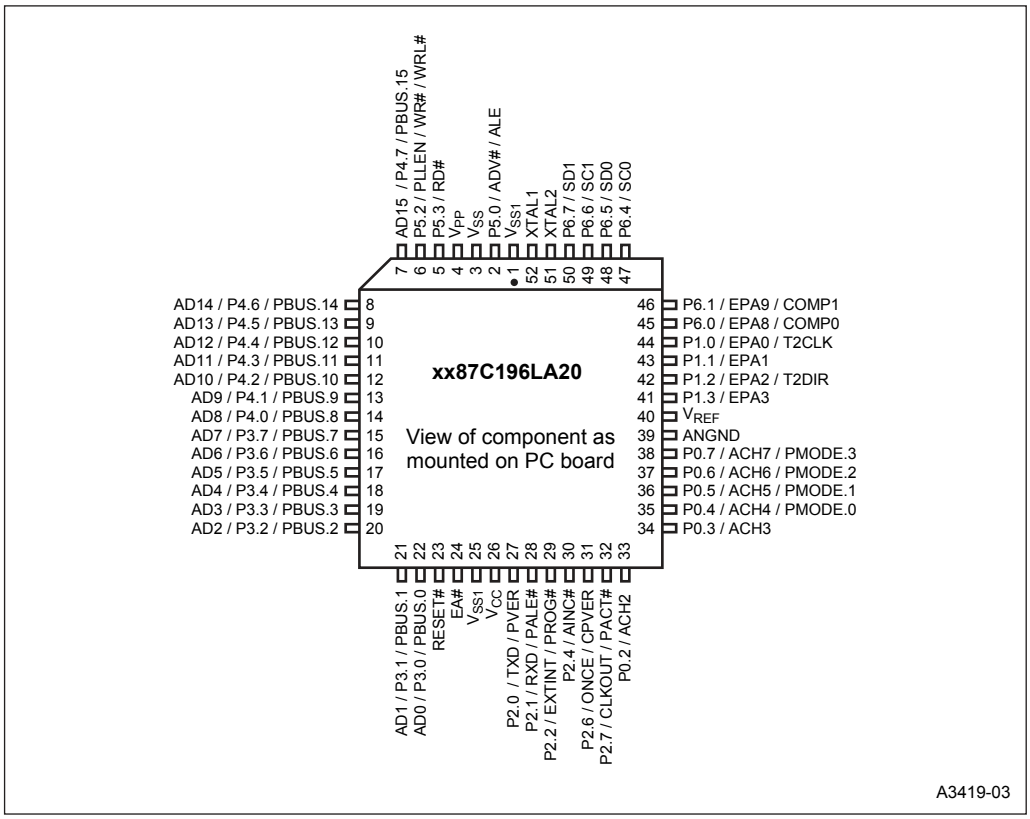


Table 2. 87C196LA 52-pin Package Pin Assignments

Pin	Name	Pin	Name	Pin	Name
1	V_{SS1}	19	AD3 / P3.3 / PBUS.3	37	P0.6 / ACH6 / PMODE.2
2	P5.0 / ADV# / ALE	20	AD2 / P3.2 / PBUS.2	38	P0.7 / ACH7 / PMODE.3
3	V_{SS}	21	AD1 / P3.1 / PBUS.1	39	ANGND
4	V_{PP}	22	AD0 / P3.0 / PBUS.0	40	V_{REF}
5	P5.3 / RD#	23	RESET#	41	P1.3 / EPA3
6	P5.2 / PLLEN / WR# / WRL#	24	EA#	42	P1.2 / EPA2 / T2DIR
7	AD15 / P4.7 / PBUS.15	25	V_{SS1}	43	P1.1 / EPA1
8	AD14 / P4.6 / PBUS.14	26	V_{CC}	44	P1.0 / EPA0 / T2CLK
9	AD13 / P4.5 / PBUS.13	27	P2.0 / TXD / PVER	45	P6.0 / EPA8 / COMP0
10	AD12 / P4.4 / PBUS.12	28	P2.1 / RXD / PALE#	46	P6.1 / EPA9 / COMP1
11	AD11 / P4.3 / PBUS.11	29	P2.2 / EXTINT / PROG#	47	P6.4 / SC0
12	AD10 / P4.2 / PBUS.10	30	P2.4 / AINC#	48	P6.5 / SD0
13	AD9 / P4.1 / PBUS.9	31	P2.6 / ONCE/CPVER	49	P6.6 / SC1
14	AD8 / P4.0 / PBUS.8	32	P2.7 / CLKOUT / PACT#	50	P6.7 / SD1
15	AD7 / P3.7 / PBUS.7	33	P0.2 / ACH2	51	XTAL2
16	AD6 / P3.6 / PBUS.6	34	P0.3 / ACH3	52	XTAL1
17	AD5 / P3.5 / PBUS.5	35	P0.4 / ACH4 / PMODE.0		
18	AD4 / P3.4 / PBUS.4	36	P0.5 / ACH5 / PMODE.1		

Table 3. Pin Assignment Arranged by Functional Categories

Addr & Data	
Name	**Pin**
AD0	22
AD1	21
AD2	20
AD3	19
AD4	18
AD5	17
AD6	16
AD7	15
AD8	14
AD9	13
AD10	12
AD11	11
AD12	10
AD13	9
AD14	8
AD15	7

Input/Output	
Name	**Pin**
P0.2 / ACH2	33
P0.3 / ACH3	34
P0.4 / ACH4	35
P0.5 / ACH5	36
P0.6 / ACH6	37
P0.7 / ACH7	38
P1.0 / EPA0 / T2CLK	44
P1.1 / EPA1	43
P1.2 / EPA2 / T2DIR	42
P1.3 / EPA3	41
P2.0 / TXD	27

Input/Output (Cont'd)	
Name	**Pin**
P2.1 / RXD	28
P2.2	29
P2.4	30
P2.6	31
P2.7	32
P3.0	22
P3.1	21
P3.2	20
P3.3	19
P3.4	18
P3.5	17
P3.6	16
P3.7	15
P4.0	14
P4.1	13
P4.2	12
P4.3	11
P4.4	10
P4.5	9
P4.6	8
P4.7	7
P5.0	2
P5.2	6
P5.3	5
P6.0 / EPA8 / COMP0	45
P6.1 / EPA9 / COMP1	46
P6.4 / SC0	47
P6.5 / SD0	48
P6.6 / SC1	49
P6.7 / SD1	50

Program Control	
Name	**Pin**
AINC#	30
CPVER	31
PACT#	32
PALE#	28
PBUS.0	22
PBUS.1	21
PBUS.2	20
PBUS.3	19
PBUS.4	18
PBUS.5	17
PBUS.6	16
PBUS.7	15
PBUS.8	14
PBUS.9	13
PBUS.10	12
PBUS.11	11
PBUS.12	10
PBUS.13	9
PBUS.14	8
PBUS.15	7
PMODE.0	35
PMODE.1	36
PMODE.2	37
PMODE.3	38
PROG#	29
PVER	27

Processor Control	
Name	**Pin**
EA#	24
EXTINT	29
PLLEN	6
RESET#	23
XTAL1	52
XTAL2	51

Bus Cont & Status	
Name	**Pin**
ADV# / ALE	2
CLKOUT	32
RD#	5
WR# / WRL#	6

Power & Ground	
Name	**Pin**
ANGND	39
V_{CC}	26
V_{PP}	4
V_{REF}	40
V_{SS}	3
V_{SS1}	1
V_{SS1}	25

4.0 Signals

Table 4. Signal Descriptions (Sheet 1 of 6)

Name	Type	Description
ACH7:2	I	Analog Channels These signals are analog inputs to the A/D converter. The A/D inputs share package pins with port 0. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*y*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. The ANGND and V_{REF} pins must be connected for the A/D converter and port 0 to function. ACH7:2 share package pins with the following signals: ACH2/P0.2, ACH3/P0.3, ACH4/P0.4/PMODE.0, ACH5/P0.5/PMODE.1, ACH6/P0.6/PMODE.2, and ACH7/ P0.7/PMODE.3.
AD15:0	I/O	Address/Data Lines These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred. AD7:0 share package pins with P3.7:0 and PBUS.7:0. AD15:8 share package pins with P4.7:0 and PBUS.15:8.
ADV#	O	Address Valid This active-low output signal is asserted only during external memory accesses. ADV# indicates that valid address information is available on the system address/ data bus. The signal remains low while a valid bus cycle is in progress and is returned high as soon as the bus cycle completes. An external latch can use this signal to demultiplex the address from the address/ data bus. A decoder can also use this signal to generate chip selects for external memory. ADV# shares a package pin with P5.0 and ALE.
AINC#	I	Auto Increment During slave programming, this active-low input enables the auto-increment feature. (Auto increment allows reading or writing of sequential OTPROM locations, without requiring address transactions across the programming bus for each read or write.) AINC# is sampled after each location is programmed or dumped. If AINC# is asserted, the address is incremented and the next data word is programmed or dumped. AINC# shares a package pin with P2.4.

Table 4. Signal Descriptions (Sheet 2 of 6)

Name	Type	Description
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus. An external latch can use this signal to demultiplex the address from the address/data bus. ALE shares a package pin with P5.0 and ADV#.
ANGND	GND	Analog Ground ANGND must be connected for A/D converter and port 0 operation. ANGND and V_{SS} should be nominally at the same potential.
CLKOUT	O	Clock Output Output of the internal clock generator. You can select one of three frequencies: f, f/2, or f/4. CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7 and PACT#.
COMP1:0	O	Event Processor Array (EPA) Compare Pins These signals are the outputs of the EPA compare-only channels. COMP1:0 share package pins with the following signals: COMP0/P6.0/EPA8 and COMP1/P6.1/EPA9.
CPVER	O	Cumulative Program Verification During slave or programming, a high signal indicates that all locations programmed correctly, while a low signal indicates that an error occurred during the program operation. CPVER shares a package pin with P2.6 and ONCE#.
EA#	I	External Access This input determines whether memory accesses to special-purpose and program memory partitions are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant. EA# also controls entry into the programming modes. If EA# is at V_{PP} voltage (typically +12.5 V) on the rising edge of RESET#, the microcontroller enters a programming mode. EA# is sampled and latched only on the rising edge of RESET#. Changing the level of EA# after reset has no effect.
EPA9:8 EPA3:0	I/O	Event Processor Array (EPA) Capture/Compare Channels High-speed input/output signals for the EPA capture/compare channels. The EPA signals share package pins with the following signals: EPA0/P1.0/T2CLK, EPA1/P1.1, EPA2/P1.2/T2DIR, EPA3/P1.3, EPA8/P6.0/COMP0, and EPA9/P6.1/COMP1. EPA7:6 do not connect to package pins. They cannot be used to capture an event, but they can function as software timers. EPA5:4 are not implemented.

Table 4. Signal Descriptions (Sheet 3 of 6)

Name	Type	Description
EXTINT	I	External Interrupt In normal operating mode, a rising edge on EXTINT sets the EXTINT interrupt pending bit. EXTINT is sampled during phase 2. The minimum high time is one state time. In powerdown mode, asserting the EXTINT signal causes the device to resume normal operation. The interrupt does not need to be enabled. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT shares a package pin with P2.2 and PROG#.
P0.7:2	I	Port 0 This is a high-impedance, input-only port. Port 0 pins should **not** be left floating. The port 0 signals share package pins with the A/D inputs. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*y*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. ANGND and V_{REF} must be connected for port 0 to function. P0.3:2 share package pins with ACH3:2 and P0.7:4 share package pins with ACH7:4 and PMODE.3:0.
P1.3:0	I/O	Port 1 This is a standard bidirectional port that shares package pins with individually selectable special-function signals. Port 1 shares package pins with the following signals: P1.0/EPA0/T2CLK, P1.1/ EPA1, P1.2/EPA2/T2DIR, P1.3/EPA3.
P2.7:6 P2.4 P2.2:0	I/O	Port 2 This is a standard bidirectional port that shares package pins with individually selectable special-function signals. Port 2 shares package pins with the following signals: P2.0/TXD/PVER, P2.1/RXD/ PALE#, P2.2/EXTINT/PROG#, P2.4/AINC#, P2.6/ONCE/CPVER. P2.7/OSCOUT/PACT# is output pin only.
P3.7:0	I/O	Port 3 This is a memory-mapped, 8-bit, bidirectional port with programmable open-drain or complementary output modes. The pins are shared with the multiplexed address/data bus, which has complementary drivers. P3.7:0 share package pins with AD7:0 and PBUS.7:0.
P4.7:0	I/O	Port 4 This is a memory-mapped, 8-bit, bidirectional port with open-drain or complementary output modes. The pins are shared with the multiplexed address/ data bus, which has complementary drivers. P4.7:0 share package pins with AD15:8 and PBUS.15:8.
P5.3:2 P5.0	I/O	Port 5 This is a memory-mapped, bidirectional port. Port 5 shares package pins with the following signals: P5.0/ADV#/ALE, P5.2/WR#/ WRL#/PLLEN, and P5.3/RD#. P5.1 and P5.7:4 are not implemented.

Table 4. Signal Descriptions (Sheet 4 of 6)

Name	Type	Description
P6.7:4 P6.1:0	O	Port 6 This is a standard bidirectional port. Port 6 shares package pins with the following signals: P6.0/EPA8/COMP0, P6.1/ EPA9/COMP1, P6.4/SC0, P6.5/SD0, P6.6/SC1, and P6.7/SD1.
PACT#	O	Programming Active During auto programming or slave dump, a low signal indicates that programming or dumping is in progress, while a high signal indicates that the operation is complete. PACT# shares a package pin with P2.7 and OSCOUT.
PALE#	I	Programming ALE During slave programming, a falling edge causes the device to read a command and address from the programming bus. PALE# is multiplexed with P2.1 and RXD.
PBUS.15:0	I/O	Address/Command/Data Bus During slave programming, ports 3 and 4 serve as a bidirectional port with open-drain outputs to pass commands, addresses, and data to or from the device. Slave programming requires external pull-up resistors. During auto programming and ROM-dump, ports 3 and 4 serve as a regular system bus to access external memory. P4.6 and P4.7 are left unconnected; P1.1 and P1.2 serve as the upper address lines. **Slave programming:** PBUS.7:0 share package pins with AD7:0 and P3.7:0. PBUS.15:8 share package pins with AD15:8 and P4.7:0. **Auto programming:** PBUS.15:8 share package pins with AD15:8 and P4.7:0; PBUS.7:0 share package pins with AD7:0 and P3.7:0.
PLLEN	I	Phase-locked Loop Enable This active-high input pin enables the on-chip clock multiplier. Tie this pin to V_{CC} at power-up to bypass the on-chip clock multiplier.
PMODE.3:0	I	Programming Mode Select These pins determine the programming mode. PMODE3:0 are sampled after a device reset and must be static while the microcontroller is operating. PMODE3:0 share package pins with P0.7:4 and ACH7:4.
PROG#	I	Programming Start During programming, a falling edge latches data on the programming bus and begins programming, while a rising edge ends programming. The current location is programmed with the same data as long as PROG# remains asserted, so the data on the programming bus must remain stable while PROG# is active. During a word dump, a falling edge causes the contents of an OTPROM location to be output on the PBUS, while a rising edge ends the data transfer. PROG# shares a package pin with P2.2 and EXTINT.
PVER	O	Program Verification During slave or auto programming, PVER is updated after each programming pulse. A high output signal indicates successful programming of a location, while a low signal indicates a detected error. PVER shares a package pin with P2.0 and TXD.

Table 4. Signal Descriptions (Sheet 5 of 6)

Name	Type	Description
RD#	O	Read Read-signal output to external memory. RD# is asserted during external memory reads. RD# shares a package pin with P5.3.
RESET#	I/O	Reset A level-sensitive reset input to, and an open-drain system reset output from, the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown and idle modes, asserting RESET# causes the microcontroller to reset and return to normal operating mode. After a reset, the first instruction fetch is from 2080H.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD shares a package pin with P2.1 and PALE#.
SC1:0	I/O	Clock Pins for SSIO0 and 1 For handshaking transfers, configure SC1:0 as open-drain outputs. This pin carries a signal only during receptions and transmissions. When the SSIO port is idle, the pin remains either high (with handshaking) or low (without handshaking). SC0 shares a package pin with P6.4, and SC1 shares a package pin with P6.6.
SD1:0	I/O	Data Pins for SSIO0 and 1 These pins are the data I/O pins for SSIO0 and 1. For transmissions, configure SD*x* as a complementary output signal. For receptions, configure SD*x* as a high-impedance input signal. SD0 shares a package pin with P6.5, and SD1 shares a package pin with P6.7.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. It is also used in conjunction with T2DIR for quadrature counting mode. T2CLK shares a package pin with P1.0 and EPA0.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. It is also used in conjunction with T2CLK for quadrature counting mode. T2DIR shares a package pin with P1.2 and EPA2.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD shares a package pin with P2.0 and PVER.

Table 4. Signal Descriptions (Sheet 6 of 6)

Name	Type	Description
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{PP}	PWR	Programming Voltage V_{PP} causes the device to exit powerdown mode when it is driven low for at least 50 ns. Use this method to exit powerdown only when using an external clock source because it enables the internal phase clocks, but not the internal oscillator. If you do not plan to use the powerdown feature, connect V_{PP} to V_{CC}.
V_{REF}	PWR	Reference Voltage for the A/D Converter This pin supplies operating voltage to the A/D converter.
V_{SS}, V_{SS1}	GND	Digital Circuit Ground These pins supply ground for the digital circuitry. Connect each V_{SS} and V_{SS1} pin to ground through the lowest possible impedance path. V_{SS} pins are connected to the core ground region of the microcontroller, while V_{SS1} pins are connected to the port ground region. (ANGND is connected to the analog ground region.) Separating the ground regions provides noise isolation.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. Forcing WR# high while RESET# is low causes the device to enter PLL-bypass mode. When the device is in PLL-bypass mode, the internal phase clocks operate at one-half the frequency of the frequency on XTAL1. WR# shares a package pin with P5.2, WRL#, and PLLEN. †When this pin is configured as a special-function signal (P5_MODE.2 = 1), the chip configuration register 0 (CCR0) determines whether it functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRL#	O	Write Low† During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares a package pin with P5.2, WR#, and PLLEN. †When this pin is configured as a special-function signal (P5_MODE.2 = 1), the chip configuration register 0 (CCR0) determines whether it functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

5.0 Address Map

Table 5. Address Map

Hex Address Range	Description	Addressing Modes
FFFF 8000	External device (memory or I/O) connected to address/data bus	Indirect or indexed
7FFF 2080	Program memory (internal nonvolatile or external memory); see Note 1.	Indirect or indexed
207F 2000	Special-purpose memory (internal nonvolatile or external memory)	Indirect or indexed
1FFF 1FE0	Memory-mapped SFRs	Indirect or indexed
1FDF 1F00	Peripheral SFRs	Indirect, indexed, or windowed direct
1EFF 0300	External device (memory or I/O) connected to address/data bus; (future SFR expansion; see Note 2).	Indirect or indexed
02FF 0100	Upper register file (general-purpose register RAM)	Indirect, indexed, or windowed direct
00FF 0000	Lower register file (register RAM, stack pointer, and CPU SFRs)	Direct, indirect, or indexed

NOTES:
1. After a reset, the microcontroller fetches its first instruction from 2080H.
2. The content or function of these locations may change in future microcontroller revisions, in which case a program that relies on a location in this range might not function properly.

6.0 Electrical Characteristics

Note: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 6. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–60°C to +150°C
Voltage from V_{PP} or EA# to V_{SS} or ANGND	–0.5 V to +13.0 V
Voltage from any other pin to V_{SS} or ANGND	–0.5 V to +7.0 V
Power Dissipation	0.5 W

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 7. Operating Conditions

Parameter	Values
T_A (Ambient Temperature Under Bias)	–40°C to +125°C
V_{CC} (Digital Supply Voltage)	4.75 V to 5.25 V
V_{REF} (Analog Supply Voltage) (Notes 1, 2)	4.75 V to 5.25 V
F_{XTAL1} (Input Frequency): - PLL in 2x mode - PLL bypassed	 4 MHz to 10 MHz 8 MHz to 20 MHz

NOTES:
1. ANGND and V_{SS} should be nominally at the same potential.
2. V_{REF} should not exceed V_{CC} by more than 0.5 V.

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

6.1 DC Characteristics

Table 8. DC Characteristics at V_{CC} = 4.75 V to 5.25 V (Sheet 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions (Note 1)
I_{CC}	V_{CC} supply current (-40°C to +125°C ambient)		50	95	mA	F_{XTAL1} = 20 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.25 V (While device is in reset)
I_{CC1}	Active mode supply current (typical)		50		mA	
I_{REF}	A/D reference supply current		2	5	mA	
I_{IDLE}	Idle mode current		15	42	mA	F_{XTAL1} = 20 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.25 V
V_{IL}	Input low voltage (all pins)	0.5 V		0.3 V_{CC}	V	
V_{IH}	Input high voltage (all pins)	0.7 V_{CC}		V_{CC} + 0.5	V	(3)
V_{OL}	Output low voltage (outputs configured as complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA (4) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output high voltage (outputs configured as complementary)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = – 200 µA (4) I_{OH} = – 3.2 mA I_{OH} = – 7.0 mA
I_{LI}	Input leakage current (standard inputs)			± 8	µA	$V_{SS} \le V_{IN} \le V_{CC}$ (5)
I_{LI1}	Input leakage current (port 0—A/D inputs)			± 1	µA	$V_{SS} \le V_{IN} \le V_{REF}$
V_{OL2}	Output low voltage in reset (all pins except P2.6)			1	V	I_{OL} = 15 µA (6, 7)
I_{OL2}	Output low current in reset (all pins except P2.6)	15 30 35		110 185 215	µA µA µA	V_{OL2} = 1.0 V V_{OL2} = 2.5 V V_{OL2} = 4.0 V
R_{RST}	Reset pullup resistor	6 K		65 K	Ω	
V_{OL3}	Output low voltage in reset (RESET# pin only)			0.3 0.5 0.8	V V V	I_{OL3} = 4 mA (7) I_{OL3} = 6 mA I_{OL3} = 10 mA
V_{OL4}	Output low voltage in reset (P2.6 only)			1	V	I_{OL4} = 500 µA

NOTES:
1. Device is static and should operate below 1 Hz, but is tested only down to 4 MHz with the PLL enabled. With the PLL bypassed, the device is tested only down to 8 MHz.
2. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC}$ = 5.25 V.
3. V_{IH} max for port 0 is V_{REF} + 0.5 V.
4. All bidirectional pins when configured as complementary outputs.
5. Standard input pins include XTAL1, EA#, RESET#, and ports 1–6 when configured as inputs.
6. All bidirectional pins except P2.7/CLKOUT, which is excluded because it is not weakly pulled low in reset. Bidirectional pins include ports 1–6.
7. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

Table 8. DC Characteristics at V_{CC} = 4.75 V to 5.25 V (Sheet 2 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions (Note 1)
C_S	Pin capacitance (any pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPD2}	Weak pulldown resistance (all pins except P2.6)		~100 K		Ω	(Note 2)
I_{OL4}	P2.6 only	0.4 1.0 1.2		2.0 3.5 4.0	mA mA mA	V_{OL4} = 1.0 V V_{OL4} = 2.5 V V_{OL4} = 4.0 V
R_{WPD4}	P2.6 only		3 K		Ω	

NOTES:
1. Device is static and should operate below 1 Hz, but is tested only down to 4 MHz with the PLL enabled. With the PLL bypassed, the device is tested only down to 8 MHz.
2. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.25$ V.
3. V_{IH} max for port 0 is V_{REF} + 0.5 V.
4. All bidirectional pins when configured as complementary outputs.
5. Standard input pins include XTAL1, EA#, RESET#, and ports 1–6 when configured as inputs.
6. All bidirectional pins except P2.7/CLKOUT, which is excluded because it is not weakly pulled low in reset. Bidirectional pins include ports 1–6.
7. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

6.2 AC Characteristics (Over Specified Operating Conditions)

6.2.1 Test Condition

- Capacitive load on all pins = 100 pF
- Rise and fall times = 10 ns
- F_{XTAL1} = 8 MHz with PLL enabled in clock-doubler mode

Table 9. AC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units
The 87C196LA meets these specifications				
F_{XTAL1}	Frequency on XTAL1, PLL bypassed	8	20	MHz(1)
	Frequency on XTAL1, PLL in 2x mode	4	10	
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	8	20	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period t = 1/f	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t - 10	t + 20	ns
T_{CLLH}	CLKOUT Falling to ALE Rising	- 10	30	ns
T_{LLCH}	ALE Falling to CLKOUT Rising	- 35	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns
T_{LHLL}	ALE High Period	t - 10	t + 10	ns
T_{AVLL}	Address Setup to ALE Low	t - 15		ns
T_{LLAX}	Address Hold after ALE Low	t - 40		ns
T_{LLRL}	ALE Low to RD# Low	t — 30		ns
T_{RLCL}	RD# Low to CLKOUT Low	0	30	ns
T_{RHLH}	RD# High to ALE Rising	t - 5		ns
T_{RLRH}	RD# Low to RD# High	t	t + 25	ns(3)
T_{RLAZ}	RD# Low to Address Float		10	ns
T_{LLWL}	ALE Low to WR# Low	t - 10		ns
T_{CLWL}	CLKOUT Low to WR# Falling Edge	- 5	25	ns
T_{QVWH}	Data Valid to WR# High	t - 23		ns
T_{CHWH}	CLKOUT High to WR# Rising Edge	- 5	30	ns
T_{WLWH}	WR# Low to WR# High	t - 20		ns
T_{WHQX}	Data Hold after WR# High	t - 25		ns
T_{WHLH}	WR# High to ALE High	t - 10	t + 15	ns(3)
T_{WHAX}	AD15:8 Hold after WR# High	t - 30		ns(4)
T_{RHAX}	AD15:8 Hold after RD# High	t - 30		ns(4)

NOTES:
1. Testing performed at 4.0 MHz with PLL enabled. With the PLL bypassed, the device is tested only down to 8 MHz. However, the device is static by design and typically operates below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 9. AC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units
The system must meet these specifications to work with the 87C196LA				
T_{AVDV}	Address Valid to Input Data Valid		3t - 55	ns
T_{RLDV}	RD# Low to Input Data Valid		t - 22	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		t - 50	ns
T_{RHDZ}	RD# High to Input Data Float		t	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Testing performed at 4.0 MHz with PLL enabled. With the PLL bypassed, the device is tested only down to 8 MHz. However, the device is static by design and typically operates below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

6.2.2 Explanation of AC Symbols

Each symbol is two pairs of letters prefixed by “t” for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 10. AC Timing Symbol Definitions

A	AD15:0
C	CLKOUT
D	AD15:0, AD7:0
L	ALE
Q	AD15:0, AD7:0
R	RD#
W	WR#, WRL#

Character	Condition
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating (low impedance)

Figure 4. System Bus Timing

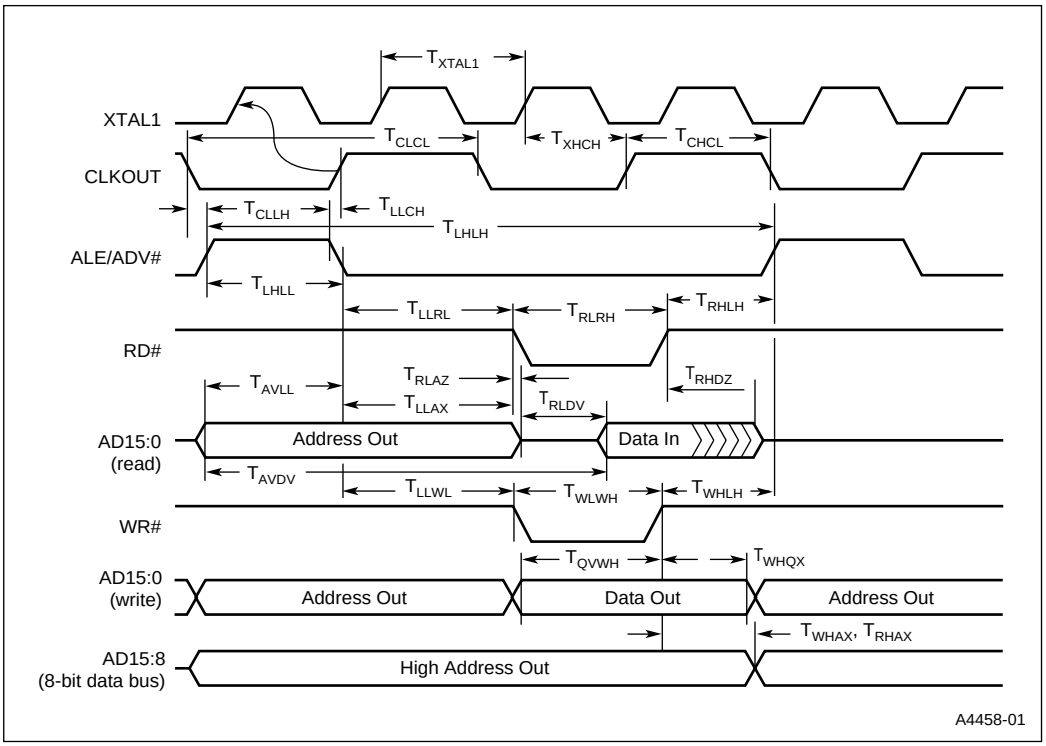


Table 11. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Frequency on X_{TAL1}, PLL bypassed	8	20	MHz(1)
	Frequency on X_{TAL1}, PLL in 2x mode	4	10	
T_{XLXL}	Oscillator Period (T_{OSC})	50	250	ns
T_{XHXX}	High Time	0.35T	0.65T	ns
T_{XLXX}	Low Time	0.35T	0.65T	ns
T_{XLXH}	Rise Time		10	ns
T_{XHLX}	Fall Time		10	ns

1. Testing performed at 4.0 MHz with PLL enabled. With the PLL bypassed, the device is tested only down to 8 MHz. However, the device is static by design and typically operates below 1 Hz.

Figure 5. External Clock Drive Waveform

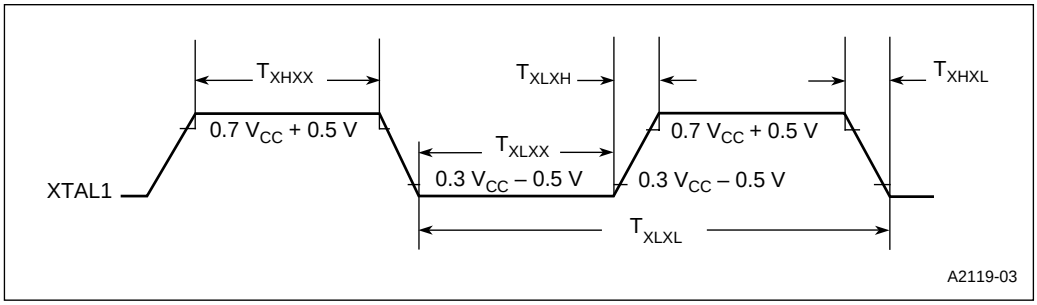


Figure 6. AC Testing Input, Output Waveforms

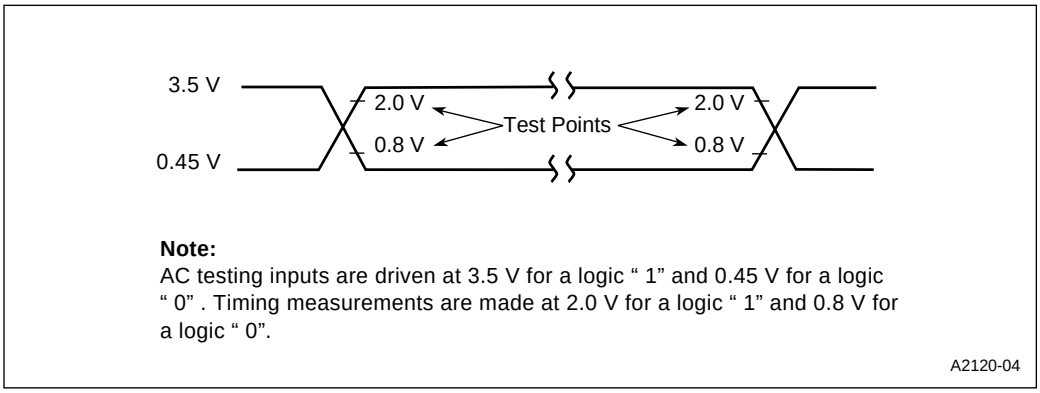
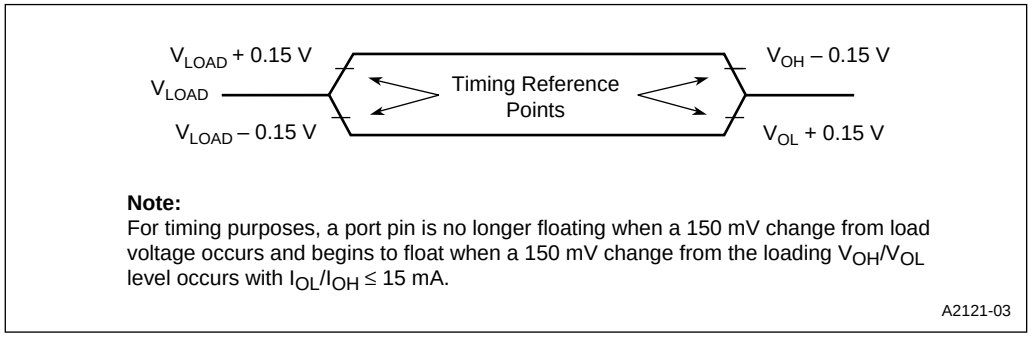


Figure 7. Float Waveform



7.0 EPROM Specifications

7.1 Operating Conditions

- Load Capacitance = 150 pF
- T_C = 25°C ±5°C
- V_{REF} = 5.0 V ±0.25 V
- V_{SS}
- ANGND = 0.0 V
- VPP = 12.5 V ±0.25 V
- EA# = 12.5 V ±0.25 V
- F_{OSC} = 5.0 MHz

Table 12. AC EPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	PALE# Pulse Width	50		T_{OSC}
T_{PLPH}	PROG# Pulse Width[3]	50		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PHLL}	PROG# High to Next PALE# Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	PROG# High to Next PROG# Low	220		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PLDV}	PROG# Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	RESET# High to First PALE# Low	1100		T_{OSC}
T_{PHIL}	PROG# High to AINC# Low	0		T_{OSC}
T_{ILIH}	AINC# Pulse Width	240		T_{OSC}
T_{ILVH}	PVER# Hold after AINC# Low	50		T_{OSC}
T_{ILPL}	AINC# Low to PROG# Low	170		T_{OSC}
T_{PHVL}	PROG# High to PVER# Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5.0 V ±0.25 V, T_C = 25°C ±5°C and V_{PP} = 12.5 V ±0.25 V. For run-time programming over a full operating range, contact factory.
2. Programming Specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use 300 T_{OSC} + 100 µs.

Table 13. DC EPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100	mA

NOTE: V_{PP} must be within 1 V of V_{CC} while V_{CC} <4.5 V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} >4.5 V.

7.2 EPROM Programming Waveforms

Figure 8. Slave Programming Mode Data Program Mode with Single Program Pulse

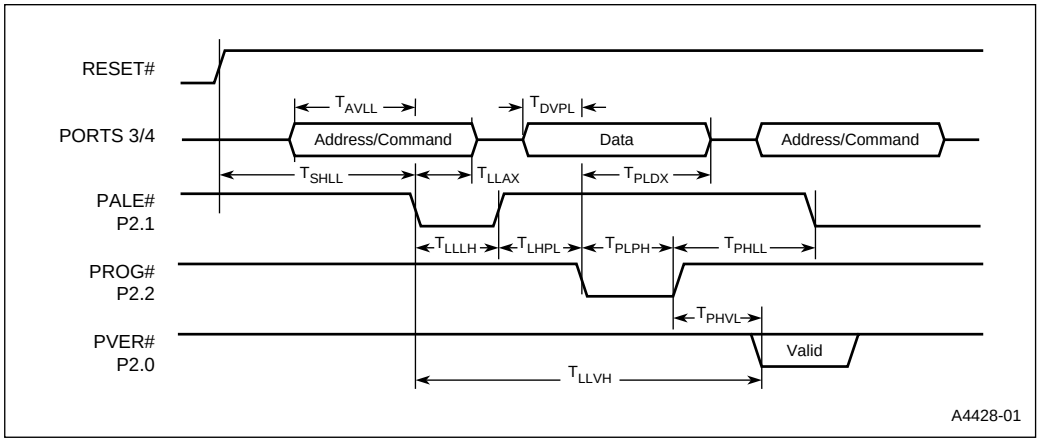


Figure 9. Slave Programming Mode in WORD Dump or Data Verify Mode with Auto Increment

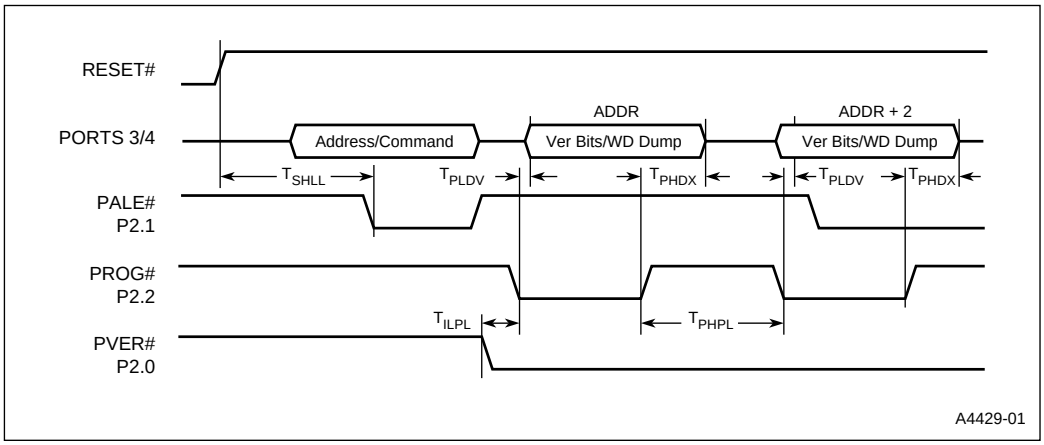
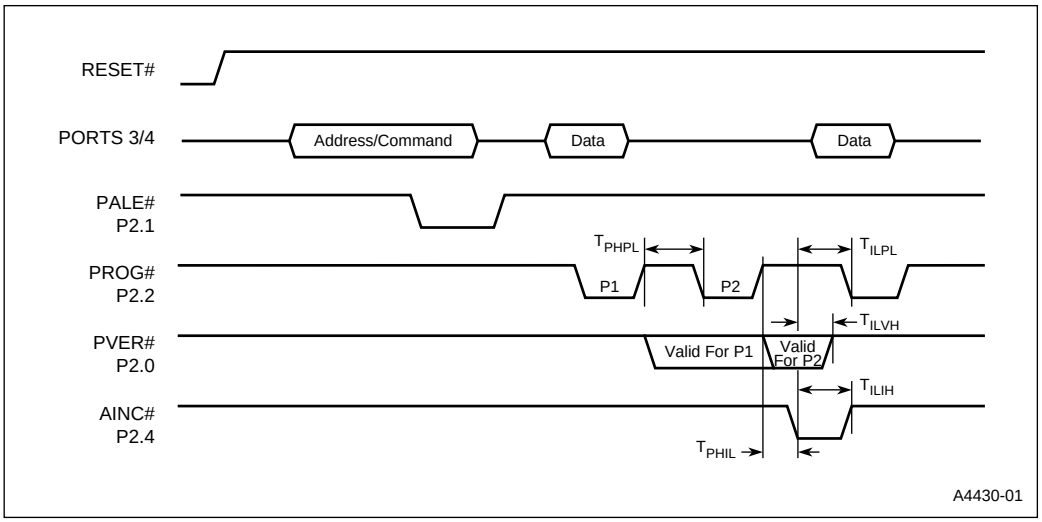


Figure 10. Slave Programming Mode Timing in Data Program Mode with Repeated Program Pulse and Auto Increment



8.0 A/D Converter Specifications

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD_TIME special function register to the appropriate value. The AD_TIME register only programs the speed at which the conversions are performed, not the speed at which it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be within 0.5 V of V_{CC} since it supplies both the resistor ladder and the digital portion of the converter and input port pins.

For testing purposes, after a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12 V and 20 MHz operating frequency.

There is an AD_TEST register that allows for conversion on ANGND and V_{REF}, as well as zero offset adjustment. The absolute error listed is without doing any adjustments.

Table 14. A/D Operating Conditions - Symbol Descriptions[1]

Symbol	Description	Min	Max	Units
T_A	Automotive Ambient Temperature	-40	+125	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25(2,3)	V
T_{SAM}	Sample Time	2.0		µs(4)
T_{CONV}	Conversion Time	15	18	µs(4)
F_{OSC}	Oscillator Frequency	4	20	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5 V.
3. Testing is performed at V_{REF} = 5.12 V.
4. The value of AD_TIME must be selected to meet these specifications.

Table 15. A/D Operating Conditions - Parameter Descriptions

Parameter	Typical†,1	Min	Max	Units‡
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3	LSBs
Full Scale Error	±2			LSBs
Zero Offset Error	±2			LSBs
Non-Linearity			±3	LSBs
Differential Non-Linearity		≥0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	0.009			LSBs/C(1)
Off Isolation		- 60		dB(1,2,3)
Feedthrough	- 60			dB(1,2)
V_{CC} Power Supply Rejection	- 60			dB(1,2)
Input Resistance		750	1.2 K	Ω(1)
DC Input Leakage		0	2	µA

NOTES:
† These values are expected for most parts at 25°C, but are not tested or guaranteed.
‡ An “LSB”, as used here, has a value of approximately 5 mV. (See Automotive Handbook for A/D glossary of terms).
1. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
2. DC to 100 KHz.
3. Multiplexer Break-Make Guaranteed.

9.0 AC Characteristics - Serial Port - Shift Register Mode

9.1 Test Conditions

- T_A = -40°C to +125°C
- V_{CC} = 5.0 V ±5%
- V_{SS} = 0.0 V
- Load Capacitance = 100 pF

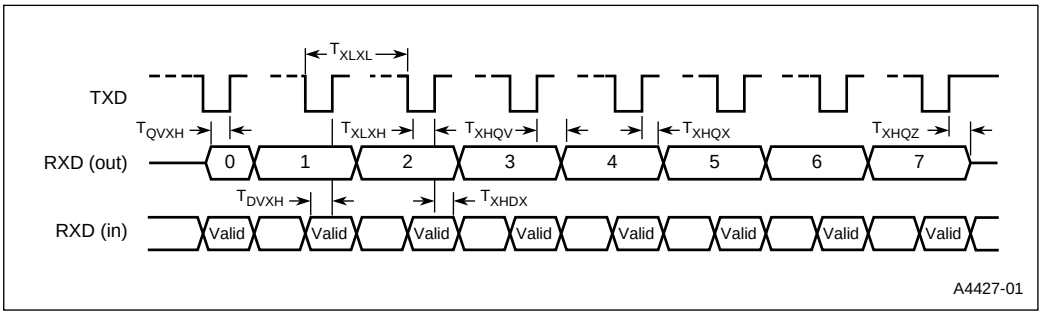
Table 16. Serial Port Timing - Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8T		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4T - 50	4T + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3T		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2T - 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2T + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2T + 200		ns
T_{XHDX}[1]	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}[1]	Last Clock Rising to Output Float		5T	ns

1. Parameter not tested.

9.2 Waveform - Serial Port - Shift Register Mode0

Figure 11. Serial Port Waveform - Shift Register Mode



10.0 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 17. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
xx87C196LA (52-pin PLCC)	42 °C/W	15°C/W

NOTES:
1. θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 foot away from case in static air flow environment.
   θ_{JC} = Thermal resistance between junction and package surface (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ± 2°C/W.
3. Values listed are at a maximum power dissipation of 0.5 W.
4. To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

11.0 Design Considerations

To be supplied.

12.0 Device Errata

Contact your Intel sales representative for this product's specification update.

13.0 Datasheet Revision History

For revision (004), to address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

These revisions were made for the (003) datasheet.

Table 18. Revision History (Sheet 1 of 2)

Revision	Item	Change
002	All	Data sheet moved from Product Preview to Advance Information status.
002	Cover	List of features changed to reflect 24 Kbytes of OTPROM and 768 bytes of register RAM.
002	Figure 3	Modified to include PLLEN designation on pin 6.
002	Table 4	Signal descriptions modified for the PLLEN pin, to reflect the method for bypassing the on-chip PLL.
002	Section 6.0	Changed "PLL in 1x mode" to "PLL bypassed".

Table 18. Revision History (Sheet 2 of 2)

Revision	Item	Change
002	Section 6.1	Changes to DC Characteristics as follows: • I_{CC}Max from TBD to 95 mA • I_{REF}Max from TBD to 5 mA • I_{IDLE}Max from TBD to 42 mA • $_{PD}$Deleted • IHDeleted • I_{OL2} (All pins except P2.6) Min, Max, @ V_{OL2} from TBD to: Min = 15 mAMax = 110 µA@ V_{OL2} = 1.0 V Min = 30 mAMax = 185 µA@ V_{OL2} = 2.5 V Min = 35 mAMax = 215 µA@ V_{OL2} = 4.0 V • R_{WPU} replaced with R_{WPD2} to accurately reflect the weak pulldown device. Typical set to 100 KΩ for all pins except P2.6. • I_{OL2} (Added for P2.6 only) Min = 0.4 mAMax = 2.0 µA@ V_{OL4} = 1.0 V Min = 1.0 mAMax = 3.5 µA@ V_{OL4} = 2.5 V Min = 1.2 mAMax = 4.0 µA@ V_{OL4} = 4.0 V • R_{WPD4} (Added for P2.6 only) To accurately reflect the weak pulldown device for P2.6. Typical set to 3 KΩ.
002	Table 9	Changes to AC Characteristics as follows: • T_{CHCL}Max from T+15 to T+20 ns • T_{CLLH}Max from 15 to 30 ns • T_{LLCH}Min from -20 to -35 ns • T_{RLCL}Min from 4 to 0 • T_{RLAZ}Max from 5 to 10 ns • T_{CHWH}Min from -10 to -5 ns Max from 15 to 30 ns
002	Table 11 and Figure 5	Added External clock drive specifications and waveform.
002	Figure 6	Added AC testing input/output waveform.
002	Figure 7	Added Float Waveform.
002	Section 7.2	Added EPROM specifications for programming characteristics.
002	Section 8.0	Added A/D converter specifications.
002	Section 9.0	Added AC characteristics for the serial port.
003	All	Changed V_{CC} and V_{REF} operating spec conditions.