

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK1283 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low on-state resistance
 $R_{DS(on)} = 0.18 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2 \text{ A)}$
 $R_{DS(on)} = 0.24 \Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 2 \text{ A)}$
- Low C_{iss} $C_{iss} = 500 \text{ pF TYP}$
- Built-in G-S gate protection diode

QUALITY GRADE

Standard

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of quality grade on the devices and its recommended applications.

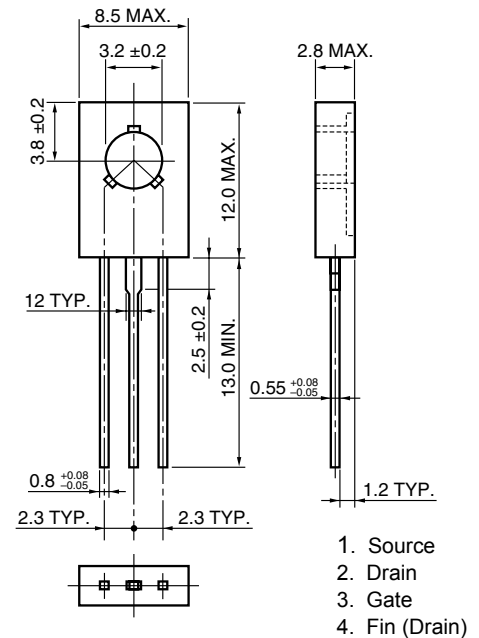
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 3.0	A
Drain Current (pulse)	$I_{D(pulse)}$ ^{Note}	± 12	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.3	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

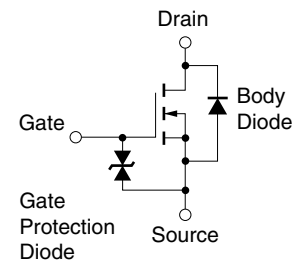
Note $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



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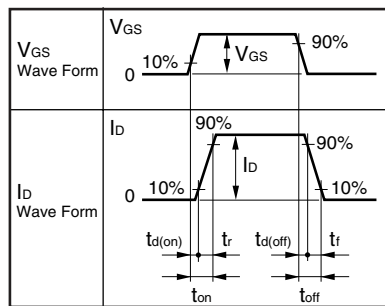
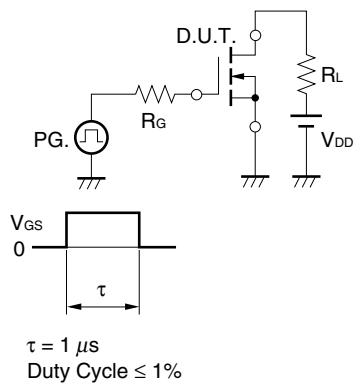
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

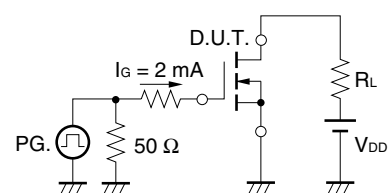
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance Note	R _{DS(on)}		0.15	0.18	Ω	V _{GS} = 10 V, I _D = 2 A
			0.18	0.24	Ω	V _{GS} = 4.0 V, I _D = 2 A
★ Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance Note	y _{fs}	2.4			S	V _{DS} = 10 V, I _D = 2 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 60 V, V _{GS} = 0 V
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{DS} = ±20 V, V _{GS} = 0 V
Input Capacitance	C _{iss}		500		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		200		pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}		40		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		40		ns	V _{GS(on)} = 10 V
Rise Time	t _r		100		ns	V _{DD} = 30 V
Turn-off Delay Time	t _{d(off)}		550		ns	I _D = 2 A, R _G = 10 Ω
Fall Time	t _f		200		ns	R _L = 15 Ω
Total Gate Charge	Q _G		13		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		3		nC	I _D = 3 V
Gate to Drain Charge	Q _{GD}		3		nC	V _{DD} = 48 V
Diode Forward Voltage Note	V _{SD}		0.9		V	I _{SD} = 3 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		140		ns	I _F = 3 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}		700		nC	di/dt = 50 A/μs

Note Pulsed

TEST CIRCUIT 1 SWITCHING TIME

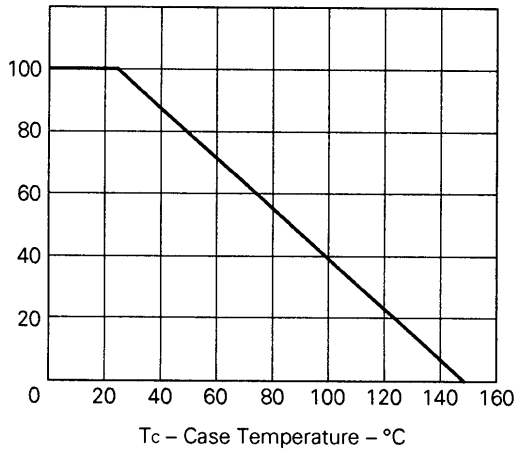


TEST CIRCUIT 2 GATE CHARGE

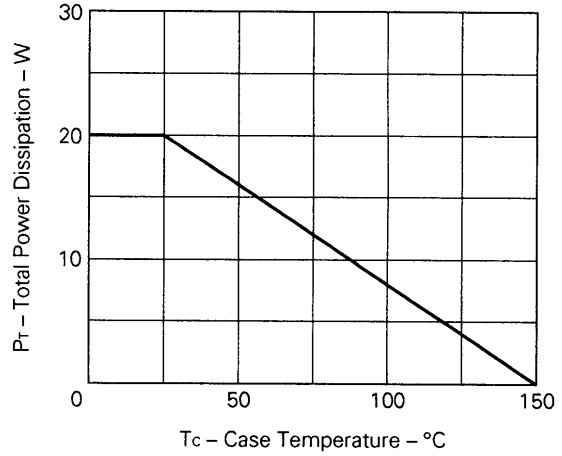


TYPICAL CHARACTERISTICS (T_A = 25°C)

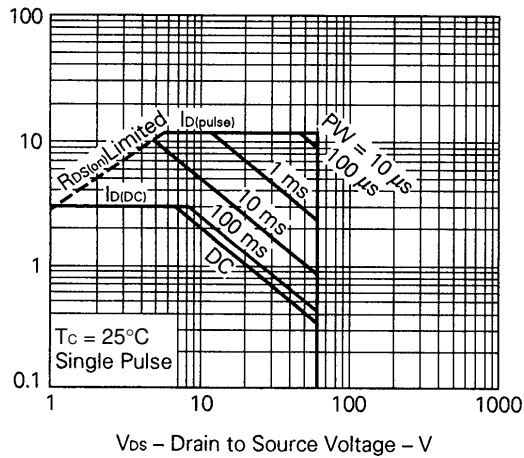
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



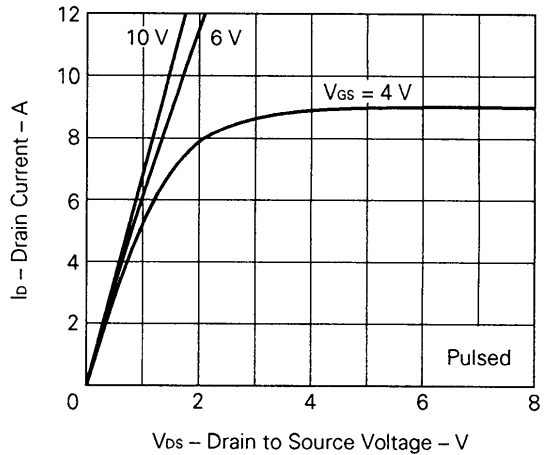
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



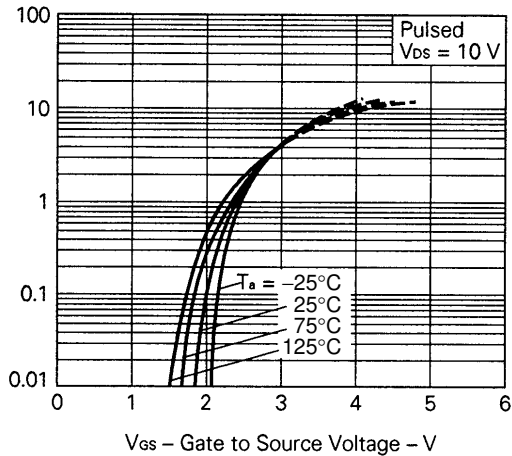
FORWARD BIAS SAFE OPERATING AREA

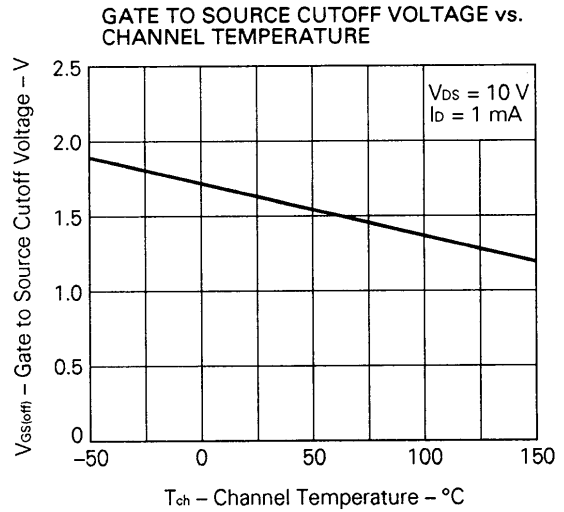
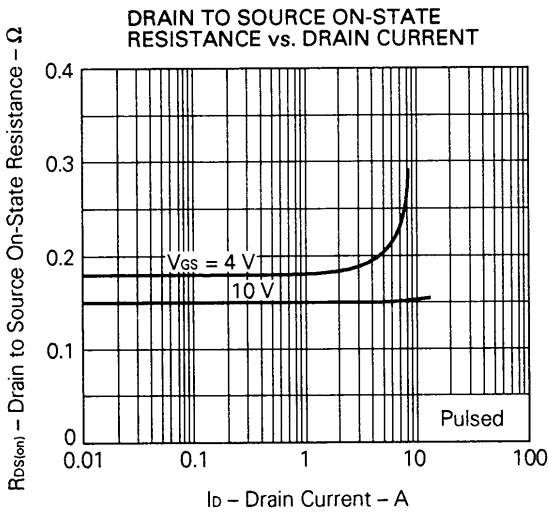
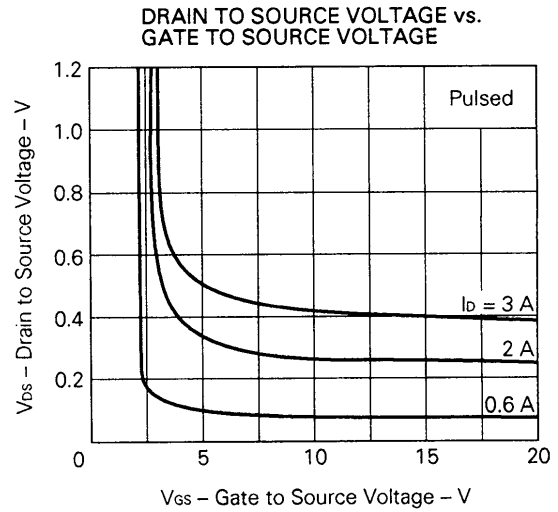
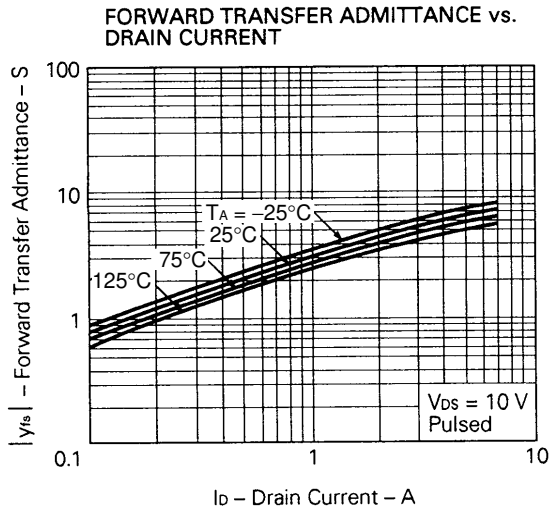
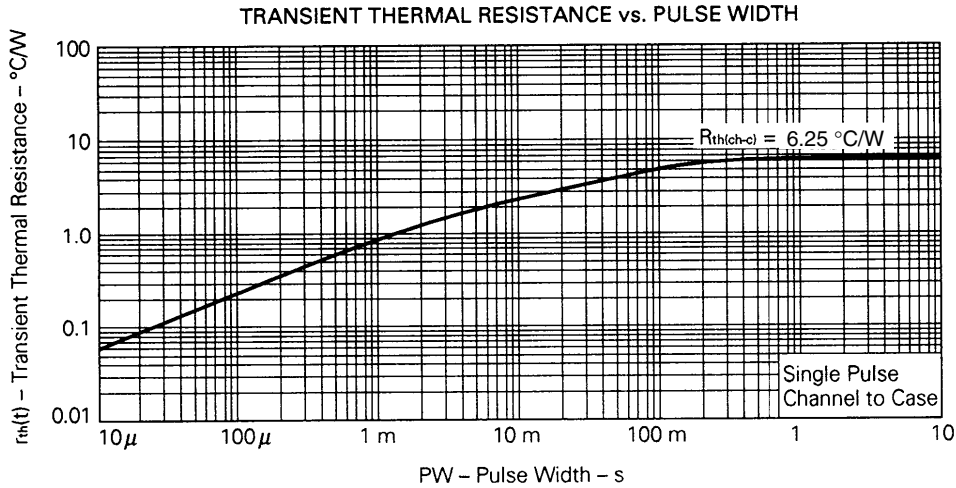


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

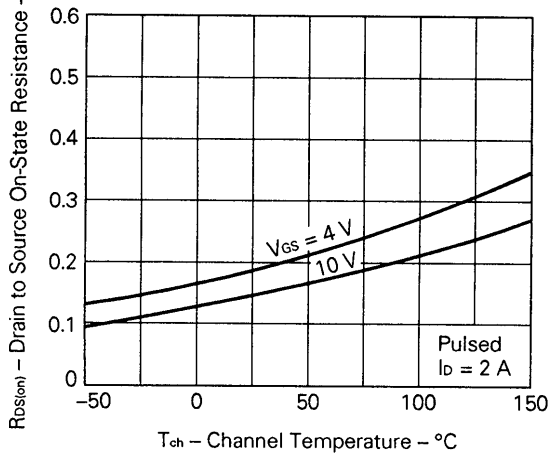


TRANSFER CHARACTERISTICS

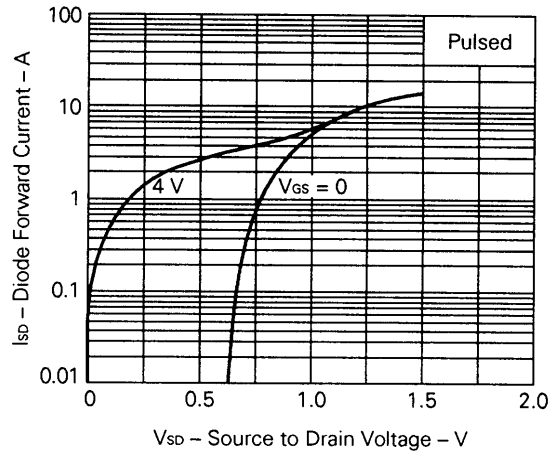




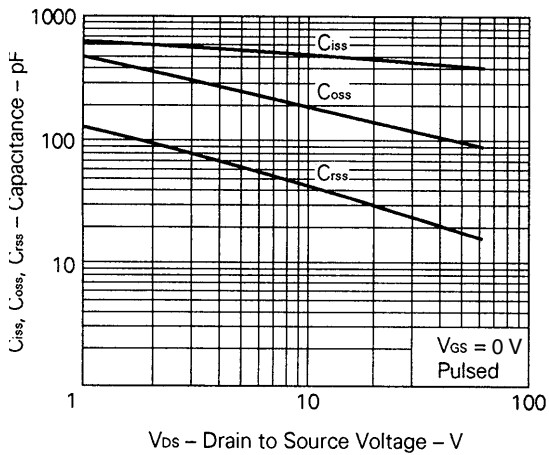
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



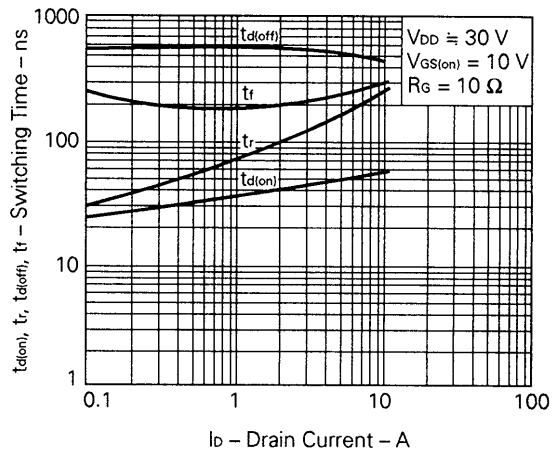
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



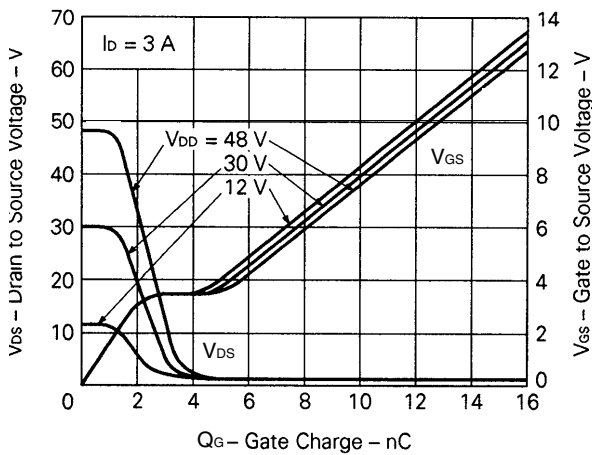
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



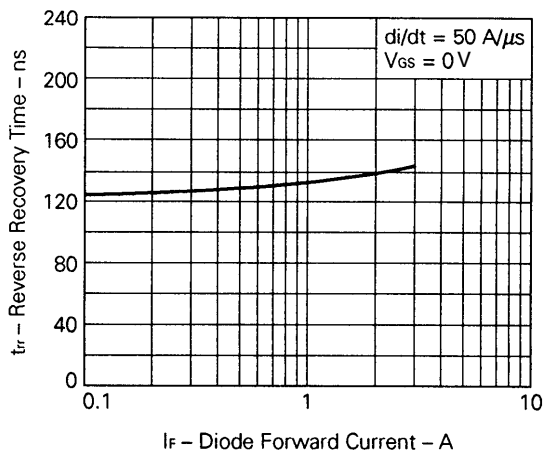
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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