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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# RENESAS

# MOS FIELD EFFECT TRANSISTOR μ **PA2756GR**

### SWITCHING **N-CHANNEL POWER MOS FET**

#### DESCRIPTION

The µ PA2756GR is Dual N-channel MOS Field Effect Transistor designed for switching applications.

#### **FEATURES**

- Low on-state resistance  $R_{DS(on)1} = 105 \text{ m}\Omega \text{ MAX.}$  (Vgs = 10 V, ID = 2.0 A)  $R_{DS(on)2}$  = 150 m $\Omega$  MAX. (Vgs = 4.0 V, ID = 2.0 A)
- Low Ciss: Ciss = 260 pF TYP.
- Built-in G-S protection diode against ESD
- Small and surface mount package (Power SOP8)

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
$\mu$ PA2756GR	Power SOP8

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}C$ )

Drain to Source Voltage (Vgs = 0 V)	VDSS	60
Gate to Source Voltage (VDS = 0 V)	Vgss	±20
Drain Current (DC) Note1	ID(DC)	±4.0
Drain Current (pulse) Note2	D(pulse)	±16
Total Power Dissipation (1 unit) Note1	Pt1	1.6
Total Power Dissipation (2 units) Note1	Pt2	2.0
Channel Temperature	Tch	150
Storage Temperature	Tstg	–55 to +150
Single Avalanche Current Note3	las	4.0
Single Avalanche Energy Note3	Eas	1.6
Repetitive Avalanche Energy Note4	Ear	1.6

Notes 1. Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 2.2 mm

- **2.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V
- **4.** IAR  $\leq$  4.0 A, Tch  $\leq$  150°C
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

V

V А

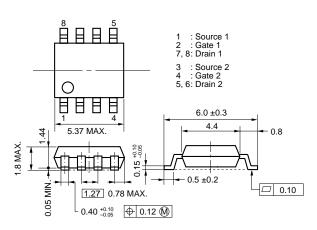
А

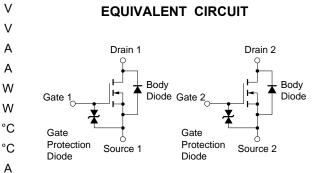
W

А mJ mJ

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### PACKAGE DRAWING (Unit: mm)





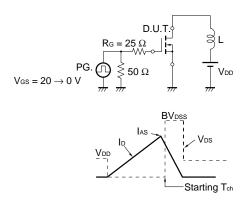
ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ±18 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	<b>y</b> fs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.0 A	2.0			S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A		85	105	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 2.0 A		106	150	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		260		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		65		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		20		pF
Turn-on Delay Time	<b>t</b> d(on)	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.0 A		14		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		5		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 10 Ω		80		ns
Fall Time	tr			30		ns
Total Gate Charge	QG	V <sub>DD</sub> = 48 V		6		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		1		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = 4.0 A		1.5		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 4.0 A, VGS = 0 V		0.9		V
Reverse Recovery Time	trr	IF = 4.0 A, VGS = 0 V		24		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		22		nC

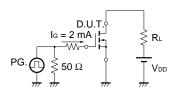
Note Pulsed

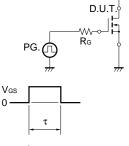
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

#### **TEST CIRCUIT 2 SWITCHING TIME**

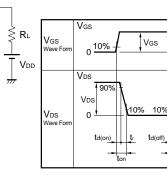


#### TEST CIRCUIT 3 GATE CHARGE





 $\begin{array}{l} \tau = 1 \, \mu s \\ \text{Duty Cycle} \leq 1\% \end{array}$ 



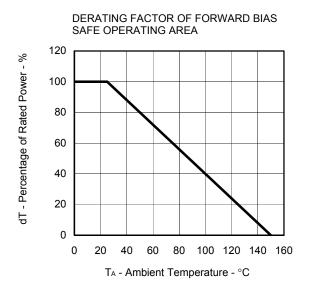
90%

90%

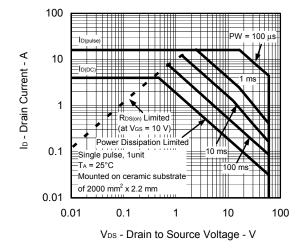
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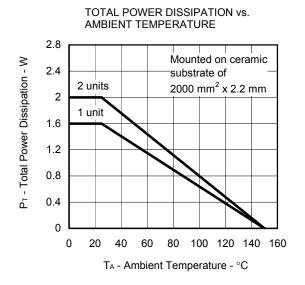
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#### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

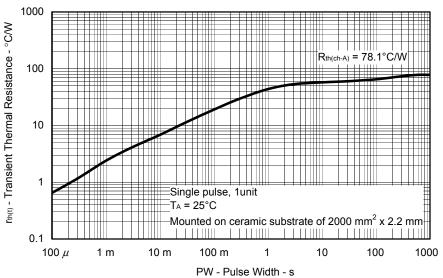


FORWARD BIAS SAFE OPERATING AREA





TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

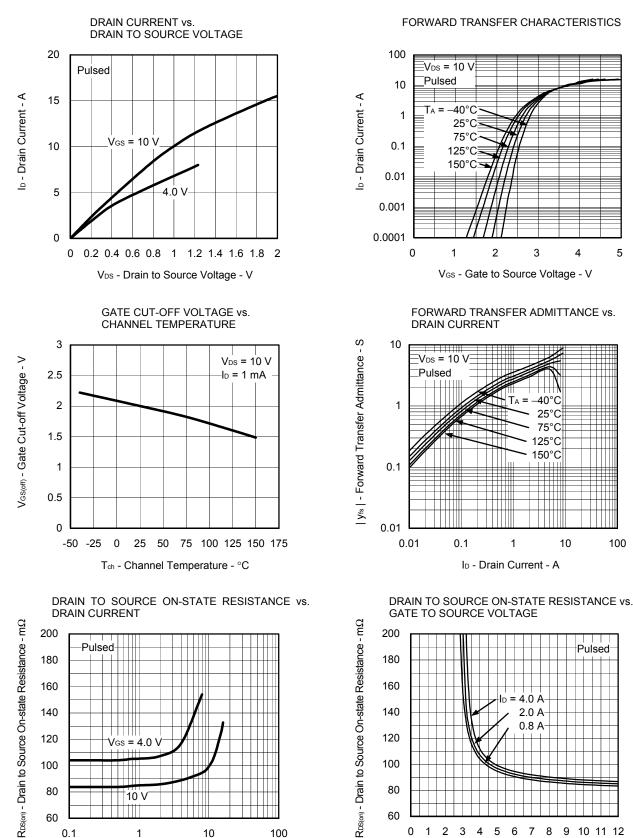


5

100

0.8 A

5 6 7 8 9 10 11 12



#### FORWARD TRANSFER CHARACTERISTICS

100

120

100

80

60

0 1 2

3 4

VGS - Gate to Source Voltage - V

120

100

80

60

0.1

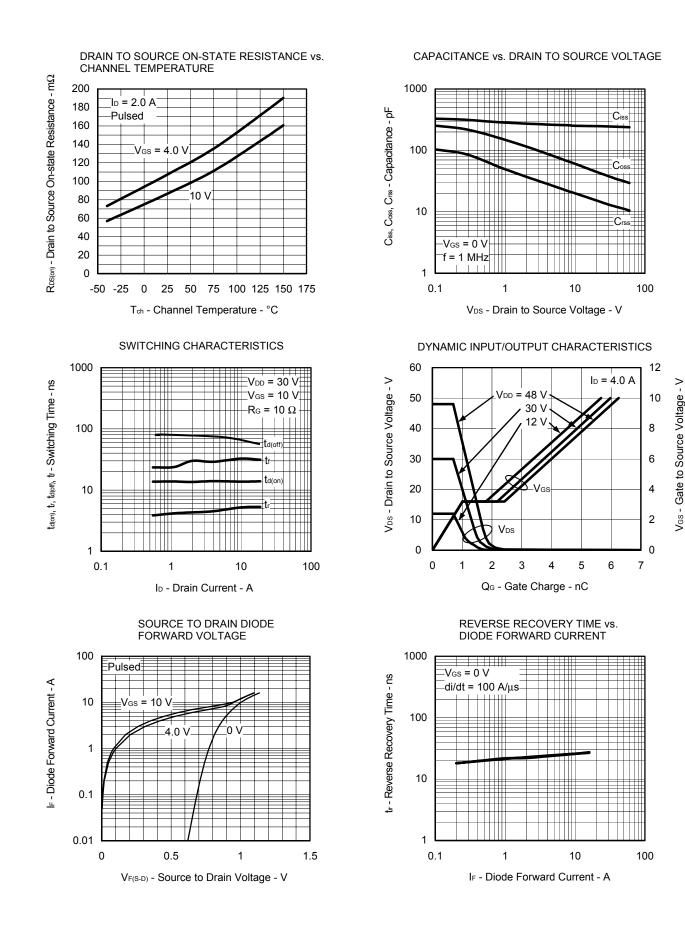
Vgs = 4.0 V +++

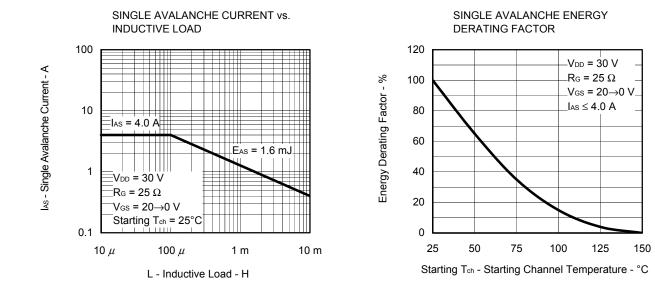
10 V

1

10

ID - Drain Current - A





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