Low Voltage 16-Bit I^2C-bus I/O Expander

Features

- I^2C to 16-bit I/O ports expander
- 1MHz Fast-mode Plus I^2C bus
- Operating voltage range of 1.65V to 5.5V for both I^2C bus and I/O ports
- Four adjustable I^2C slave addresses via ADDR
- I^2C multiple-register group programming with global loop or local loop
- Active low reset input ($\overline{\text{RESET}}$)
- Active low open-drain interrupt output ($\overline{\text{INT}}$)
- Internal power-on reset and I^2C software reset
- Noise filter on SCL/SDA inputs
- Input/Output port configurable
- Input with polarity/latch/pull-up/pull-down/ interrupt functions
- Allowing port input voltage above supply
- Interrupt with trigger/mask/clear/status features
- Programmable input debounce enable/time
- Output with bank/pin selectable push-pull or open-drain
- Bit-wise programmable output drive strength
- Low standby current of 4µA typical at 3.3V
- Maximum 25mA driving capability for each port
- RoHS and Green Compliant

Applications

- Smartphone, Tablet and Wearables
- Laptop and Desktop

Brief Description

KTS1622 is a 16-bit general-purpose I/O expander via the I^2C bus for microcontrollers when additional I/Os are needed while keeping interconnections to the minimum.

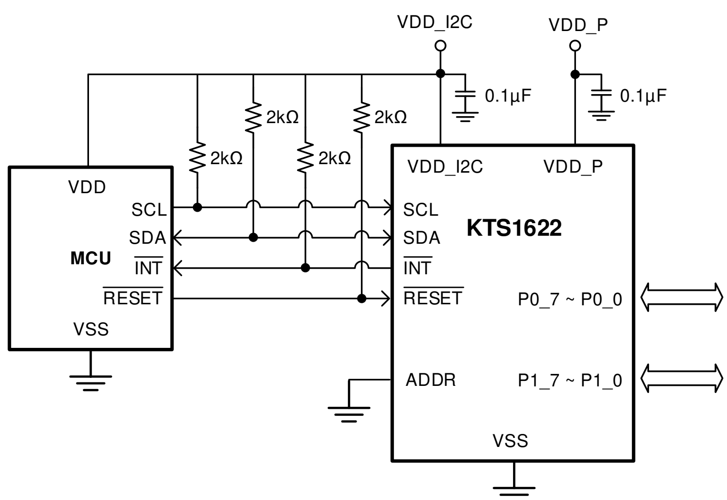
KTS1622 has separate power rails (VDD_I2C and VDD_P) for I^2C bus and I/O ports, both ranging from 1.65V to 5.5V, allowing mixed power system where I^2C bus power is not compatible with I/O port power.

KTS1622 meets the I^2C Fast-mode Plus spec up to 1MHz. External reset input, internal power-on reset and I^2C software reset provide flexible ways to reset the IC. Four adjustable I^2C slave addresses allow multiple KTS1622s in one I^2C bus system.

KTS1622 provides multiple ways to program the 16-bit I/O ports. When the port works as input, it can program the polarity, latch, pull-up, pull-down and interrupt functions. The interrupt function includes the level/edge trigger, mask, clear, status features. For system with noisy input, KTS1622 also provides debounce function with programmable debounce time. When the port works as output, it can program output stage with bank/pin selectable push-pull or open-drain options, it can also program four drive strengths of the output stage to optimize the rise/fall times.

KTS1622 is available in RoHS and Green compliant 25-ball 2.0mm x 2.0mm FO-WLP package and 24-pin 4.0mm x 4.0mm TQFN package.

Typical Application

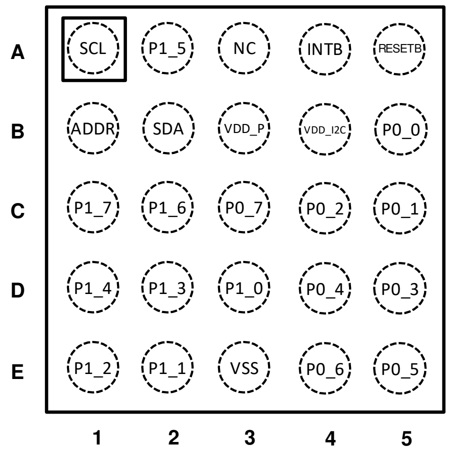


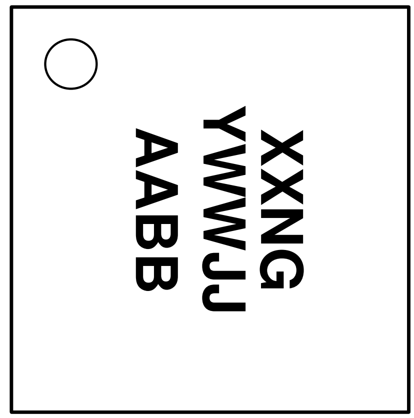
Pin Descriptions

Pin #		Pin Name	Function
FO-WLP55-25	TQFN44-24		
B4	23	VDD_I2C	Power supply pin of the I²C bus
B2	20	SDA	Bi-directional data pin of the I²C interface
A1	19	SCL	Clock input pin of the I²C interface
B3	21	VDD_P	Power supply pin of the I/O ports
B1	18	ADDR	Input pin to program I²C slave address
E3	9	VSS	Ground pin
A5	24	$\overline{\text{RESET}}$	Input pin for active-low reset
A4	22	$\overline{\text{INT}}$	Interrupt open-drain output pin
B5	1	P0_0	Port 0's bit-0 I/O pin
C5	2	P0_1	Port 0's bit-1 I/O pin
C4	3	P0_2	Port 0's bit-2 I/O pin
D5	4	P0_3	Port 0's bit-3 I/O pin
D4	5	P0_4	Port 0's bit-4 I/O pin
E5	6	P0_5	Port 0's bit-5 I/O pin
E4	7	P0_6	Port 0's bit-6 I/O pin
C3	8	P0_7	Port 0's bit-7 I/O pin
D3	10	P1_0	Port 1's bit-0 I/O pin
E2	11	P1_1	Port 1's bit-1 I/O pin
E1	12	P1_2	Port 1's bit-2 I/O pin
D2	13	P1_3	Port 1's bit-3 I/O pin
D1	14	P1_4	Port 1's bit-4 I/O pin
A2	15	P1_5	Port 1's bit-5 I/O pin
C2	16	P1_6	Port 1's bit-6 I/O pin
C1	17	P1_7	Port 1's bit-7 I/O pin
A3	NC	NC	No connection

FO-WLP55-25

Top View



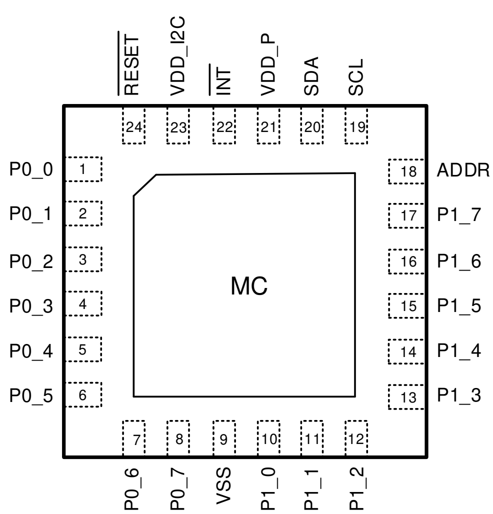


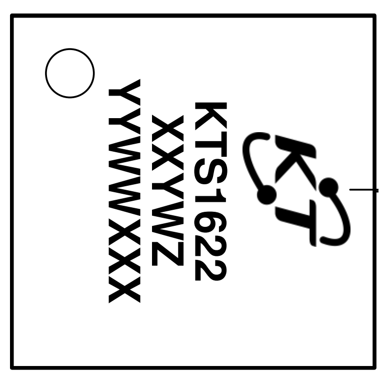
25-Bump 2.0mm x 2.0mm x 0.8mm
FO-WLP55-25 Package

Top Mark
XX = Device Code, NG = Manufacturing Code
YWW = Date Code, JJ = Lot Code
AABB = Serial Number

TQFN44-24

Top View





24-Lead 4.0mm x 4.0mm x 0.75mm
TQFN44-24 Package

Top Mark
KT Logo
KTS1622 = Part Number
XX = Device Code, YWZ = Date Code
YY = Assembly Year, WW = Assembly Week, XXX = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	MIN	MAX	Unit
VDD_I2C	I²C bus power supply voltage	-0.5	6.5	V
VDD_P	Port power supply voltage	-0.5	6.5	V
Px_x	I/O port voltages	-0.5	6.5	V
SCL, SDA, $\overline{RESET}$, ADDR	Control voltages	-0.5	6.5	V
$\overline{INT}$	Output voltage	-0.5	6.5	V
I_{IK}	Input clamp current at SCL/$\overline{RESET}$/ADDR		±20	mA
I_{OK}	Output clamp current at $\overline{INT}$		±20	mA
I_{IOK}	Input/output clamp current at all I/O ports and SDA		±20	mA
I_{OL1}	Output low current at all I/O ports		50	mA
I_{OL2}	Output low current at $\overline{INT}$/SDA		25	mA
I_{OH}	Output high current at all I/O ports		25	mA
I_{DD1}	Continue current through VSS		200	mA
I_{DD2}	Continue current through VDD_P		160	mA
I_{DD3}	Continue current through VDD_I2C		10	mA
T_J	Junction Operating Temperature Range	-40	125	°C
T_S	Storage Temperature Range	-65	150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)		300	°C
ESD	HBM Electrical Static Discharge		2.0	kV

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
VDD_I2C	I²C bus power supply voltage	1.65	5.5	V
VDD_P	Port power supply voltage	1.65	5.5	V
V_{IH1}	High-level input voltage at SCL/SDA	0.7 x VDD_I2C	VDD_I2C	V
V_{IH2}	High-level input voltage at $\overline{RESET}$/ADDR	0.7 x VDD_I2C	5.5	V
V_{IH3}	High-level input voltage at all I/O ports	0.7 x VDD_P	5.5	V
V_{IL1}	Low-level input voltage at SCL/SDA/$\overline{RESET}$/ADDR	-0.3	0.3 x VDD_I2C	V
V_{IL2}	Low-level input voltage at all I/O ports	-0.3	0.3 x VDD_P	V
I_{OH}	High-level output current at all I/O ports		10	mA
I_{OL}	Low-level output current at all I/O ports		25	mA
T_A	Operating ambient temperature	-40	85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Thermal Capabilities[2]

Symbol	Description	Value	Unit
	FO-WLP55-25		
θ_{JA}	Thermal Resistance – Junction to Ambient	82.6	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1211	mW
$\Delta P_D/\Delta T$	Derating Factor Above $T_A = 25°C$	-12.11	mW/°C
	TQFN44-24		
θ_{JA}	Thermal Resistance – Junction to Ambient	30.2	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	3310	mW
$\Delta P_D/\Delta T$	Derating Factor Above $T_A = 25°C$	-33.1	mW/°C

Ordering Information

Part Number	Marking[3]	Operating Temperature	Package
KTS1622EWAA-TR	NMNGYWWJJAABB	-40°C to +85°C	FO-WLP55-25
KTS1622EUAA-TR	NMYWZYYWWXXX	-40°C to +85°C	TQFN44-24

2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

3. “NMNGYWWJJAABB” is the device code, manufacturing code, date code, lot code, serial number. “NMYWZYYWWXXX” is the device code, date code, assembly year, assembly week and serial number.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while Typ values are specified at room temperature (25°C). VDD_P = 3.6V and VDD_I2C = 1.8V.

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Diode Clamp Voltage	I_I = -18mA	-1.2			V
V_{POR}	Power On Reset Voltage on VDD_P			1.28	1.5	V
V_{OH}	Port High Level Output Voltage at 10mA and Full Drive Strength	VDD_P = 1.65V	1.1			V
		VDD_P = 2.3V	1.7			V
		VDD_P = 3V	2.5			V
		VDD_P = 4.5V	4.0			V
V_{OL}	Port Low Level Output Voltage at 10mA and Full Drive Strength	VDD_P = 1.65V			0.5	V
		VDD_P = 2.3V			0.3	V
		VDD_P = 3V			0.25	V
		VDD_P = 4.5V			0.2	V
I_{OL}	Low Level Output Current	SDA: V_{OL} = 0.4V, VDD_I2C = 1.65V to 5.5V	15			mA
		$\overline{INT}$: V_{OL} = 0.4V, VDD_P = 1.65V to 5.5V	3			mA
I_I	Input Current	ADDR/SCL/SDA/$\overline{RESET}$: V_I = VDD_I2C or VSS	-1		1	µA
I_{IH}	Port High Level Input Current	Port: V_I = VDD_P = 1.65V to 5.5V	-1		2.8	µA
I_{IL}	Port Low Level Input Current	Port: V_I = VSS, VDD_P = 1.65V to 5.5V	-1		1	µA
I_{DD}	Supply Current through VDD_P and VDD_I2C SDA = $\overline{RESET}$ = VDD_I2C, ADDR = VDD_I2C or VSS, SCL with Input Clock	VDD_P = 3.6V to 5.5V, Port = VDD_P, f_{SCL} = 0kHz		7	13	µA
		VDD_P = 2.3V to 3.6V, Port = VDD_P, f_{SCL} = 0kHz		4	8.5	µA
		VDD_P = 1.65V to 2.3V, Port = VDD_P, f_{SCL} = 0kHz		2.6	6	µA
		VDD_P = 3.6V to 5.5V, Port = VDD_P, f_{SCL} = 400kHz		18	29	µA
		VDD_P = 2.3V to 3.6V, Port = VDD_P, f_{SCL} = 400kHz		10	17	µA
		VDD_P = 1.65V to 2.3V, Port = VDD_P, f_{SCL} = 400kHz		6	12	µA
		VDD_P = 3.6V to 5.5V, Port = VDD_P, f_{SCL} = 1MHz		36	55	µA
		VDD_P = 2.3V to 3.6V, Port = VDD_P, f_{SCL} = 1MHz		20	30	µA
		VDD_P = 1.65V to 2.3V, Port = VDD_P, f_{SCL} = 1MHz		12	20	µA
		Pull-ups Enabled, Port = VSS, f_{SCL} = 0kHz, VDD_P = 1.65V to 5.5V		0.93	1.5	mA
ΔI_{DD}	Additional Quiescent Current	ADDR/SCL/SDA/$\overline{RESET}$: One Input at VDD_I2C -0.6V, Other Inputs at VDD_I2C or VSS			5	µA
		Port: One Input at VDD_P-0.6V, Other Inputs at VDD_P or VSS			25	µA
R_{PU}	Internal Pull-down Resistance		50	100	150	KΩ
R_{PD}	Internal Pull-up Resistance		50	100	150	KΩ
I²C-Compatible Timing Specifications (SCL, SDA), see Figure 1						
t_1	SCL Clock Period		1			µs
t_2	Data in setup time to SCL high		50			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)		0.26			µs
t_5	SDA high hold time after SCL high (Stop)		0.26			µs

4. Device is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

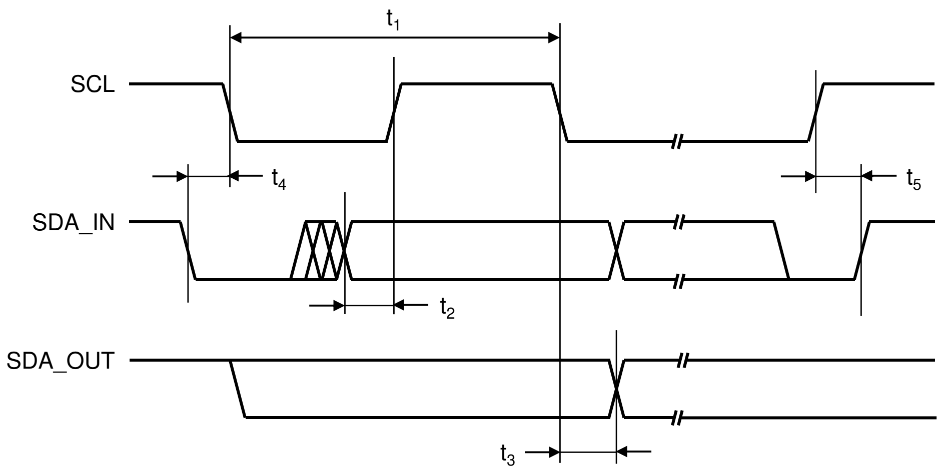
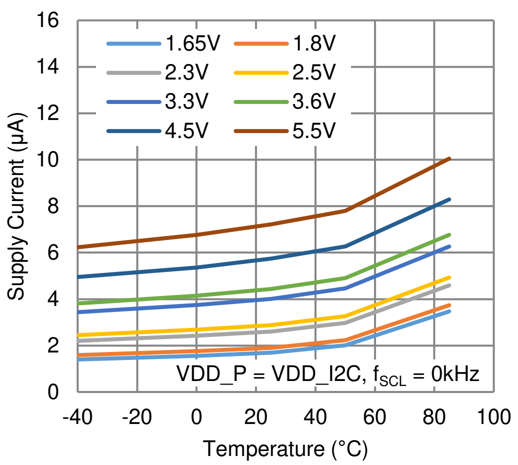


Figure 1. I²C Compatible Interface Timing

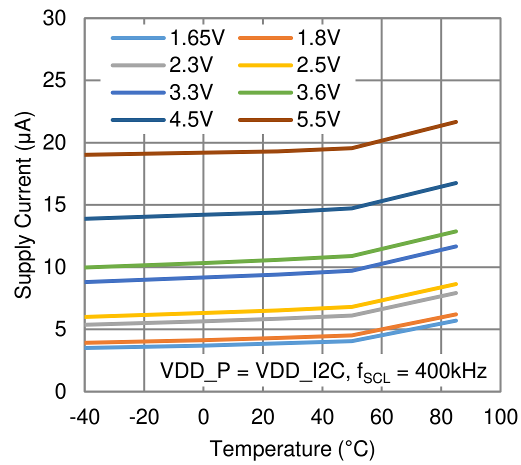
Typical Characteristics

VDD_P = 3.6V and VDD_I2C = 1.8V, C_{VDD_P} = 0.1µF, C_{VDD_I2C} = 0.1µF. T_A = 25°C unless otherwise specified.

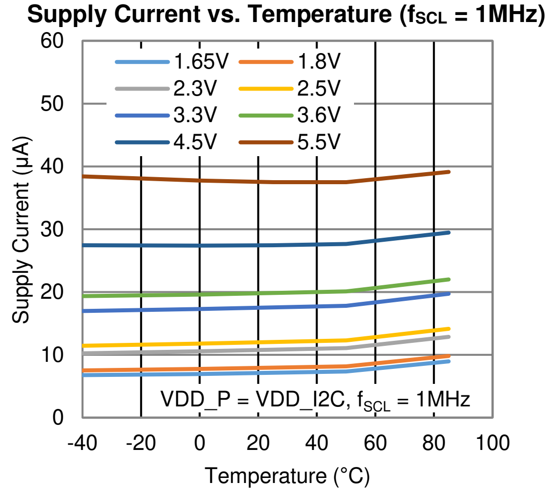
Supply Current vs. Temperature (f_{SCL} = 0kHz)



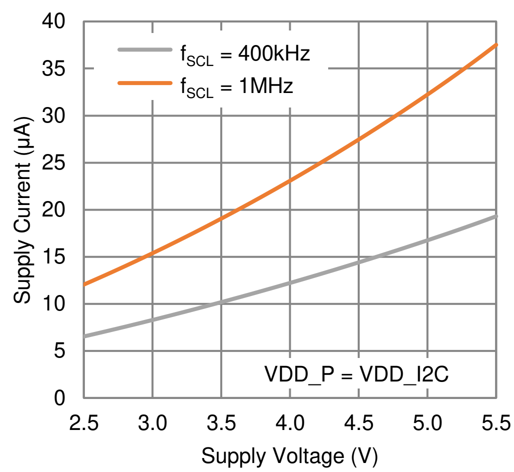
Supply Current vs. Temperature (f_{SCL} = 400kHz)



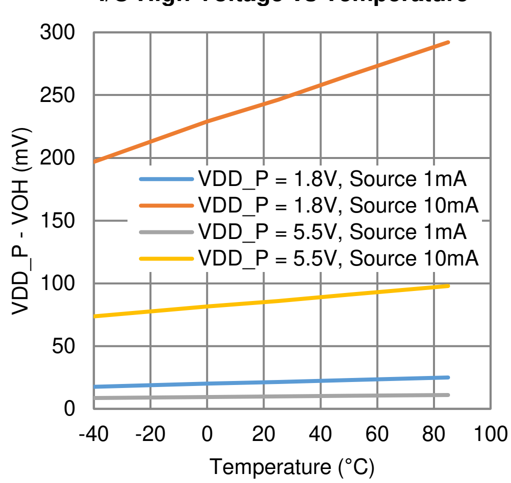
Supply Current vs. Temperature (f_{SCL} = 1MHz)



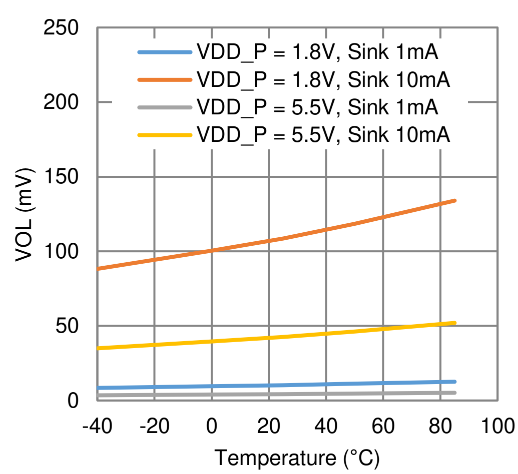
Supply Current vs. Supply Voltage



I/O High Voltage vs Temperature



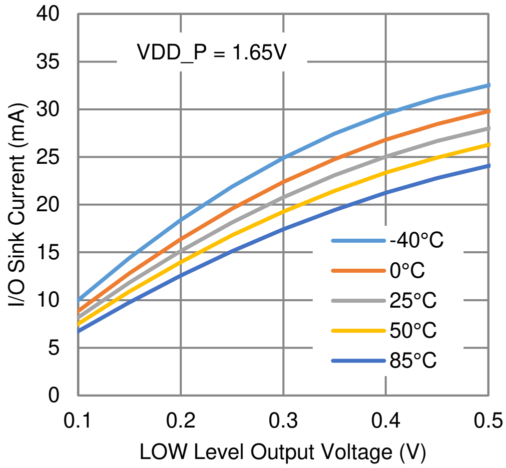
I/O Low Voltage vs Temperature



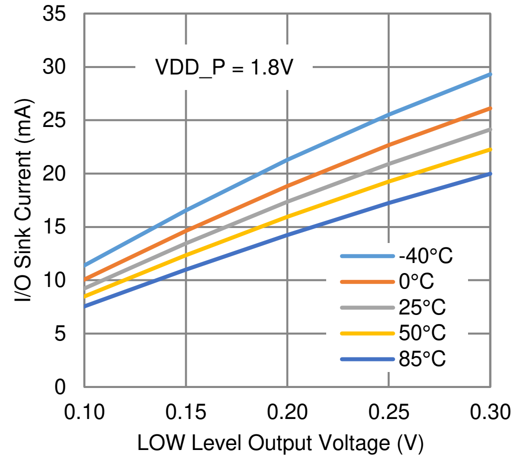
Typical Characteristics

VDD_P = 3.6V and VDD_I2C = 1.8V, C_{VDD_P} = 0.1µF, C_{VDD_I2C} = 0.1µF. T_A = 25°C unless otherwise specified.

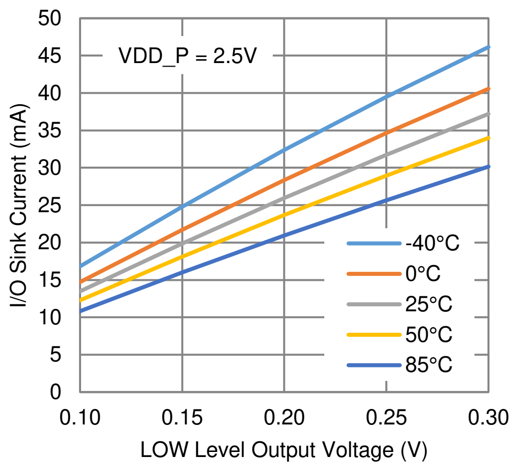
I/O Sink Current vs LOW-level Output Voltage (1.65V)



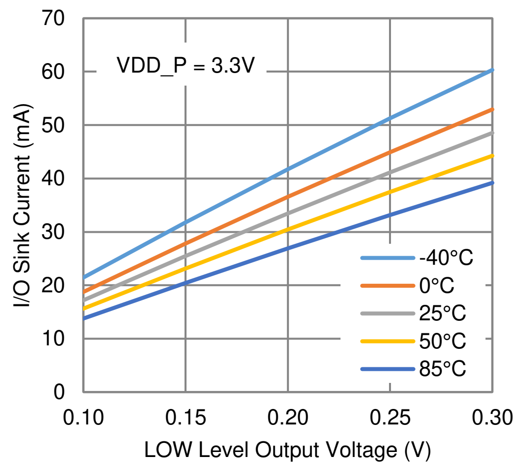
I/O Sink Current vs LOW-level Output Voltage (1.8V)



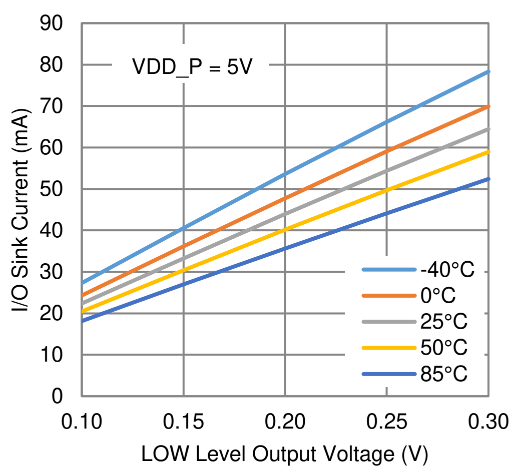
I/O Sink Current vs LOW-level Output Voltage (2.5V)



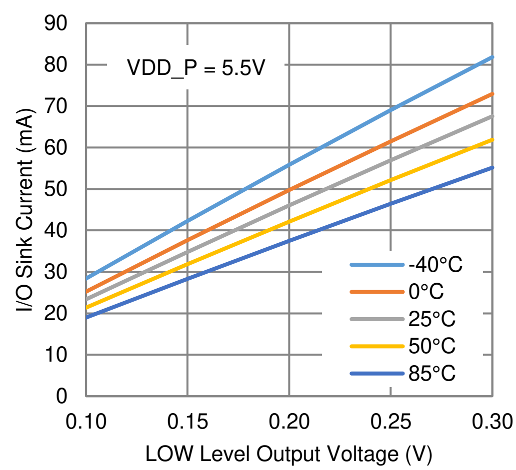
I/O Sink Current vs LOW-level Output Voltage (3.3V)



I/O Sink Current vs LOW-level Output Voltage (5V)



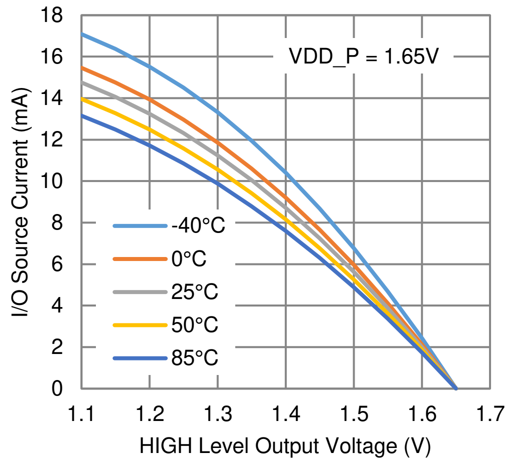
I/O Sink Current vs LOW-level Output Voltage (5.5V)



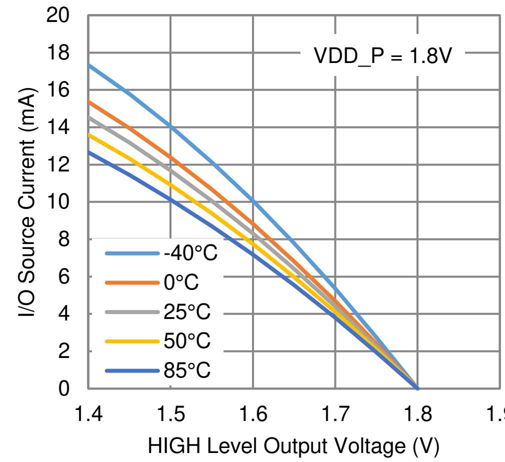
Typical Characteristics

VDD_P = 3.6V and VDD_I2C = 1.8V, C_{VDD_P} = 0.1µF, C_{VDD_I2C} = 0.1µF. T_A = 25°C unless otherwise specified.

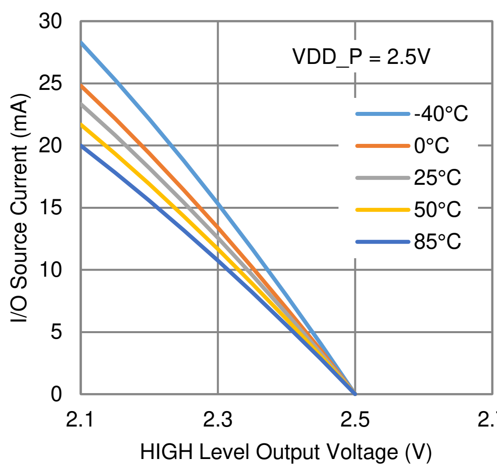
I/O Source Current vs HIGH-level Output Voltage (1.65V)



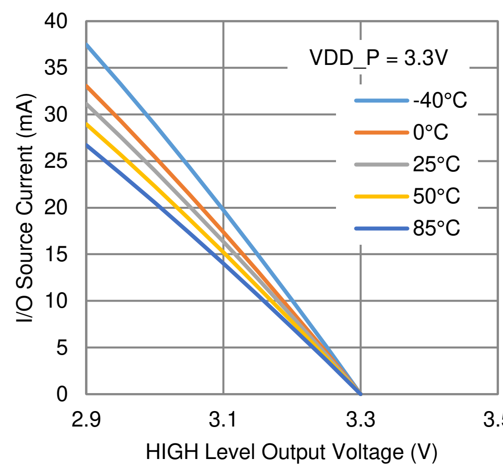
I/O Source Current vs HIGH-level Output Voltage (1.8V)



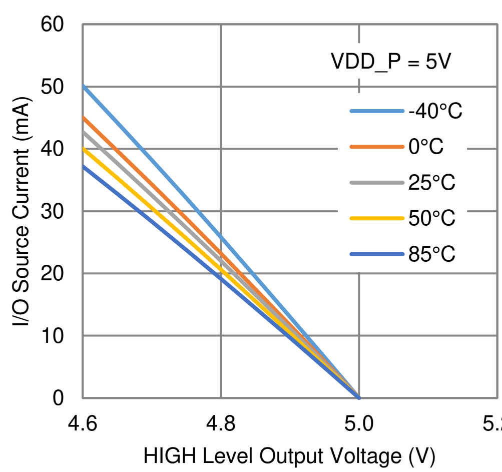
I/O Source Current vs HIGH-level Output Voltage (2.5V)



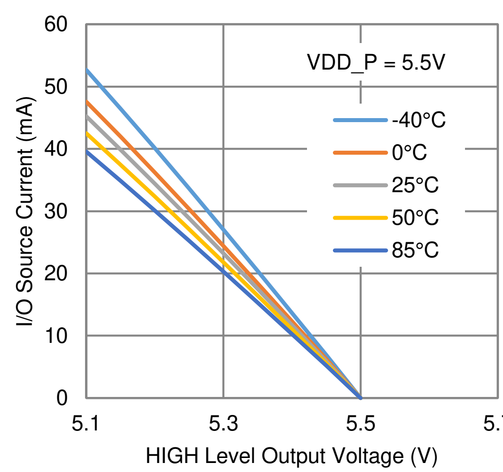
I/O Source Current vs HIGH-level Output Voltage (3.3V)



I/O Source Current vs HIGH-level Output Voltage (5V)



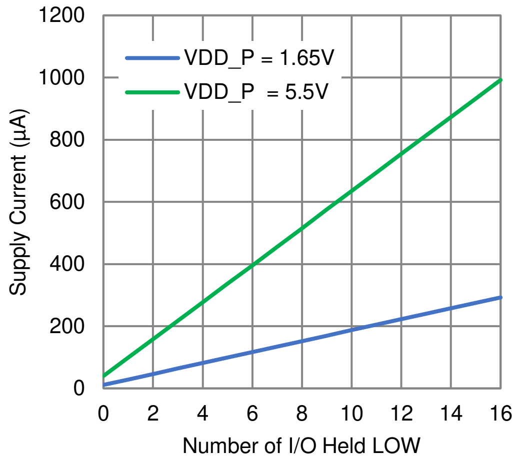
I/O Source Current vs HIGH-level Output Voltage (5.5V)



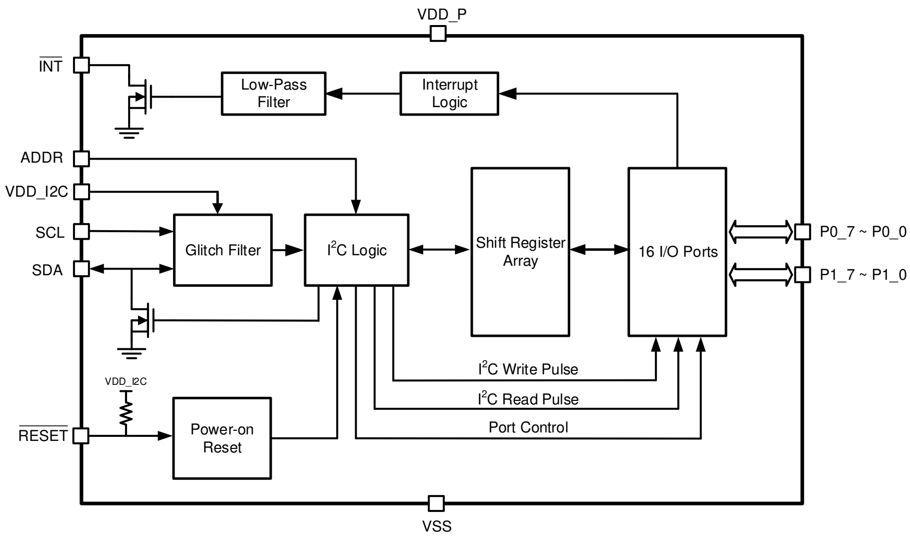
Typical Characteristics

VDD_P = 3.6V and VDD_I2C = 1.8V, C_{VDD_P} = 0.1µF, C_{VDD_I2C} = 0.1µF. T_A = 25°C unless otherwise specified.

Supply Current vs Number of I/O Held LOW (Pull-up Resistors Enabled)



Block Diagram



Functional Description

KTS1622 is a 16-bit general-purpose I/O expander via the I²C bus, it has two input power rails. VDD_I2C provides the power for the I²C bus pins (SCL/SDA), VDD_P provides the power for all the IO ports and other internal circuits.

Power-on Reset

When the supply voltage at VDD_P pin is below power-on reset threshold, the IC is kept in power-on reset condition, all the I²C registers are cleared to their default setting and the interrupt output $\overline{\text{INT}}$ is also reset. This happens when the IC is powered on or through the power-reset cycle.

External Reset ($\overline{\text{RESET}}$)

The active-low input pin $\overline{\text{RESET}}$ can also be used to reset the IC, all the I²C registers are cleared to their default setting and the interrupt output $\overline{\text{INT}}$ is also reset. An external pull-up resistor between $\overline{\text{RESET}}$ and VDD_I2C is suggested to enable the IC. If $\overline{\text{RESET}}$ pin is left floating, an internal pull-up resistor also enables the IC.

I²C Serial Data Bus

KTS1622 supports Fast-mode Plus I²C bus protocol, with speed up to 1MHz.

A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. KTS1622 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate), a fast mode (400kHz maximum clock rate) and a fast-mode plus (1MHz maximum clock rate) are defined. KTS1622 works in all modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 2:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

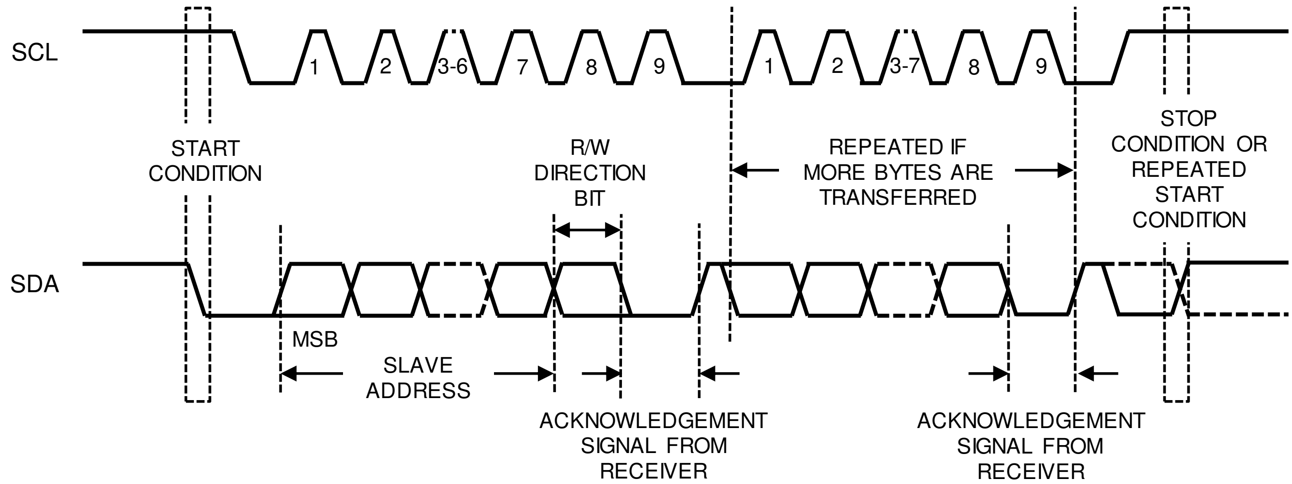


Figure 2. Data Transfer on I²C Serial Bus

Bus Not Busy
Both data and clock lines remain HIGH.

Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle
For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of ‘0’ for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 3 shows the sequence of the I²C write cycle.

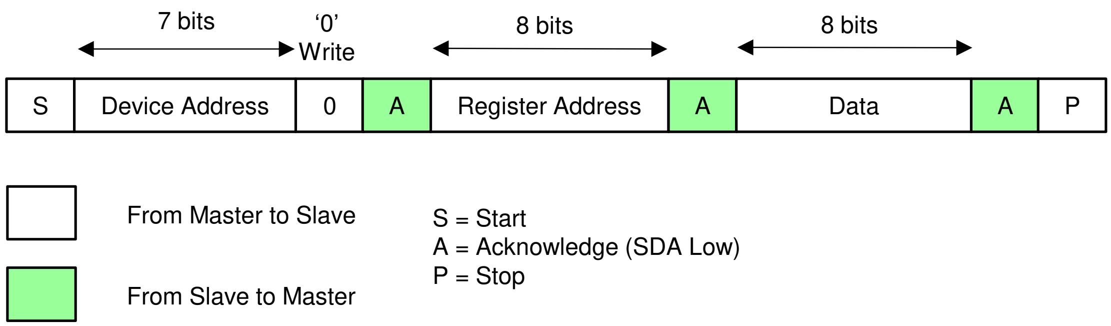


Figure 3. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 4 shows the steps of the I²C read cycle.

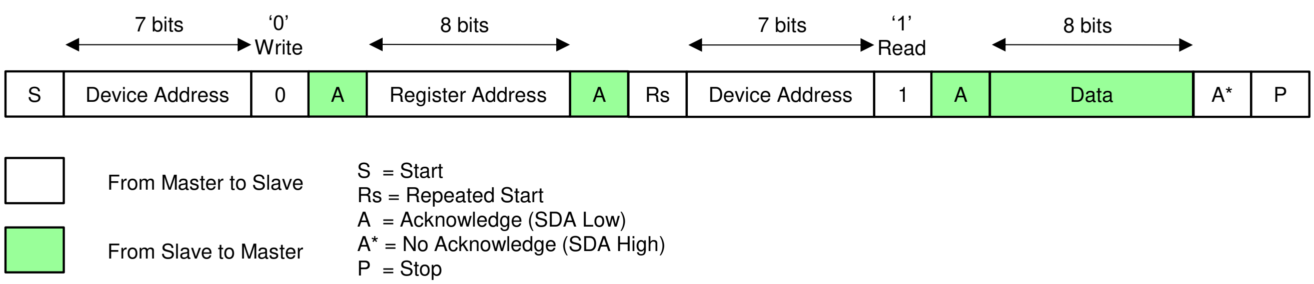


Figure 4. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

I²C Device Address

KTS1622 has four programmable I²C device addresses, controlled by ADDR pin's connection, this allows up to four KTS1622 ICs to share the same I²C bus. Table 1 shows the four 7-bit I²C device addresses depending on ADDR's connection to SCL, SDA, VSS or VDD_I2C. The first 5 bits are fixed as '01000', the last 2 bits are programmable. The device address is detected at each I²C start.

Table 1. I²C Device Address Map

ADDR	7-Bit I²C Device Address						
	A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
VSS	0	1	0	0	0	0	0
VDD_I2C	0	1	0	0	0	0	1
SCL	0	1	0	0	0	1	0
SDA	0	1	0	0	0	1	1

I²C Software Reset

The I²C software reset provides another way to reset the IC without triggering VDD_P power-on reset or using external reset pin RESETb. The following procedure defines the I²C software reset steps:

- Master generates start condition.
- Master sends 7-bit reserved device address '0000000' and 1-bit data direction '0' for write.
- Slave only sends acknowledge after seeing both the device address and write bit above. Otherwise, no acknowledge is generated.
- Master sends 8-bit data '06h'.
- Slave sends acknowledge after seeing the 8-bit data '06h'. If the data is not '06h', slave doesn't acknowledge. If master continues to send more than 1-byte data, slave doesn't acknowledge any more.
- Master generates stop condition to finish the write cycle. After that, slave resets all I²C registers to their default setting and resets the interrupt output $\overline{INT}$. If master sends a repeated start instead, slave doesn't reset.

Figure 5 shows the steps of I²C software reset.

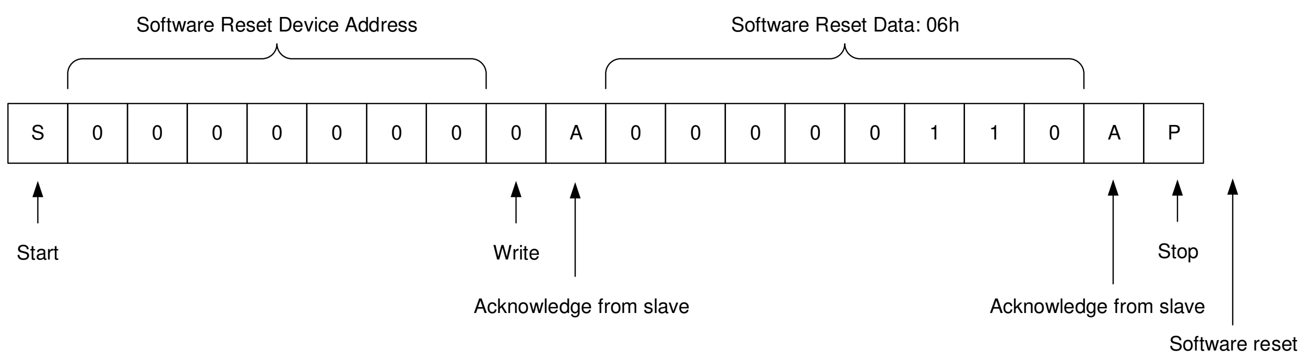


Figure 5. I²C Software Reset

Multiple-register Group Programming

For the 8-bit I²C register address, KTS1622 uses the lowest 7 bits as register address, and uses the highest one bit to define how the multiple-register group is programmed (global loop or local loop).

When the highest one bit is '0', the lowest 7-bit register address is automatically incremented globally for multiple-register I²C read or write until I²C stop comes. All the reserved registers are skipped during the incrementation. After the last register (address = 5Ch) is read or write, the address will move back to the first register (address = 00h). This allows user to program multiple I²C registers sequentially within one I²C command, this is defined as global loop programming.

When the highest one bit is '1', the lowest 7-bit register address is only incremented within the same register group for multiple-register I²C read or write until I²C stop comes. After the last register of that group is read or write, the address will move back to the first register of that group. Most of the register group includes 2 registers. There are two special 4-register groups with the address of 40h~43h and 50h~53h, one special 3-register group with the address of 5Ah~5Ch, and one special 1-register group with the address of 4Fh. This allows user to program multiple I²C registers in the same register group sequentially within one I²C command, this is defined as local loop programming.

If only one register needs to be read or write, the highest one bit can be '0' or '1'. There is no acknowledge when reading or writing the reserved registers.

I²C Register Map

Table 2 summarizes the 36 I²C registers. They can be reset to default values by power-on reset, toggling $\overline{\text{RESET}}$ pin or I²C software reset.

Table 2. I²C Register Map

7-bit Register Address (Bin)							7-bit Register Address (Hex)	Register	Read/Write	Default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	read only	xxxxxxxx
0	0	0	0	0	0	1	01h	Input port 1	read only	xxxxxxxx
0	0	0	0	0	1	0	02h	Output port 0	read/write	11111111
0	0	0	0	0	1	1	03h	Output port 1	read/write	11111111
0	0	0	0	1	0	0	04h	Polarity inversion port 0	read/write	00000000
0	0	0	0	1	0	1	05h	Polarity inversion port 1	read/write	00000000
0	0	0	0	1	1	0	06h	Configuration port 0	read/write	11111111
0	0	0	0	1	1	1	07h	Configuration port 1	read/write	11111111
-	-	-	-	-	-	-	08h to 3Fh	reserved	reserved	reserved
1	0	0	0	0	0	0	40h	Output drive strength port 0A	read/write	11111111
1	0	0	0	0	0	1	41h	Output drive strength port 0B	read/write	11111111
1	0	0	0	0	1	0	42h	Output drive strength port 1A	read/write	11111111
1	0	0	0	0	1	1	43h	Output drive strength port 1B	read/write	11111111
1	0	0	0	1	0	0	44h	Input latch port 0	read/write	00000000
1	0	0	0	1	0	1	45h	Input latch port 1	read/write	00000000
1	0	0	0	1	1	0	46h	Pull-up/pull-down enable port 0	read/write	00000000
1	0	0	0	1	1	1	47h	Pull-up/pull-down enable port 1	read/write	00000000
1	0	0	1	0	0	0	48h	Pull-up/pull-down selection port 0	read/write	11111111
1	0	0	1	0	0	1	49h	Pull-up/pull-down selection port 1	read/write	11111111
1	0	0	1	0	1	0	4Ah	Interrupt mask port 0	read/write	11111111
1	0	0	1	0	1	1	4Bh	Interrupt mask port 1	read/write	11111111
1	0	0	1	1	0	0	4Ch	Interrupt status port 0	read only	00000000
1	0	0	1	1	0	1	4Dh	Interrupt status port 1	read only	00000000
1	0	0	1	1	1	0	4Eh	reserved	reserved	reserved
1	0	0	1	1	1	1	4Fh	Output port configuration	read/write	00000000
1	0	1	0	0	0	0	50h	Interrupt edge port 0A	read/write	00000000
1	0	1	0	0	0	1	51h	Interrupt edge port 0B	read/write	00000000
1	0	1	0	0	1	0	52h	Interrupt edge port 1A	read/write	00000000
1	0	1	0	0	1	1	53h	Interrupt edge port 1B	read/write	00000000
1	0	1	0	1	0	0	54h	Interrupt clear port 0	write only	00000000
1	0	1	0	1	0	1	55h	Interrupt clear port 1	write only	00000000
1	0	1	0	1	1	0	56h	Input status port 0	read only	xxxxxxxx
1	0	1	0	1	1	1	57h	Input status port 1	read only	xxxxxxxx
1	0	1	1	0	0	0	58h	Individual pin output port 0 configuration	read/write	00000000
1	0	1	1	0	0	1	59h	Individual pin output port 1 configuration	read/write	00000000
1	0	1	1	0	1	0	5Ah	Switch debounce enable port 0	read/write	00000000

7-bit Register Address (Bin)							7-bit Register Address (Hex)	Register	Read/Write	Default
B6	B5	B4	B3	B2	B1	B0				
1	0	1	1	0	1	1	5Bh	Switch debounce enable port 1	read/write	00000000
1	0	1	1	1	0	0	5Ch	Switch debounce count	read/write	00000000
-	-	-	-	-	-	-	5Dh to 7Fh	reserved	reserved	reserved

Input Port Registers (00h, 01h)

The Input Port Registers (registers 00h, 01h) reflect the incoming logic levels of the pins. The Input port registers are read only, writes to these registers have no effect and the transaction will be acknowledged (ACK). The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 04h, 05h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 4Fh and registers 58h, 59h), the input port value is forced to 0.

After reading input port registers, all interrupts will be cleared.

Table 3. Input Port 0 Register (Address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 4. Input Port 1 Register (Address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Output Port Registers (02h, 03h)

The Output Port Registers (registers 02h, 03h) show the outgoing logic levels of the pins defined as outputs by the Configuration Registers. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Table 5. Output Port 0 Register (Address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 6. Output Port 1 Register (Address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Polarity Inversion Registers (04h, 05h)

The Polarity Inversion Registers (registers 04h, 05h) allow polarity inversion of pins defined as inputs by the Configuration Registers. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained.

Table 7. Polarity Inversion Port 0 Register (Address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 8. Polarity Inversion Port 1 Register (Address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Configuration Registers (06h, 07h)

The Configuration Registers (registers 06h, 07h) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as an input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Table 9. Configuration Port 0 Register (Address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 10. Configuration Port 1 Register (Address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Output Drive Strength Registers (40h, 41h, 42h, 43h)

The Output Drive Strength Registers (registers 40h, 41h, 42h, 43h) control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41h CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25x, 01b = 0.5x, 10b = 0.75x or 11b = 1x of the drive capability of the I/O.

Table 11. Output Drive Strength Port 0A Register (Address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 12. Output Drive Strength Port 0B Register (Address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 13. Output Drive Strength Port 1A Register (Address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 14. Output Drive Strength Port 1B Register (Address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Input Latch Registers (44h, 45h)

The Input Latch Registers (registers 44h, 45h) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 00h, 01h). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read ‘1’. The next read of the input port register bit 4 register should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level.

Table 15. Input Latch Port 0 Register (Address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 16. Input Latch Port 1 Register (Address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Pull-up/Pull-down Enable Registers (46h, 47h)

The Pull-up and Pull-down Enable Registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs. Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor.

Table 17. Pull-up/Pull-down Enable Port 0 Register (Address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 18. Pull-up/Pull-down Enable Port 1 Register (Address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

Pull-up/Pull-down Selection Registers (48h, 49h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100kΩ with minimum of 50kΩ and maximum of 150kΩ.

Table 19. Pull-up/Pull-down Selection Port 0 Register (Address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 20. Pull-up/Pull-down Selection Port 1 Register (Address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Interrupt Mask Registers (4Ah, 4Bh)

Interrupt Mask Registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted. When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted.

Table 21. Interrupt Mask Port 0 Register (Address 4Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 22. Interrupt Mask Port 1 Register (Address 4Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Interrupt Status Registers (4Ch, 4Dh)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0.

Table 23. Interrupt Status Port 0 Register (Address 4Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 24. Interrupt Status Port 1 Register (Address 4Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Output Port Configuration Register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull. A logic 1 configures the I/O as open-drain and the recommended command sequence is to program this register (4Fh) before the Configuration Register (06h, 07h) sets the port pins as outputs.

ODEN0 configures P0_x, ODEN1 configures P1_x.

Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (58h, 59h).

A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

Table 25. Output Port Configuration Register (Address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

Interrupt Edge Registers (50h, 51h, 52h, 53h)

The Interrupt Edge Registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (4Ah, 4Bh). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{\text{INT}}$ output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input Port Register (00h, 01h) which can be latched with a corresponding '1' set in the Input Latch Register (44h, 45h). If the Interrupt Edge Register entry is set to 11b, any edge, positive or negative, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the Input Latch Register (44h, 45h). These edged interrupts can be cleared in a number of ways: Reading Input Port Registers (00h, 01h); setting the Interrupt Mask Register (4Ah, 4Bh) to 1 (masked); setting the Interrupt Clear Register (54h, 55h) to 1 (this is a write-only register); resetting the Interrupt Edge Register (50h to 53h) back to 0.

Table 26. Interrupt Edge Port 0A Register (Address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 27. Interrupt Edge Port 0B Register (Address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 28. Interrupt Edge Port 1A Register (Address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 29. Interrupt Edge Port 1B Register (Address 53h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 30. Interrupt Edge Bits (IEx.x)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive (rising) edge triggered interrupt
1	0	negative (falling) edge triggered interrupt
1	1	any edge (positive or negative) triggered interrupt

Interrupt Clear Registers (54h, 55h)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{\text{INT}}$ will be cleared. After writing a logic 1 the bit returns to logic 0.

Table 31. Interrupt Clear Port 0 Register (Address 54h)

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 32. Interrupt Clear Port 1 Register (Address 55h)

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Input Status Registers (56h, 57h)

The read-only input status registers function exactly like Input Port 0, 1 (00h, 01h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration Register (06h, 07h), and is also configured as open-drain (register 4Fh and 58h, 59h), the read for that pin will always return 0, otherwise that state of that pin is returned.

Table 33. Input Status Port 0 Register (Address 56h)

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

Table 34. Input Status Port 1 Register (Address 57h)

Bit	7	6	5	4	3	2	1	0
Symbol	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Individual Pin Output Configuration Registers (58h, 59h)

The Individual Pin Output Configuration Registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration Register (4Fh).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (4Fh), the IOCRx, and finally the Configuration Register (06h, 07h) to set the pins as outputs.

Table 35. Individual Pin Output Configuration Register 0 (Address 58h)

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 36. Individual Pin Output Configuration Register 1 (Address 59h)

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Switch Debounce Enable Registers (5Ah, 5Bh)

The Switch Debounce Enable Registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin.

Table 37. Switch Debounce Enable Port 0 Register (Address 5Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 38. Switch Debounce Enable Port 1 Register (Address 5Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

Switch Debounce Count Register (5Ch)

The Switch Debounce Count Register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time (for example, the debounce time will be 10µs if this register is set to 0Ah and external oscillator frequency is 1MHz). The switch debounce logic is disabled if this register is set to 00h.

Table 39. Switch Debounce Count Register (Address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

Interrupt Output ($\overline{\text{INT}}$)

The interrupt output $\overline{\text{INT}}$ has an open-drain structure and requires pull-up resistor to VDD_P or VDD_I2C depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

- The GPIO must be configured as an input port by writing "1" to Configuration Port Registers (06h, 07h).
- The Interrupt Mask Registers (4Ah, 4Bh) must set to "0" to unmask interrupt sources.
- The Interrupt Edge Registers (50h to 53h) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The Input Latch Registers (44h, 45h) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and $\overline{\text{INT}}$ pin de-asserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from $\overline{\text{RESET}}$ pin, or I^2C software reset
- Read Input Port Registers (00h, 01h)
- Write logic 1 to Interrupt Clear Registers (54h, 55h)
- Write logic 1 to Interrupt Mask Registers (4Ah, 4Bh)
- Write logic 0 to Configuration Registers (06h, 07h) and set pin as output port
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in Interrupt Edge Registers

Switch Debounce

Mechanical switches do not make clean make-or-break connections and the contacts can ‘bounce’ for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The KTS1622 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0_1 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration.

Figure 6 shows the typical opening and closing switch debounce operation timing. To use the debounce circuitry, set the port pins (P0_1 to P0_7, and P1_0 to P1_7) with switches attached in the Switch Debounce Enable 0 and 1 registers (5Ah, 5Bh). Connect an external oscillator signal on P0_0, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (5Ch). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period or t_{DP} in Figure 6. Note that all debounce counters will use the same time base and count, but they all function independently.

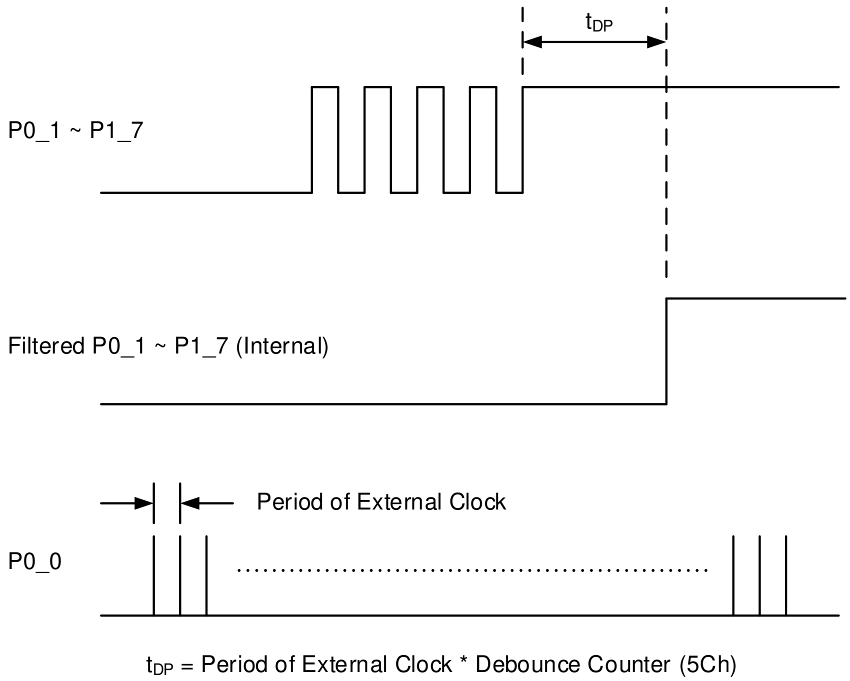


Figure 6. Debounce Timing

Recommended Layout

The VDD_P and VDD_I2C pins require bypass capacitors and they should be placed close to the IC. Use a 0.1µF, 10V rated, low ESR, X5R ceramic capacitor for best performance. Also, the trace length to VDD_P, VDD_I2C pin and the IC GND should be minimized.

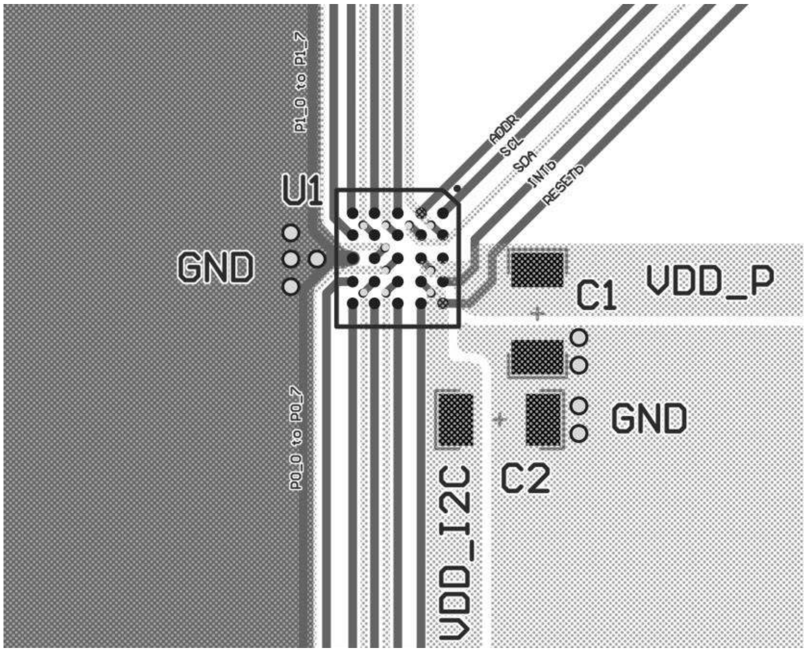


Figure 7. Recommended Layouts for FO-WLP55-25

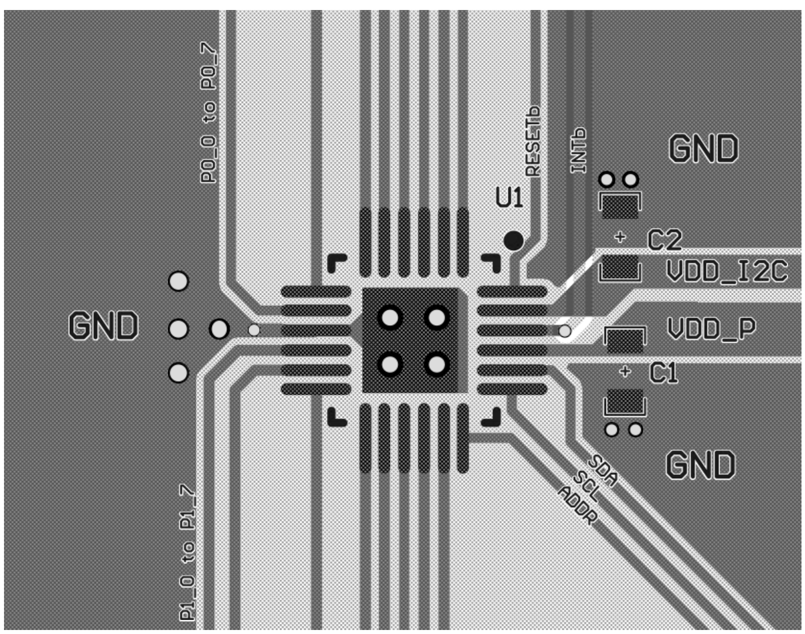
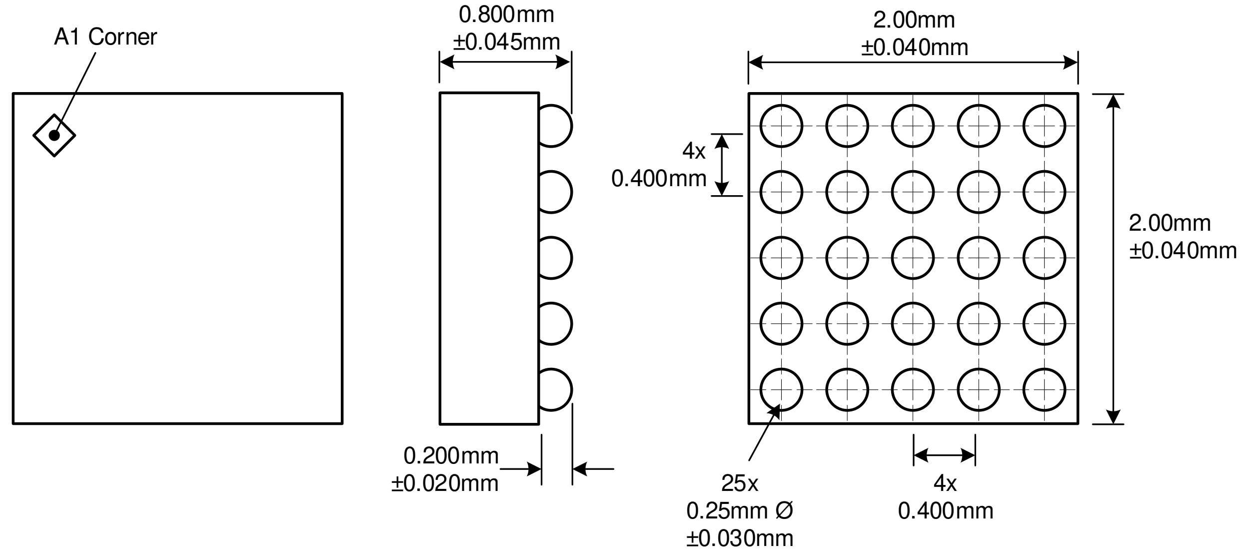


Figure 8. Recommended Layouts for TQFN44-24

Packaging Information

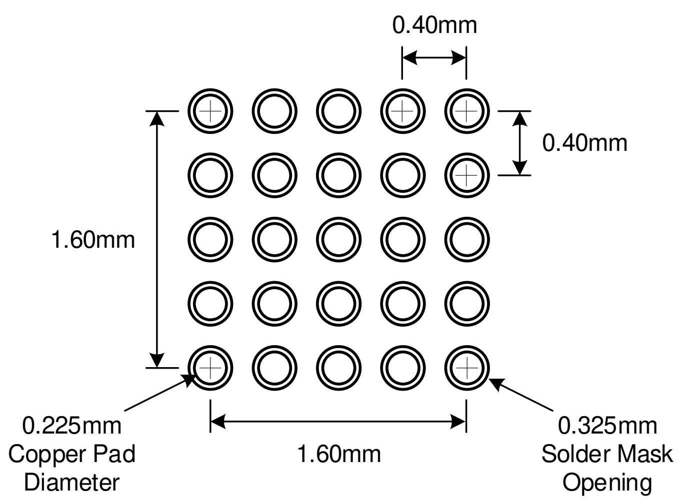
FO_WLP55-25 (2.00mm x 2.00mm x 0.800mm)

Top View **Side View** **Bottom View**



Recommended Footprint

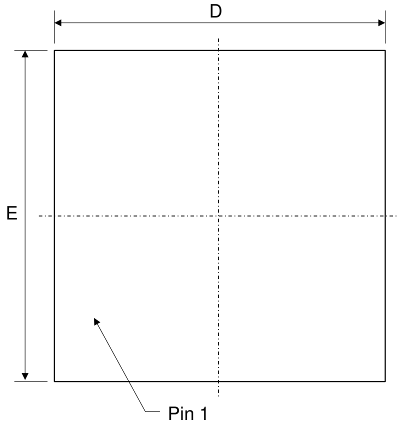
(NSMD Pad Type)



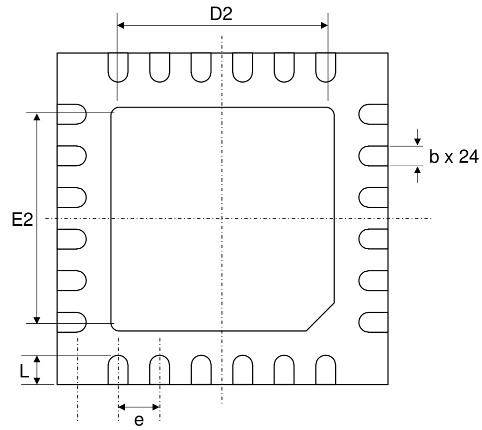
Packaging Information (continue)

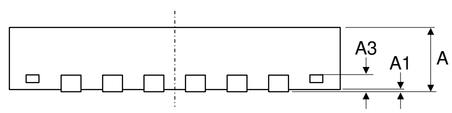
TQFN44-24 (4.00mm x 4.00mm x 0.75mm)

Top View



Bottom View





Side View

Dimension	mm		
	Min.	**Typ.**	**Max.**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	0.50 BSC		
L	0.30	0.35	0.40

Recommended Footprint