

### Features

- 1:4 HCSL clock buffer
- PCIe® Gen 1, 2 and 3 compliant
- Selectable reference inputs
- Cycle-to-Cycle Jitter <70ps
- Output-to-Output Skew <35ps
- 3.3V supply voltage
- TSSOP-20 package
- Industrial Temperature

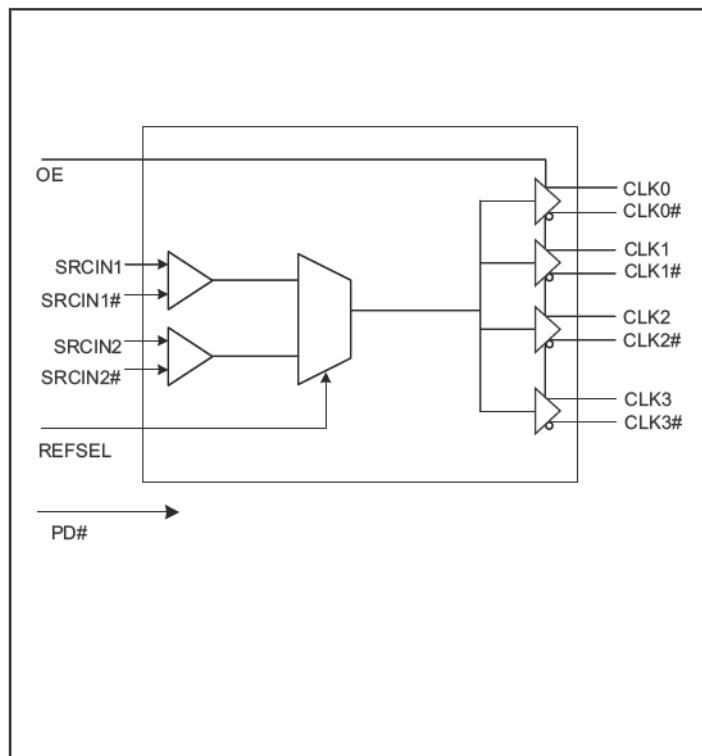
### Applications

- Servers
- Embedded computing systems
- Networking systems

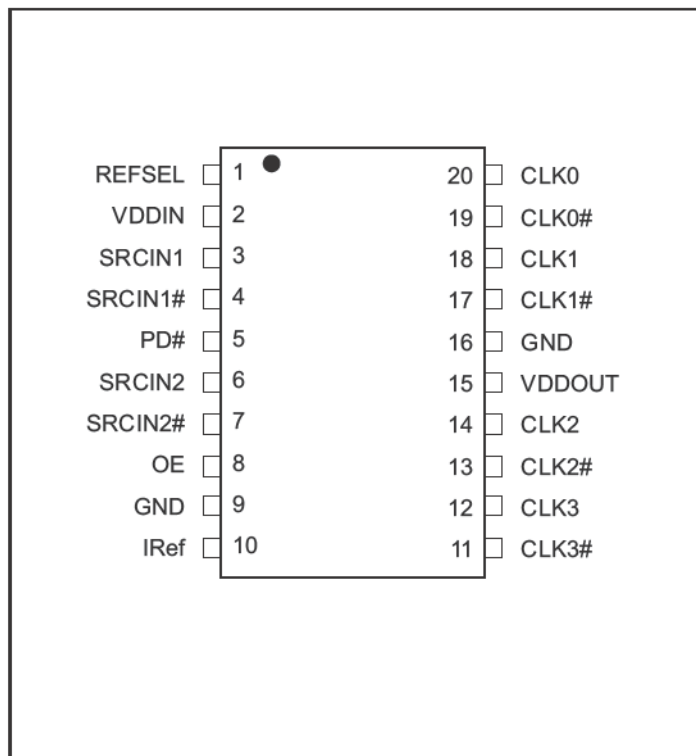
### Description

The PI6C557-06 is a high performance PCIe® buffer with four HCSL outputs compliant to PCIe® Gen 1, 2 and 3 standards. The device has selectable reference inputs to provide flexibility in system design.

### Block Diagram



### Pin Configuration



## Function Table

REFSEL	INPUT Selected
0	SRCIN2 / SRCIN2#
1	SRCIN1 / SRCIN1#

## Pin Description

Pin #	Pin	Type	Description
1	REFSEL	Input	Internal pull up. "0" select SRCIN2/2#; "1" selects SRCIN1/1#.
2	VDDIN	Power	3.3V for input buffer
3, 4	SRCIN1, SRCIN1#	Input	HCSL Input 1
5	PD#	Input	Power Down mode. "0" is "power down", "1" is normal operation. Internal pull up. Outputs are in tri-state when power down.
6, 7	SRCIN2, SRCIN2#	Input	HCSL input 2
8	OE	Input	Output enable for all outputs. "0" is "disabled" as tri-stated, "1" is enable output mode. Internal pull up.
9,16	GND	Power	Ground
10	IRef	Input	External resistor connection for internal current reference
11,12	CKL3#, CLK3	Output	HCSL output
13,14	CKL2#, CLK2	Output	HCSL output
15	VDDOUT	Power	3.3V for outputs
17, 18	CKL1#, CLK1	Output	HCSL output
19, 20	CKL0#, CLK0	Output	HCSL output

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature .....	- 65°C to +155°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
3.3V Analog Supply Voltage .....	- 0.5 to +4.6V
ESD Protection(HBM).....	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended Operating Condition**

Symbol	Description	Test Conditions	Min	Type	Max	Unit
V <sub>DD</sub>	Power supply	-	3.135	-	3.465	V
I <sub>DD</sub>	Total Power Supply Current	50Ω, 2pF	-	41 <sup>(1)</sup>		mA
		HCSL Load (See page 6)	-	-	90	mA
I <sub>DD_Output tri-stated</sub>	Total power supply current with Outputs are tri-stated	OE is "0"	-	-	15	mA
I <sub>dd power down</sub>	Total power supply current in power down mode	PD# = "0", no load			0.3	mA
T <sub>A</sub>	Operating temperature	Industrial temperature	-40		+85	°C

**Note:**

1. This is for 2 outputs. Total Current = I<sub>CORE</sub> + 2x I<sub>OUTPUT</sub> = 13 + 14 x 2 = 41mA

**LVC MOS DC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	-	2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-	-0.3	-	0.8	V
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>DD</sub>	-	-	45	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0V	-45	-	-	μA
R <sub>PU</sub>	Internal pull up resistance	REFSEL, OE, PD#	-	120	-	kOhm

**Differential DC Input Characteristics** (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>IH</sub>	Input High Current, IN-	V <sub>IN</sub> = V <sub>DD</sub> =3.465V	-	-	5	μA
	Input High Current, IN+				45	μA
I <sub>IL</sub>	Input Low Current, IN-	V <sub>IN</sub> = 0V	-45	-	-	μA
	Input Low Current, IN+		-5	-	-	μA
V <sub>IH</sub>	Input High Voltage	Single-ended swing HCSL	660	700	850	mV
V <sub>IL</sub>	Input Low Voltage		-150	0		mV
V <sub>ID</sub>	Input differential voltage	Single-ended swing LVDS	250	350	450	mV
V <sub>IO</sub>	Input Differential offset voltage	Cross point	1.125	1.25	1.375	mV

**HCSL DC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output High Voltage	-	660	-	850	mV
V <sub>OL</sub>	Output Low Voltage	-	-	-	150	mV
V <sub>CROSS</sub>	Absolute Crossing Point Voltages	-	250	-	550	mV
ΔV <sub>CROSS</sub>	Total variation of V <sub>CROSS</sub> overall edges	-	-	-	140	mV
I <sub>OH</sub>	Output High Current	With 475-Ohm resistor connected between IREF pin and GND	-	14	-	mA

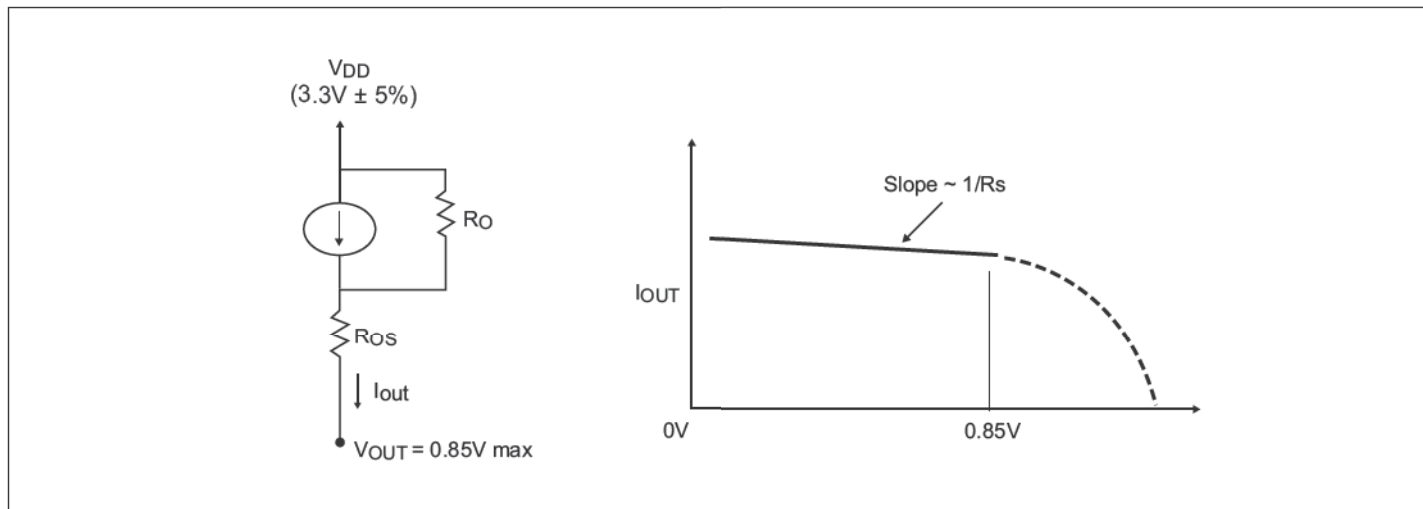
**HCSL AC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F <sub>in</sub>	Input Frequency	-	-	-	200	MHz
F <sub>OUT</sub>	Output Frequency	HCSL termination	-	-	200 <sup>(1)</sup>	MHz
T <sub>r</sub> /T <sub>f</sub>	Output Rise/Fall time	Between 0.175V and 0.525V <sup>(2)</sup>	175	-	700	ps
ΔT <sub>r</sub> /ΔT <sub>f</sub>	Rise and Fall Time Variation <sup>(2)</sup>	-	-	-	125	ps
T <sub>PD</sub>	Propagation delay	Input to output measured at the mid point level	-	3.0	4.5	ns
T <sub>skew</sub>	Output-to-Output Skew <sup>(3)</sup>	-	-	-	35	ps
T <sub>DC</sub>	Output Duty Cycle <sup>(3)</sup>	-	47	-	53	%
J <sub>C</sub>	Cycle to cycle jitter <sup>(3)</sup>	Differential waveform	-	50	70	ps
J <sub>Add</sub>	Additive RMS jitter <sup>(4)</sup>	100MHz HCSL from 12 kHz to 20MHz	-	330	-	fs
	Additive RMS jitter for PCIe 2.0		< 0	-	1	ps
J <sub>Phase</sub>	RMS phase jitter for PCIe 3.0	High Frequency	-	0.4	1	ps
		Low Frequency	-	0.6	3	ps
PSR	Power Supply Noise Rejection	50mVp-p input sine wave 100kHz to 600kHz <sup>(2)</sup>	-	-53	-	dBc
T <sub>OEN</sub>	OE enable time				100	ns
T <sub>OEF</sub>	OE disable time				100	ns

**Notes:**

1. For LVDS Termination , the maximum frequency is 100MHz
2. Measurement is taken from Single Ended waveform.
3. Measurement is taken from Differential waveform.
4. Additive jitter is calculated from input and output RMS phase jitter. ( $J_A = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$ )

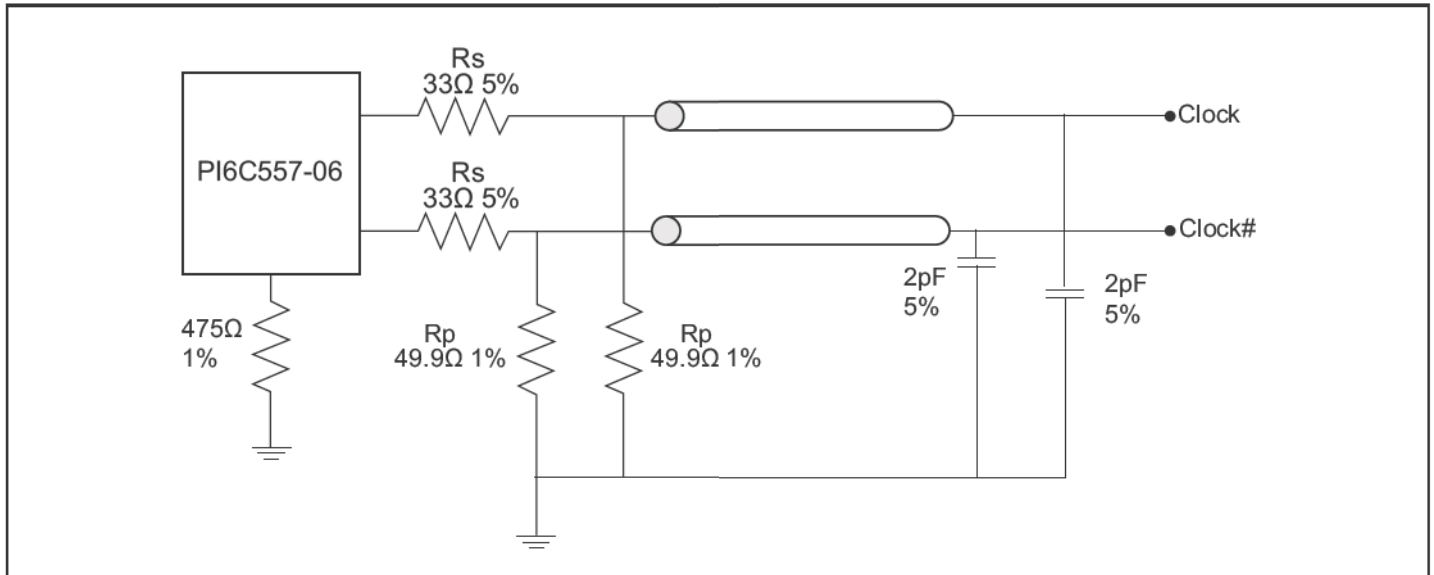
**HCSL output buffer characteristics**



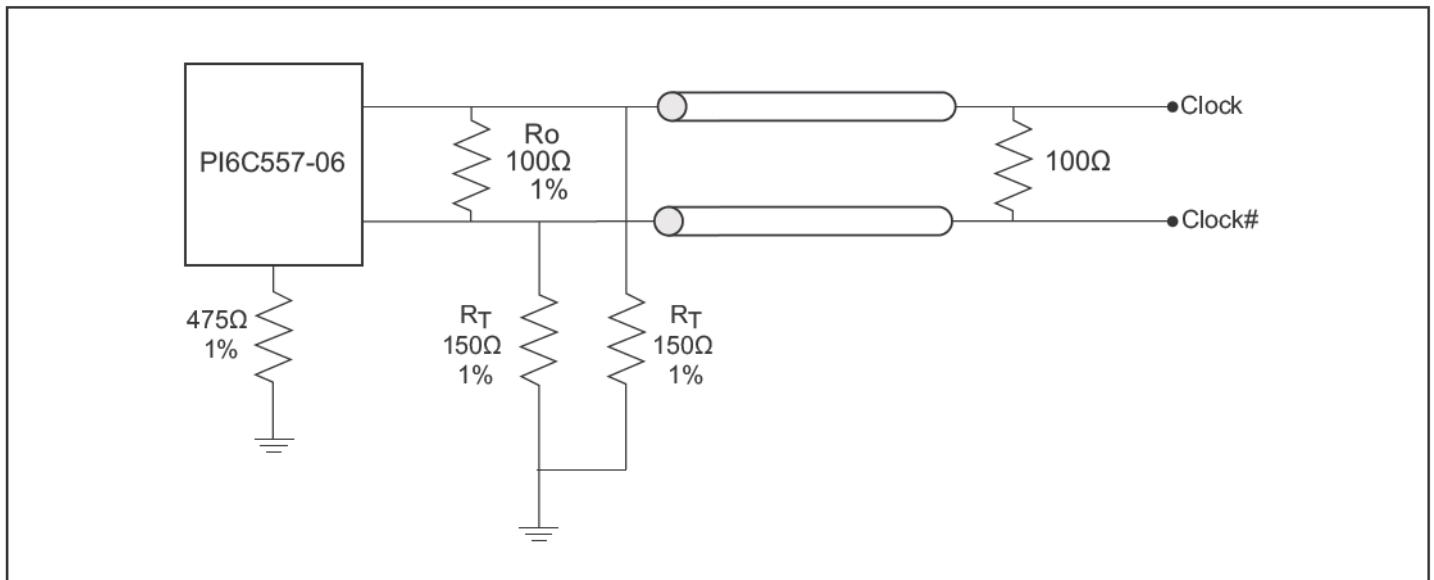
**HCSL output buffer characteristics**

Symbol	Minimum	Maximum
$R_o$	3000 $\Omega$	N/A
$R_{os}$	unspecified	unspecified
$V_{OUT}$	N/A	850mV

**Configuration**



**Test Load Board Termination for HCSL output**



**Test Load Board Termination for LVDS output**

**Packaging Mechanical: 20-pin TSSOP (L)**

DOCUMENT CONTROL NO.  
PD - 1311

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REVISION: E  
DATE: 03/09/05

**Note:**

1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimensions in millimeters
3. Ref. JEDEC MO-153F/AC

**PERICOM**

Pericom Semiconductor Corporation  
3545 N. 1st Street, San Jose, CA 95134  
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DESCRIPTION: 20-Pin, 173-Mil Wide, TSSOP

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PACKAGE CODE: L

**Ordering Information<sup>(1-3)</sup>**

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C557-06LIE	L	Pb-free & Green, 20-pin 173-mil TSSOP	-40°C to 85°C
PI6C557-06LE	L	Pb-free & Green, 20-pin 173-mil TSSOP	0°C to 70°C

**Notes:**

1. Thermal characteristics and package top marking information can be found at <http://www.pericom.com/packaging/>
2. E = lead-free and green packaging
3. Adding an X suffix = tape/reel