

MOSFET – N-Channel, UltraFET Trench

220 V, 7.0 A, 366 mΩ

FDMC2674

General Description

UltraFET device combines characteristics that enable benchmark efficiency in power conversion applications. Optimized for $R_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Features

- Max $R_{DS(on)}$ = 366 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 1.0\text{ A}$
- Typ $Q_g = 12.7\text{ nC}$ at $V_{GS} = 10\text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Converters and Off-Line UPS
- Distributed Power Architectures

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

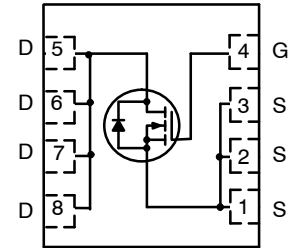
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	220	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current:		A
	Continuous (Silicon limited)	$T_C = 25^\circ\text{C}$	7.0
	Continuous (Note 1b)	$T_A = 25^\circ\text{C}$	1.0
	Pulsed		13.8
E_{AS}	Single Pulse Avalanche Energy (Note 3)	11	mJ
P_D	Power Dissipation:	$T_C = 25^\circ\text{C}$	42
		$T_A = 25^\circ\text{C}$ (Note 1a)	2.1
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

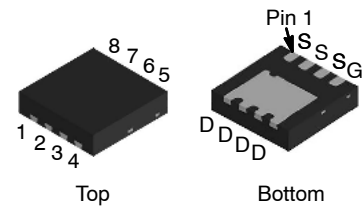
THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
220 V	366 mΩ @ 10 V	7.0 A

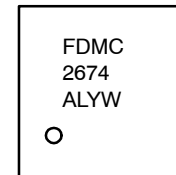


N-CHANNEL MOSFET



WDFN8 3.3 × 3.3, 0.65P
CASE 511DH

MARKING DIAGRAM



FDMC2674 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDMC2674	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDMC2674

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	220	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	248	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 176 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	3.4	4	V
ΔV _{GS(th)} /ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–10.2	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 1.0 A	–	305	366	mΩ
		V _{GS} = 10 V, I _D = 1.0 A, T _J = 150°C	–	678	814	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	–	880	1180	pF
C _{oss}	Output Capacitance		–	70	95	pF
C _{rss}	Reverse Transfer Capacitance		–	11	20	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 100 V, I _D = 1.0 A, V _{GS} = 10 V, R _{GEN} = 2.4 Ω	–	9	18	ns
t _r	Rise Time		–	13	23	ns
t _{d(off)}	Turn-Off Delay Time		–	15	27	ns
t _f	Fall Time		–	21	34	ns
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 1.0 A	–	12.7	18	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 15 V, I _D = 1.0 A	–	3.8	–	nC
Q _{gd}	Gate to Drain “Miller” Charge	V _{DD} = 15 V, I _D = 1.0 A	–	2.9	–	nC

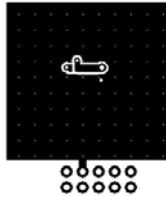
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.2 A (Note 2)	–	0.8	1.5	V
t _{rr}	Reverse Recovery Time	I _F = 1.0 A, di/dt = 100 A/μs	–	–	60	ns
Q _{rr}	Reverse Recovery Charge		–	–	109	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is determined with the device mounted on a 1 in² oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.
 - R_{θJA} = 60°C/W when mounted on a 1 in² pad of 2 oz copper, 1.5' × 1.5' × 0.062' thick PCB.
 - R_{θJA} = 135°C/W when mounted on a minimum pad of 2 oz copper.



a) 60°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 135°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- Starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 4.7 A, V_{DD} = 25 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

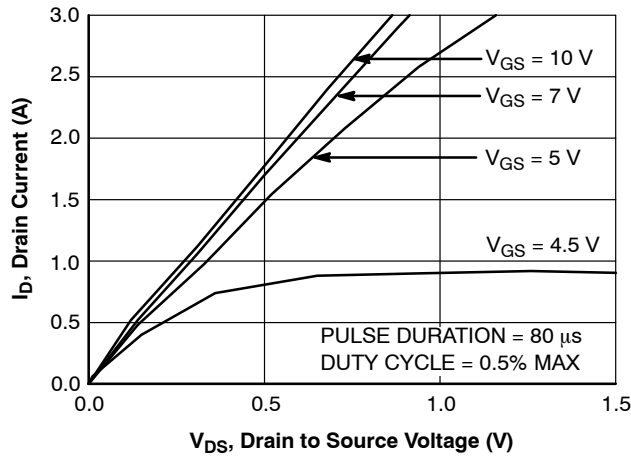


Figure 1. On-Region Characteristics

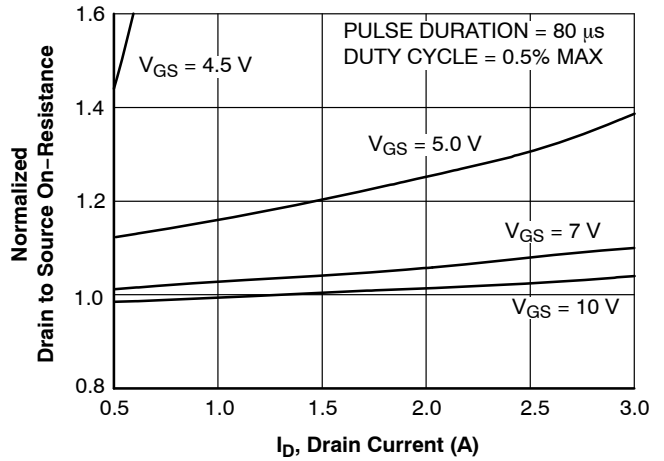


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

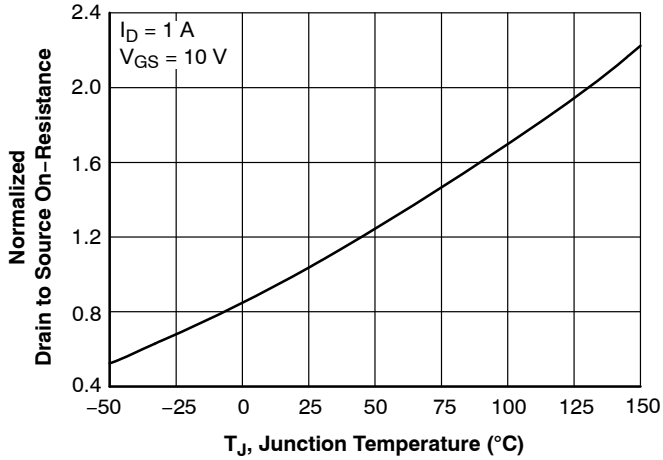


Figure 3. Normalized On-Resistance vs. Junction Temperature

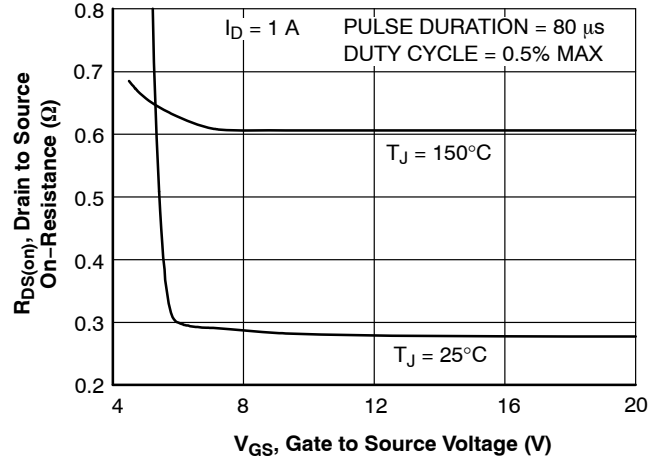


Figure 4. On-Resistance vs. Gate to Source Voltage

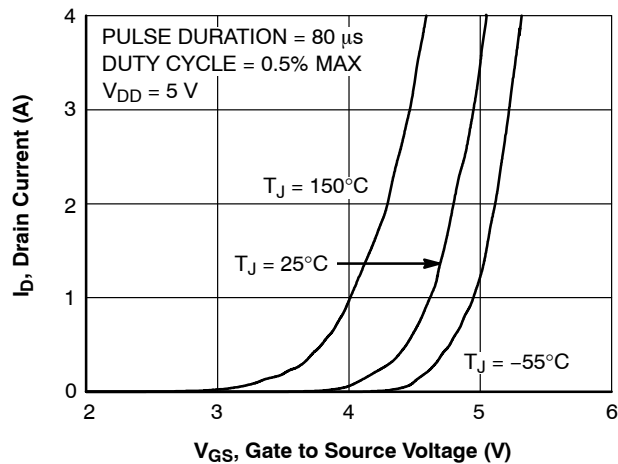


Figure 5. Transfer Characteristics

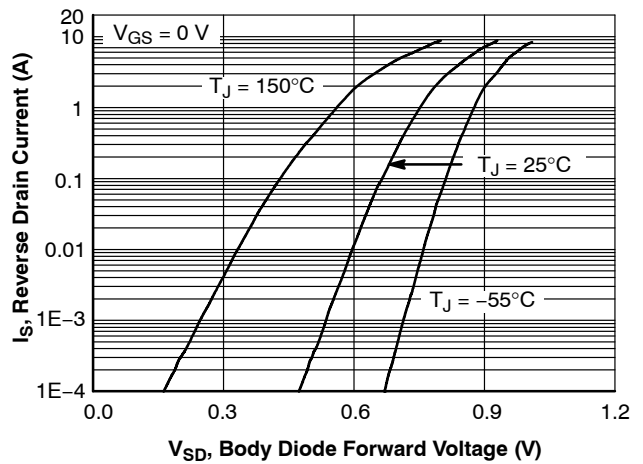


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

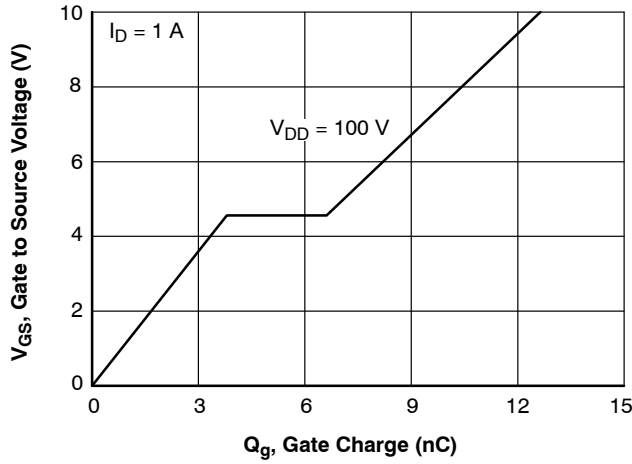


Figure 7. Gate Charge Characteristics

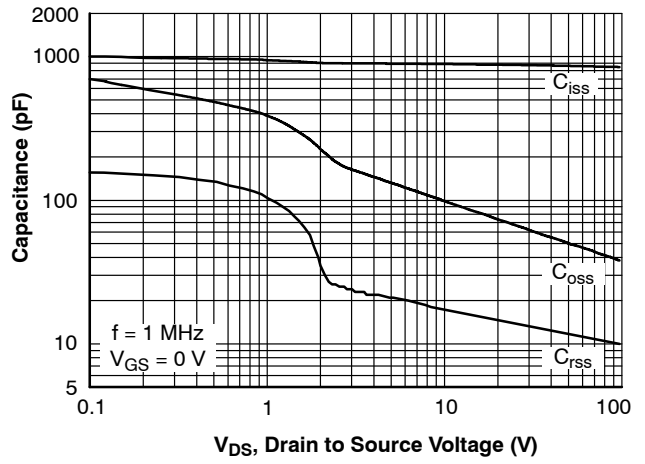


Figure 8. Capacitance vs. Drain to Source Voltage

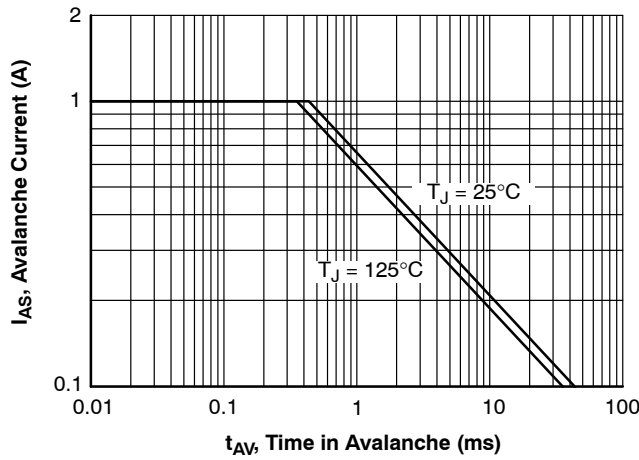


Figure 9. Unclamped Inductive Switching Capability

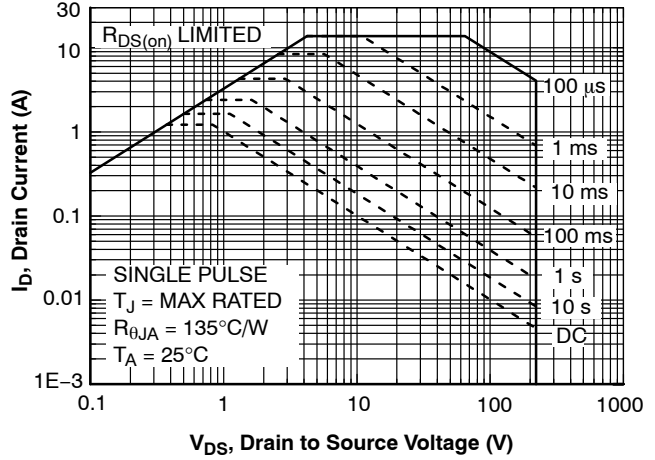


Figure 10. Forward Bias Safe Operating Area

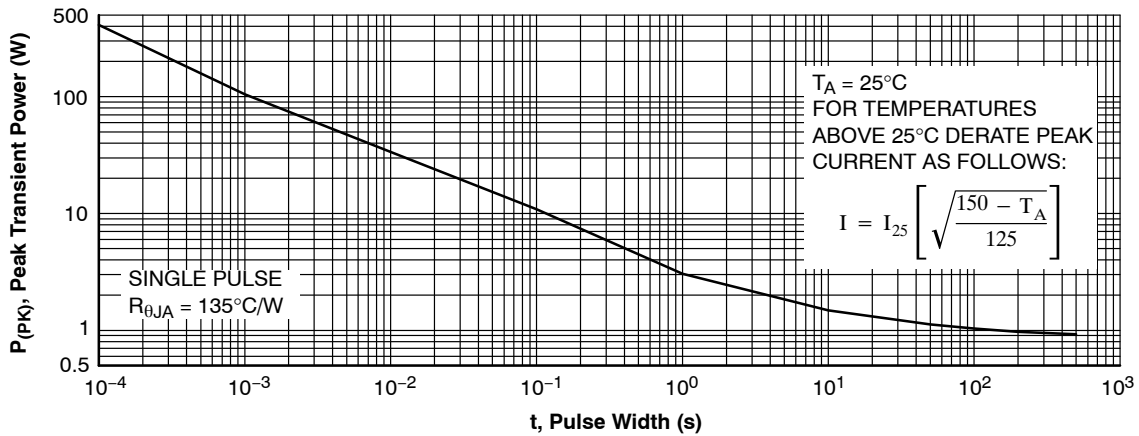


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

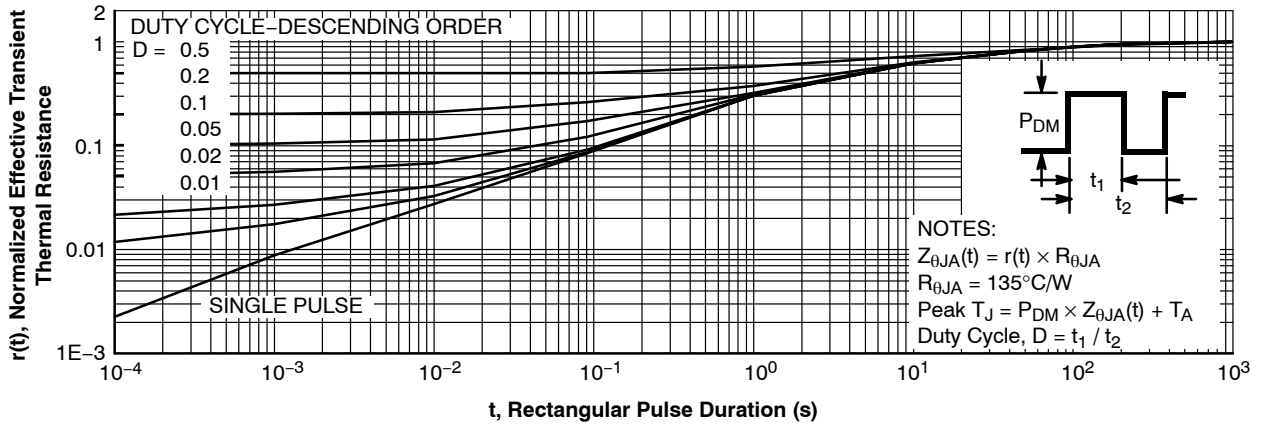


Figure 12. Transient Thermal Response Curve

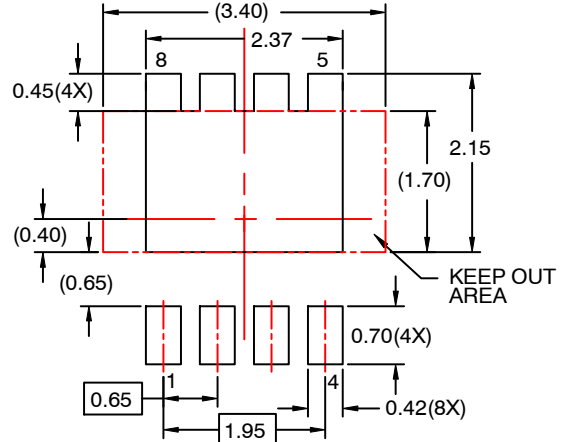
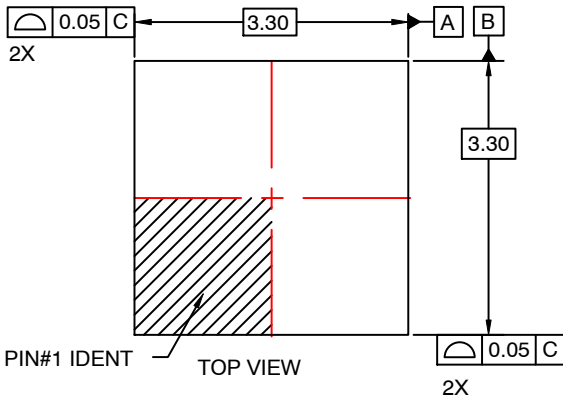
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

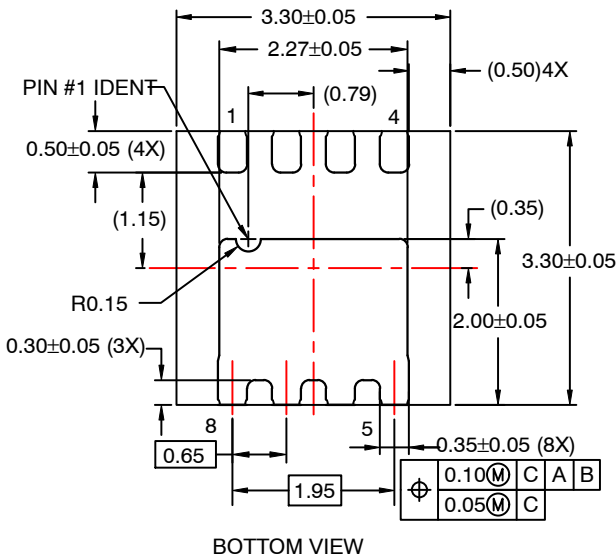
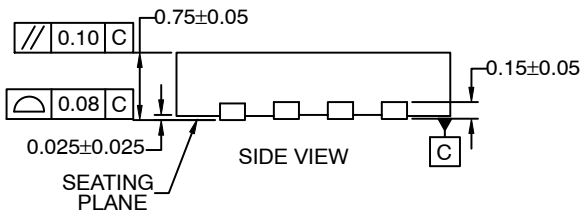


WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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