Supersedes March 2007

VP VERSA-PAC® Inductors and Transformers (Surface Mount)

Product features

- Six winding, surface mount devices that offer more than 500 usable inductor or transformer configurations
- High power density and low profile
- Low radiated noise and tightly coupled windings
- Power range from 1 Watt 70 Watts
- Frequency range to over 1 MHz
- 500 Vac Isolation
- Ferrite core material

Applications

- Inductors: buck, boost, coupled, choke, filter, resonant, noise filtering, differential, forward, common mode
- Transformers: flyback, feed forward, pushpull, multiple output, inverter, step-up, stepdown, gate drive, base drive, wide band, pulse, control, impedance, isolation, bridging, ringer, converter, autoAutomotive electronics (under hood, interior/exterior)
- Telematics
- GPS
- LED Lighting
- LCD Display
- Portable media devices

Environmental data

- Storage temperature range (component): -55 °C to $+125$ °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020 (latest revision) compliant

Product specifications

Product specifications- notes

- (1) The first three or four digits in the part number signify the size of the package. The next four digits specify the AL, or nanoHenries per turn squared. -R indicates RoHS compliant.
- (2) L_{base} = Nominal Inductance of a single winding.
- (3) I_{Base} is the lessor of $I_{\text{SAT(BASE)}}$ and $I_{\text{BMS(BASE)}}$.
- (4) Peak current that will result in 30% saturation of the core. This current value assumes that equal current flows in all six windings. For applications in which all windings are not simultaneously driven (i.e. flyback, SEPIC, Cuk, etc.), the saturation current per winding may be calculated as follows:

$$
I_{\text{SAT}} = \frac{6 \times I_{\text{SAT(BASE)}}}{\text{Number of Windows Drive}}
$$

- (5) RMS Current that results in a surface temperature of approximately 40 °C above ambient. The 40 °C rise occurs when the specified current flows through each of the six windings.
- (6) Maximum DC Resistance of each winding.
- (7) For multiple windings in series, the volt-usecond T_{OTAL} (μ Vs) capability varies as the number of windings in series (S):

$$
Volt\text{-}usec_{\text{total}} = S \times Volt\text{-}usec_{(\text{BASE})}
$$

For multiple windings in parallel, the volt-usecond T_{DMA} (µVs) capability is as shown in the table above.

(8) Maximum Energy capability of each winding. This is based on 30% saturation of the core:

Energy_{SERIES} = $S^2 \times \frac{1}{2} \times 0.7L_{BASE} \times I_{SAT(BASE)}^2$

Energy_{PARALLEL} = $P^2 \times \frac{1}{2} \times 0.7L_{BASE} \times I_{SAT(BASE)}^2$

For multiple windings, the energy capability varies as the square of the number of windings. For example, six windings (either parallel or series) can store 36 times more energy than one winding.

- (9) Thermal Resistance is the approximate surface temperature rise per Watt of heat loss under still-air conditions. Heat loss is a combination of core loss and wire loss. The number assumes the underlying PCB copper area equals 150% of the component area.
- (10) These devices are designed for feed-forward applications, where load current dominates magnitizing current.

VERSA-PAC temperature rise depends on total power losses and size. Any other **PCM** configurations other than those suggested could run hotter than acceptable.

Certain topologies or applications must be analyzed for needed requirements and matched with the best **VERSA-PAC** size and configuration. Proper consideration must be used with all parameters, especially those associated with current rating, energy storage, or maximum volt-seconds.

VERSA-PAC should not be used in off-line or safety related applications. The breakdown voltage from one winding to any other winding is 500 VAC maximum.

Dimensions- mm

VP1 and VPH1

max ref max ref ref max ref ref ref ref ref max VP1 and VPH1 12.9 9.2 13.0 0.7 5.9 6.2 1.5 0.1 0.25 11.5 1.5 2.25 9.7 14.2 2.0 0.5

NOTES:

- 1)Tolerances A I are ± 0.25 mm unless specified otherwise.
- 2)Tolerances J P are +/- 0.1 mm unless specified otherwise.
- 3)Marking:
- a) Dot for pin #1 identification
- b) VP(H)x-xxx (product code, size, 4 digit part number per family table.)
- c) Versa Pac Logo (optional)
- d) wwllyy = (date code) $R =$ (revision level) 4)All soldering surfaces must be coplanar within
- 0.102 mm.
- 5)Packaged in tape and reel 600 parts per reel

Dimensions- mm

FRONT VIEW

RECOMMENDED PCB LAYOUT

NOTES:

1)Tolerances A - I are ± 0.25 mm unless specified otherwise.

2)Tolerances J - P are +/- 0.1 mm unless specified otherwise.

3)Marking:

 (a) Dot for pin #1 identification

b) VP(H)x-xxx (product code, size, 4 digit part number per family table.)

c) Versa Pac Logo (optional)

d) wwllyy = (date code) $R =$ (revision level)

4)All soldering surfaces must be coplanar within 0.102 mm.

5)Packaged in tape and reel 300 parts per reel

J

VP3 and VPH3

NOTES:

1) Tolerances A - I are ± 0.25 mm unless specified otherwise.

2) Tolerances J - P are +/- 0.1 mm unless specified otherwise.

3) Marking:

- a) Dot for pin #1 identification
- b) VP(H)x-xxx (product code, size, 4 digit part number per family table.)
- c) Versa Pac Logo (optional)

d) wwllyy = (date code) $R =$ (revision level) 4) All soldering surfaces must be coplanar within

0.102 mm.

5) Packaged in tape and reel 200 parts per reel

A

I

Dimensions- mm

VP4 and VPH4

M L

NOTES:

O (10PLCS)

> N $(10PLCS)$

- 1) Tolerances A I are ± 0.25 mm unless specified otherwise.
- 2) Tolerances J P are +/- 0.1 mm unless specified otherwise.
- 3)Marking:
- a)Dot for pin #1 identification
- b) VP(H)x-xxx (product code, size, 4 digit part number per family table.)
- c) Versa Pac Logo (optional)
- d) wwllyy = (date code) $R =$ (revision level)
- 4)All soldering surfaces must be coplanar within
- 0.102 mm.
- 5) Bulk packaged
- For tape and reel add TR to part number: (i.e. VP4-0140TR-R) 140 parts per reel

VP5 and VPH5

VP5 and VPH5 21.0 21.0 28.5 0.7 10.8 2.95 0.1 0.4 17.25 2.25 3.15 22.7 29.0 3.0 0.75

NOTES:

1) Tolerances A - I are ± 0.25 mm unless specified otherwise.

- 2) Tolerances J P are +/- 0.1 mm unless specified otherwise.
- 3)Marking:
- a) Dot for pin #1 identification
- b) VP(H)x-xxx (product code, size, 4 digit part number per family table.)
- c) Versa Pac Logo (optional)
- d) wwllyy = (date code) $R =$ (revision level)
- 4)All soldering surfaces must be coplanar within 0.102 mm.
- 5) Bulk packaged
	- For tape and reel add TR to part number: (i.e. VP5-0155TR-R) 115 parts per reel

How to use multiple windings

Discrete inductors combine like resistors, when connected in series or parallel. For example, inductors in series add and inductors in parallel reduce in a way similar to Ohm's Law.

$$
L_{\text{Series}} = L1 + L2 + L3...Ln
$$

$$
L_{\text{Parallel}} = 1/[1/L1 + 1/L2 + 1/L3....1/Ln]
$$

Windings on the same magnetic core behave differently. Two windings in series result in four times the inductance of a single winding. This is because the inductance varies proportionately to the square of the turns.

Paralleled **VERSA-PAC** windings result in no change to the net inductance because the total number of turns remains unchanged; only the effective wire size becomes larger. Two parallel windings result in approximately twice the current carrying capability of a single winding. The net inductance of a given **PCM** configuration is based on the number of windings in series squared multiplied by the inductance of a single winding (LBASE). The current rating of a **PCM** configuration is derived by multiplying the maximum current rating of one winding (I_{BASE}) by the number of windings in parallel. Examples of simple two-winding devices are shown below:

Where:

 $L_{\text{BASE}} =$ Inductance of a single winding

- $P =$ Number of windings in parallel (use 1 with all windings in series)
- S = Number of windings in series
- I_{BASE} = Maximum current rating of one winding

How to pin-configure VERSA-PAC®

Each **VERSA-PAC** can be configured in a variety of ways by simply connecting pins together on the Printed Circuit Board (PCB). As shown below, the connections on the PCB are equal to the pin configuration statement shown at the bottom of the schematic symbol. Connecting a number of windings in parallel will increase the current carrying capability, while connecting in series will multiply the inductance. Each **VERSA-PAC** part can be configured in at least 6 combinations for inductor use or configured in at least 15 turns ratios for transformer applications. The **VERSA-PAC** allows for at least 500 magnetic configurations. The **PCM** configurations can either be created by the designer or simply chosen from the existing **PCM** diagrams. The following inductor example shows 6 windings in series, which result in an inductance of 36 times the base inductance and 1 times the base current.

INDUCTOR EXAMPLE FOR SIZES VP3,VP4 AND VP5

Each VERSA-PAC may be used in at least 15 transformer applications. More than 375 transformer combinations may be achieved using the available VERSA-PAC parts.

TRANSFORMER EXAMPLE FOR SIZES VP3, VP4 AND VP5 1 12 ত 11 হ 10 4 1 12 76 9 5 8 6 7 1 12 2 7 $L_{PRIMARY} = 1 \text{ x } L_{BASE}$ I_{PI} $=$ 1 x I_{BASE} \Box I_{SEC} $1 x I_{BASE}$ = 1:5 **PIN CONFIGURATIONS** (3,11)(4,10)(5,9)(6,8)

The PCM configurations may be selected from the examples above or created by the designer. The printed circuit board layout in each example illustrates the connections to obtain the desired inductance or turns ratio. The examples may be used by the PCB designer to configure **VERSA-PAC** as desired.

To assist the designer, **VERSA-PAC** phasing, coupling and thermal issues have been considered in each of the PCM configurations illustrated. Additionally, the inductance and current ratings, as a function of the respective base values are shown in each PCM example.

It is important to carefully select the proper **VERSA-PAC** part in order to minimize the component size without exceeding the RMS current capability or saturating the core. The Product specification table indicates maximum ratings.

VERSA-PAC® Performance characteristics

Bipolar (Push-Pull) Power vs Frequency

Unipolar (Flyback) Power vs Frequency

Inductance characteristics

These curves represent typical power handling capability.

Indicated power levels may not be achievable with all configurations.

3.3V Buck Converter

This circuit utilizes the gap of the VP5-0083 to handle the 12.5 Amp output current without saturating. In each of the five **VERSA-PAC** sizes, the gap is varied to achieve a selection of specific inductance and current values (see **VERSA-PAC** Data Table).

All six windings are connected in parallel to minimize AC/DC copper losses and to maximize heat dissipation. With **VERSA-PAC,** this circuit works well at or above 300 KHz. Also, the closed flux-path EFD geometry enables much lower radiation characteristics than open-path bobbin core style components.

LITHIUM-ION BATTERY TO 3.3V SEPIC CONVERTER

The voltage of a Lithium-Ion Battery varies above and below +3.3V depending on the degree of charge. The SEPIC configuration takes advantage of **VERSA-PAC**'s multiple tightly coupled windings. This results in lower ripple current which lowers noise and core losses substantially. The circuit does not require a snubber to control the voltage "spike" associated with switch turnoff, and is quite efficient due to lower RMS current in the windings.

5V to 3.3V Buck Converter With 5V Output

This circuit minimizes both board space and cost by eliminating a second regulator. **VERSA-PAC**'s gap serves to prevent core saturation during the switch on-time and also stores energy for the +5V load which is delivered during the flyback interval. The +3.3V buck winding is configured by placing two windings in series while the +5V is generated by an additional flyback winding stacked on the 3.3V output. Extra windings are paralleled with primary windings to handle more current. The turns ratio of 2:1 adds 1.67V to the +3.3V during the flyback interval to achieve +5V.

Solder Reflow Profile

Table 1 - Standard SnPb Solder $(\mathsf{T}_{\mathcal{O}})$

Table 2 - Lead (Pb) Free Solder $(\mathsf{T}_{\mathsf{C}})$

Reference JDEC J-STD-020

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

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