HARRIS

RFP17N06L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 17A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

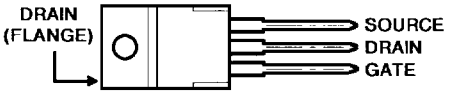
Description

The RFP17N06L is an N-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP17N06L is supplied in the JEDEC TO-220AB plastic package.

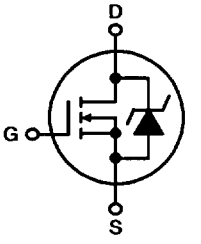
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	17	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

6 LOGIC LEVEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2272.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0 mA, V_{GS} = 0 V	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1.0 mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0 V	—	1	μA
		T_C = 150° C		50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V	—	100	nA
On Resistance	$R_{DS}(on)$	I_D = 8.5 A, V_{GS} = 4.0 V	—	0.150	Ω
		I_D = 8.5 A, V_{GS} = 5.0 V	—	0.100	
		I_D = 17.0 A, V_{GS} = 5.0 V	—	0.130	
Forward Transconductance	g_{FS}	I_D = 8.5 A, V_{DS} = 5.0 V	6.0	—	S
Turn-On Delay Time	$T_d(on)$	V_{DD} = 30 V, I_D = 8.5 A	—	40	ns
Rise Time	T_R	R_{GEN} = 12.5 ohms	—	150	
Turn-Off Delay Time	$T_d(off)$	R_{GS} = 12.5 ohms	—	240	
Fall Time	T_F	V_{GS} = +5 V	—	110	
Total Gate Charge	$Q_g(total)$	I_D = 8.5 A, V_{DD} = 30 V	—	45	nC
		V_{GS} = 10 V, R_L = 3.5 ohms			
Gate Charge at 5 volts	$Q_g(5)$	V_{GS} = 5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 1 V	—	2.0	
Thermal Resistance Junction to Case	$R_{\theta JC}$		—	2.083	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 17 A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 17 A, dI_F/d_t = 100 A/μs	115 (typ)		ns

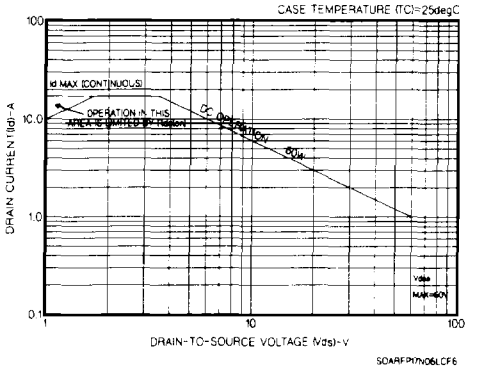


Fig. 1 - Maximum safe operating areas for all types.

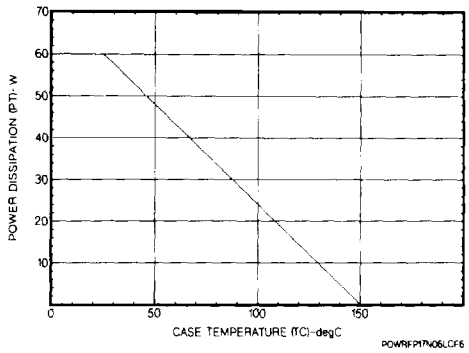


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

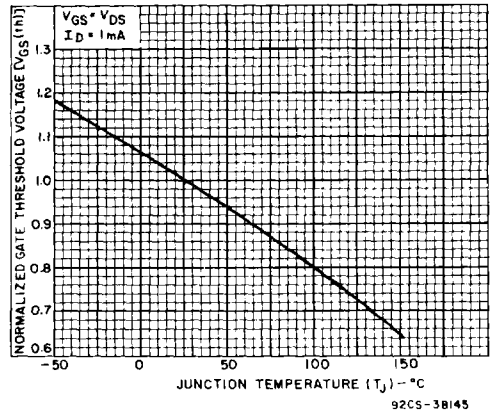


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

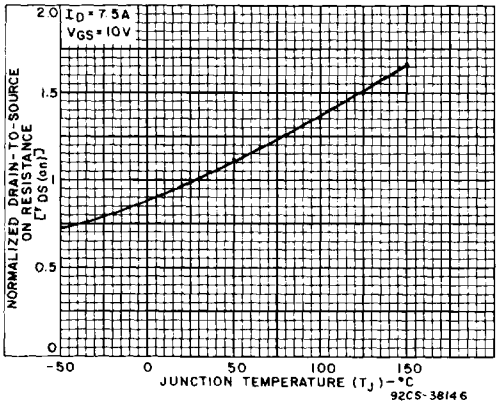


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

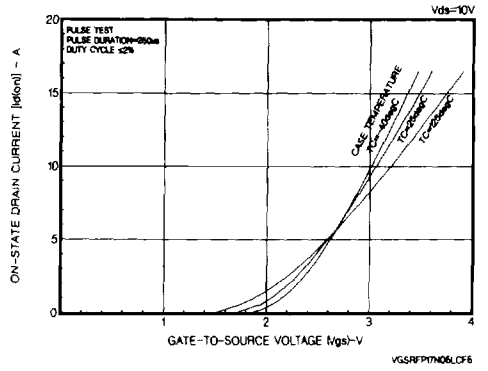


Fig. 5 - Typical transfer characteristics for all types.

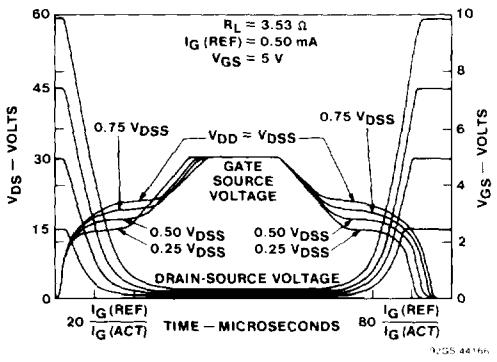


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

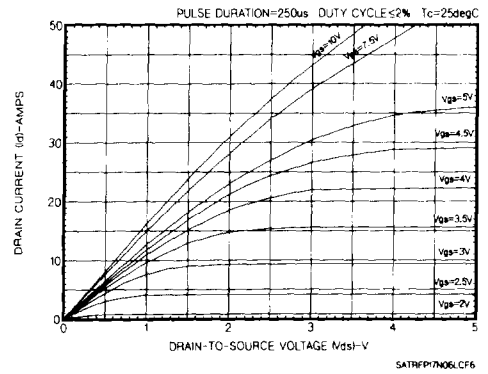


Fig. 7 - Typical saturation characteristics for all types.

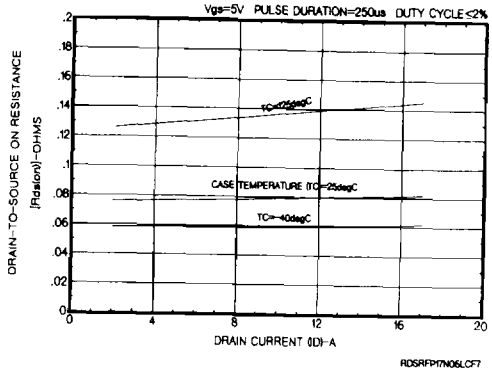


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

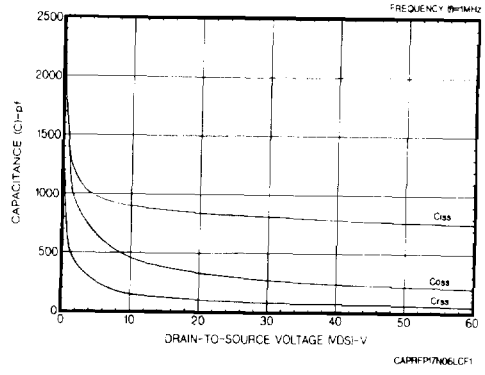


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

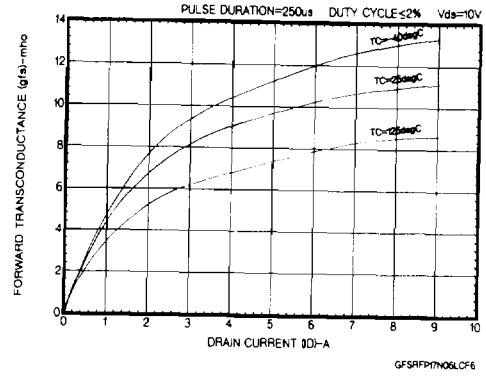


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

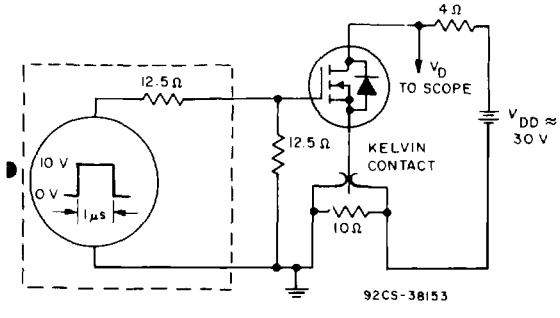


Fig. 11 - Switching Time Test Circuit.