MOSFET Drive Switching Regulator IC for Buck Converter

■ GENERAL DESCRIPTION

The **NJW4161** is a MOSFET Drive switching regulator IC for Buck Converter that operates wide input range from 3.1V to 40V. It can provide large current application because of built-in highly effective Pch MOSFET 10V drive circuit.

There are two types, Hiccup type and Latch type, of over current protection version.

It is suitable for logic voltage generation from high voltage that Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

■ PACKAGE OUTLINE

NJW4161R
(MSOP8(VSP8))

NJW4161D
(DIP8)

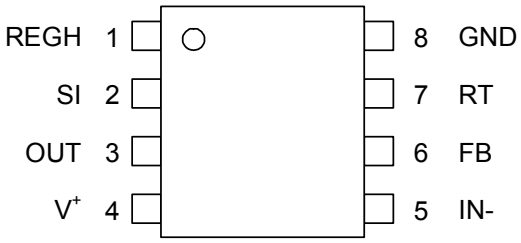
■ FEATURES

- Pch MOSFET Driving — Driving Voltage V^+-10V(typ.)
- Wide Operating Voltage Range — 3.1V to 40V
- PWM Control
- Automatic PWM/PFM Control improves power efficiency at light load. (C ver.)
- Wide Oscillating Frequency — 50kHz to 1MHz
- Soft Start Function — 15ms (typ.)
- Over Current Protection — Hiccup type (A, C ver.)
  Latch type (B ver.)
- Thermal Shutdown Protection
- UVLO (Under Voltage Lockout)
- Standby Function
- Package Outline — NJW4161R: MSOP8(VSP8) *MEETJEDEC MO-187-DA
  NJW4161D: DIP8

■ PRODUCT CLASSFICATION

Part Number	Version	Controller	Over Current Protection	Package	Operating Temperature Range
NJW4161R-A	A	PWM control	Hiccup type	MSOP8 (VSP8)	General Spec. -40°C to +125°C
NJW4161D-A	A	PWM control	Hiccup type	DIP8	General Spec. -40°C to +125°C
NJW4161R-B	B	PWM control	Latch type	MSOP8 (VSP8)	General Spec. -40°C to +125°C
NJW4161R-C	C	PWM/PFM control	Hiccup type	MSOP8 (VSP8)	General Spec. -40°C to +125°C

■ PIN CONFIGURATION



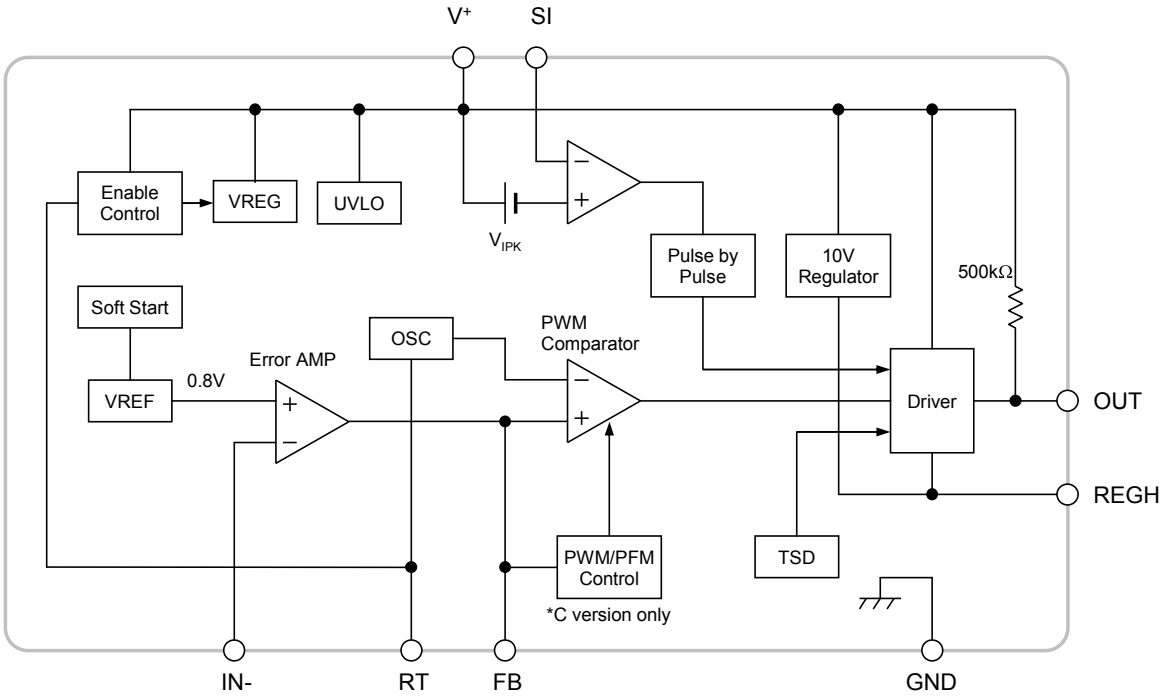
NJW4161R-A
NJW4161R-B
NJW4161R-C

NJW4161D-A

■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
REGH	1	Output pin of the high side regulator. Connect a bypass capacitor to stabilize a driver circuit.
SI	2	Current Sensing pin When difference voltage between the V^+ pin and the SI pin exceeds 120mV(typ.), over current protection operates.
OUT	3	Output pin for Power MOSFET Driving The OUT pin Voltage is clamped with V^+ -10V(typ.) at the time of Low level, in order to protect a gate of Pch MOSFET.
V^+	4	Power Supply pin
IN-	5	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.
FB	6	Feedback Setting pin The feedback resistor and capacitor are connected between the FB pin and the IN- pin.
RT	7	Oscillating Frequency Setting pin by Timing Resistor. Oscillating Frequency should set between 50kHz and 1MHz. NJW4161 becomes the standby mode when make RT pin open.
GND	8	GND pin

■ BLOCK DIAGRAM



RT State
ON: Connect timing resistor to GND
OFF (Stand-by): RT terminal open

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage	V^+	-0.3 to +45	V
OUT pin Voltage	V_{OUT}	V^+-11 to V^+ (*1)	V
SI pin Voltage	V_{SI}	V^+-5 to V^+ (*2)	V
REGH pin Voltage	V_{REGH}	V^+-11 to V^+ (*1)	V
IN- pin Voltage	V_{IN-}	-0.3 to +6	V
RT pin Voltage	V_{RT}	-0.3 to +6 (*3)	V
OUT pin Peak Current	I_{O_PEAK+} $I_{O\ PEAK-}$	1,700 (Source) 1,100 (Sink)	mA
Power Dissipation	P_D	MSOP8 595 (*4) (VSP8) 805 (*5) DIP8 700 (Device itself)	mW
Operating Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

(*1): When Supply voltage is less than +11V, the absolute maximum rating is -0.3 to V^+.

(*2): When Supply voltage is less than +5V, the absolute maximum rating is -0.3 to V^+.

(*3): When Supply voltage is less than +6V, the absolute maximum voltage is equal to the Supply voltage.

(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*5): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+	3.1	–	40	V
Timing Resistor	R_T	1.5	–	43	kΩ
Oscillating Frequency	f_{OSC}	50	–	1,000	kHz
REGH Capacitor	C_{REGH}	0.01	0.1	1	μF

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V^+=12V, R_T=10kΩ, C_{REGH}=0.1μF, Ta=25°C)

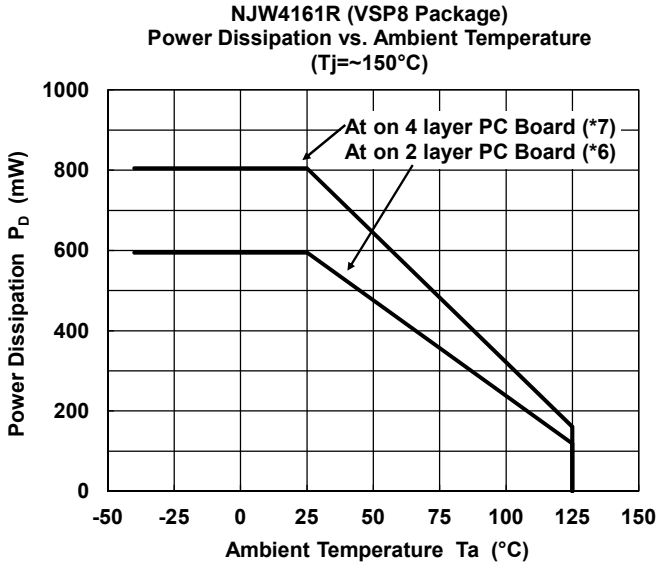
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillator Block						
Oscillating Frequency 1	f_{OSC1}	R_T=3.6kΩ	450	500	550	kHz
Oscillating Frequency 2	f_{OSC2}	R_T=10kΩ	180	200	220	kHz
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.8	+1.0%	V
Input Bias Current	I_B		-0.1	–	0.1	μA
Output Source Current	I_{OM+}	V_{FB}=1V, V_{IN-}=0.7V	50	90	140	μA
Output Sink Current	I_{OM-}	V_{FB}=1V, V_{IN-}=0.9V	6	13	20	mA
Soft Start Block						
Soft Start Time	t_{SS}	V_B=0.75V	7.5	15	24	ms
PWM Comparate Block						
Input Threshold Voltage (FB pin)	V_{T_0}	Duty=0%, V_{IN-}=0.6V	0.32	0.4	0.48	V
	V_{T_50}	Duty=50%, V_{IN-}=0.6V	0.63	0.7	0.77	V
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{FB}=1.2V	100	–	–	%
PWM/PFM Change Duty Cycle	$PFMD_{UTY}$	C version	5	10	15	%
Current Limit Detection Block						
Current Limit Detection Voltage	V_{IPK}		110	120	130	mV
Delay Time	t_{DELAY}		–	80	–	ns
Over Current Protection Block						
Cool Down Time	t_{COOL}	A, C version	–	60	–	ms
Timer Latch Time	t_{LATCH}	B version	–	10	–	ms
Output Block						
Output High Level ON Resistance	R_{OH}	I_O= -50mA	–	3.5	7	Ω
Output Low Level ON Resistance	R_{OL}	I_O= +50mA	–	3.5	7	Ω
REGH Output Current	I_{O_REGH}	REGH pin=V^+-8V	50	150	250	mA
OUT pin Limiting Voltage	V_{OLIM}		V^+-11	V^+-10	V^+-9	V
OUT pin Pull-Up Resistance	R_{OUT}		–	500	–	kΩ
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^+= L → H	2.9	3.0	3.1	V
OFF Threshold Voltage	V_{T_OFF}	V^+= H → L	2.6	2.7	2.8	V

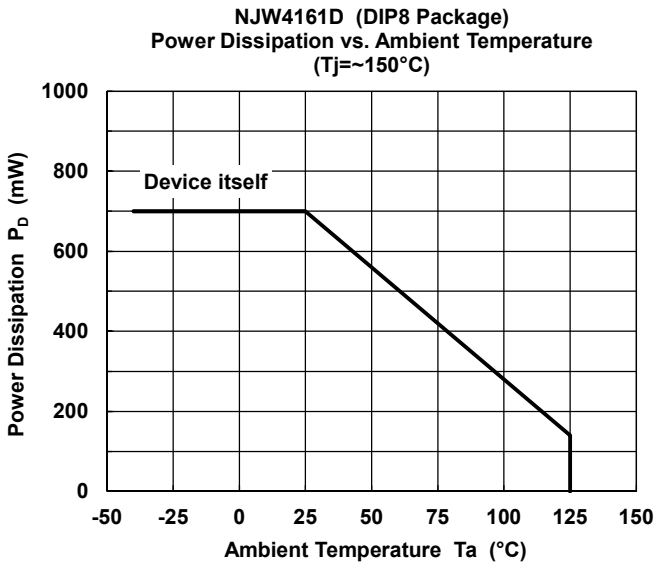
■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V^+=12V, R_T=10kΩ, C_{REGH}=0.1μF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
RT pin Enable Control Block						
RT pin Current at Standby	I_{RT_STB}		5.0	–	–	μA
General Characteristics						
Quiescent Current	I_{DD}	R_L=no load, V_{IN-}=0.7V, V_{FB}=0.7V	–	1.5	3	mA
Standby Current	I_{DD_STB}	V_{RT}=OPEN	–	2	10	μA

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE





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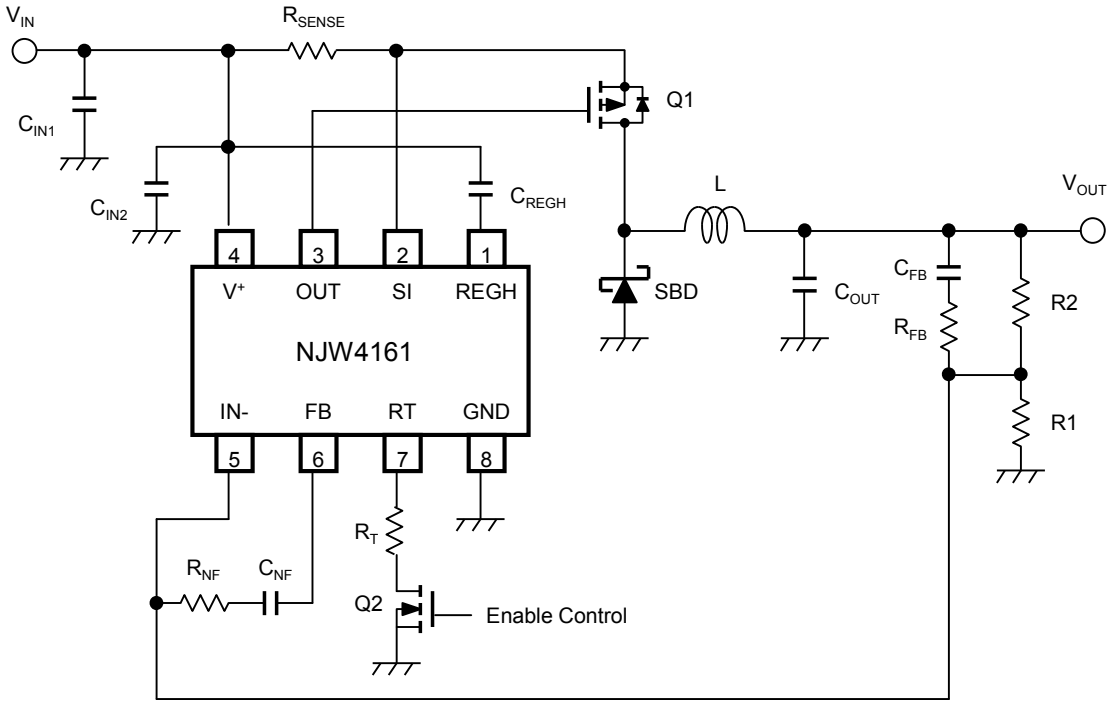
(*7): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

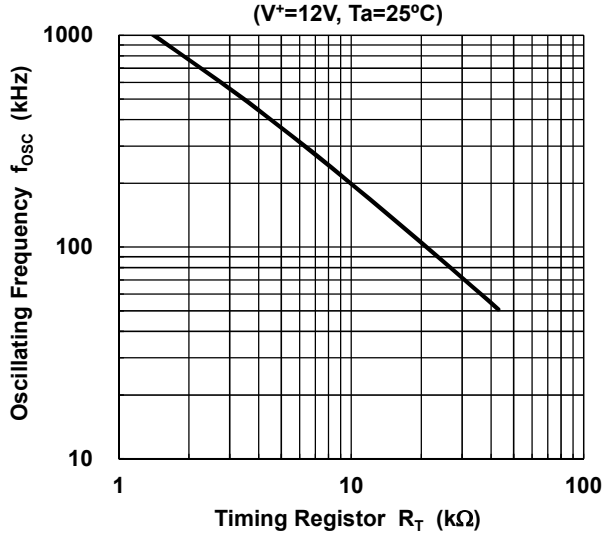
■ TYPICAL APPLICATIONS

Non-isolated Buck Converter

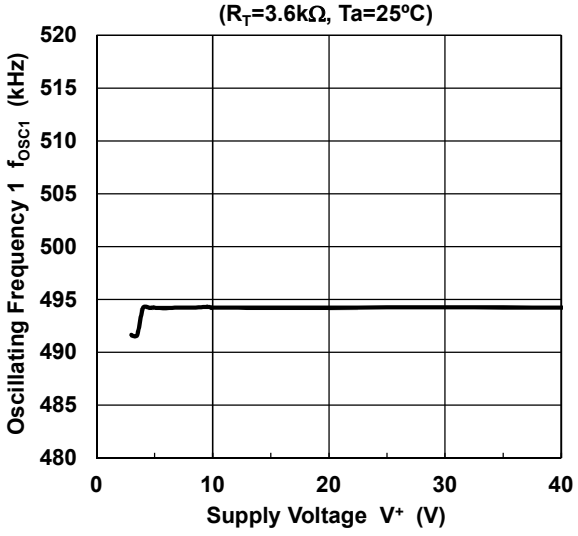


■ TYPICAL CHARACTERISTICS

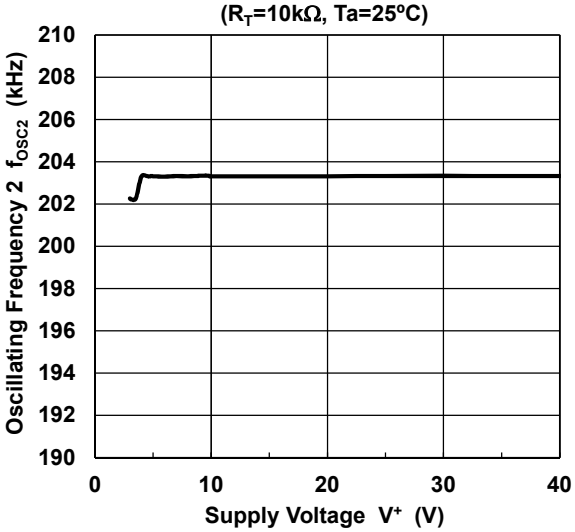
Oscillating Frequency vs. Timing Registor
(V^+=12V, Ta=25ºC)



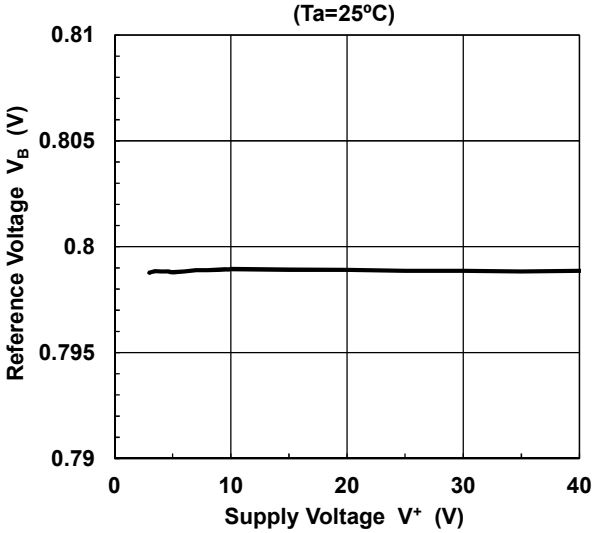
Oscillating Frequency 1 vs. Supply Voltage
(R_T=3.6kΩ, Ta=25ºC)



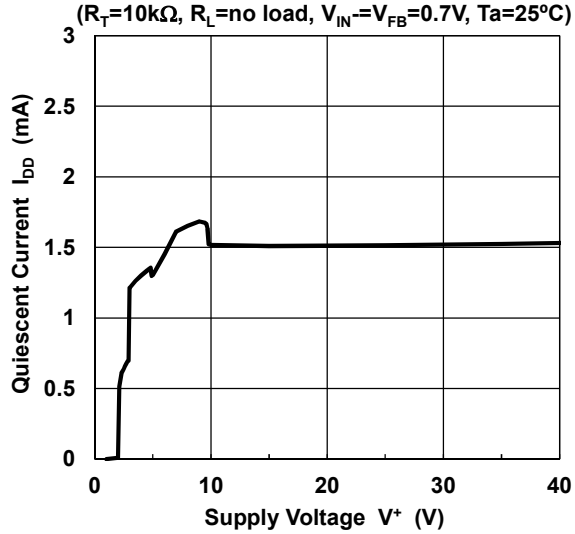
Oscillating Frequency 2 vs. Supply Voltage
(R_T=10kΩ, Ta=25ºC)



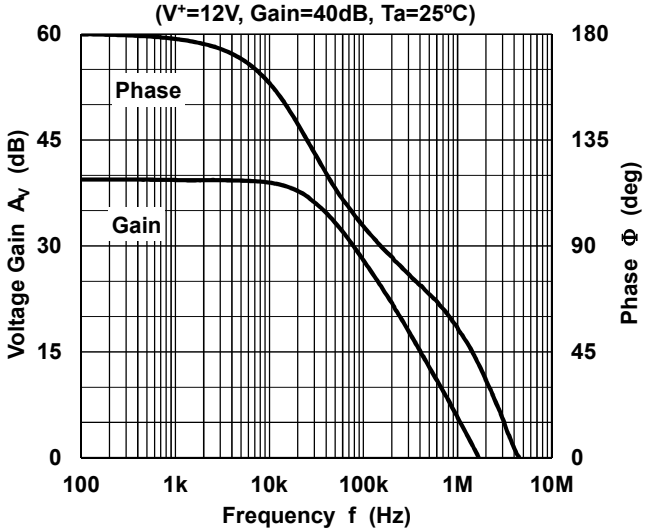
Reference Voltage vs. Supply Voltage
(Ta=25ºC)



Quiescent Current vs. Supply Voltage
(R_T=10kΩ, R_L=no load, V_{IN}-=V_{FB}=0.7V, Ta=25ºC)

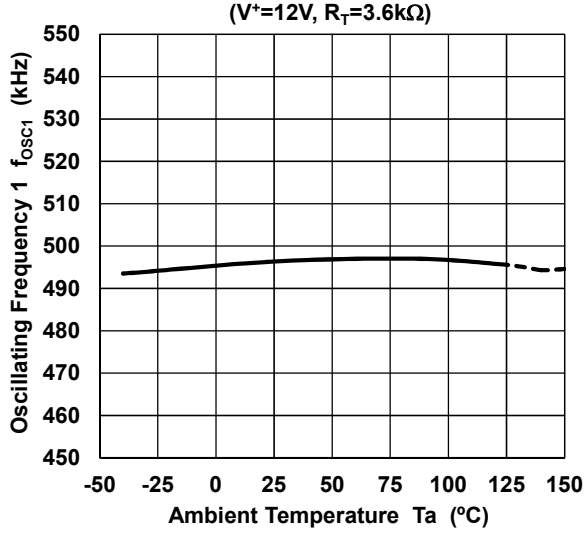


Error Amplifier Block
Voltage Gain, Phase vs. Frequency
(V^+=12V, Gain=40dB, Ta=25ºC)

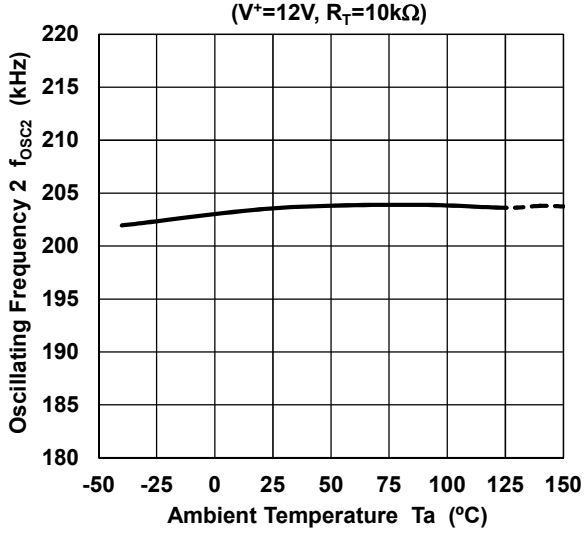


■ TYPICAL CHARACTERISTICS

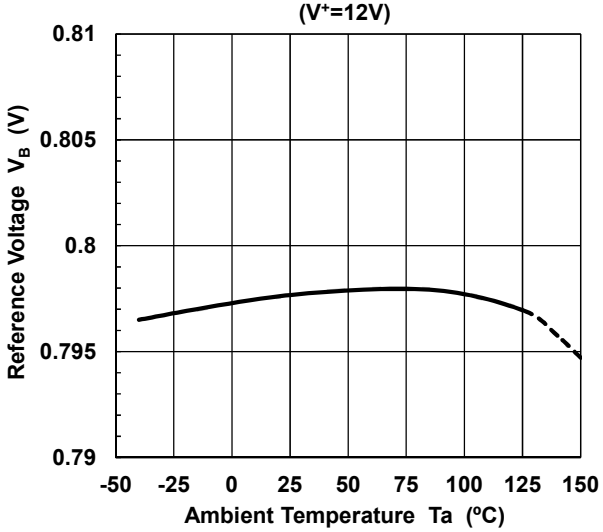
Oscillating Frequency 1 vs. Temperature
(V^+=12V, R_T=3.6kΩ)



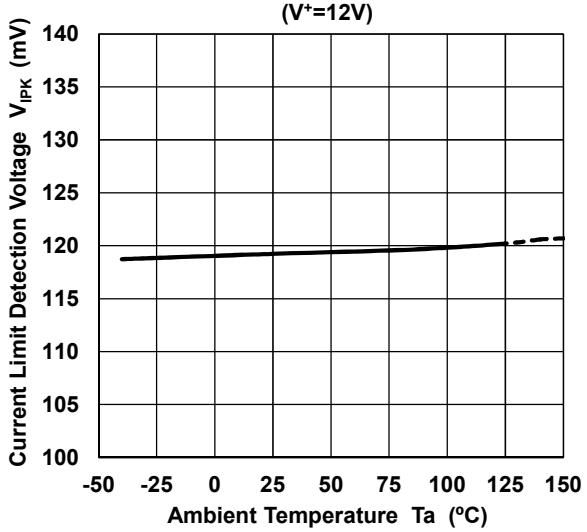
Oscillating Frequency 2 vs. Temperature
(V^+=12V, R_T=10kΩ)



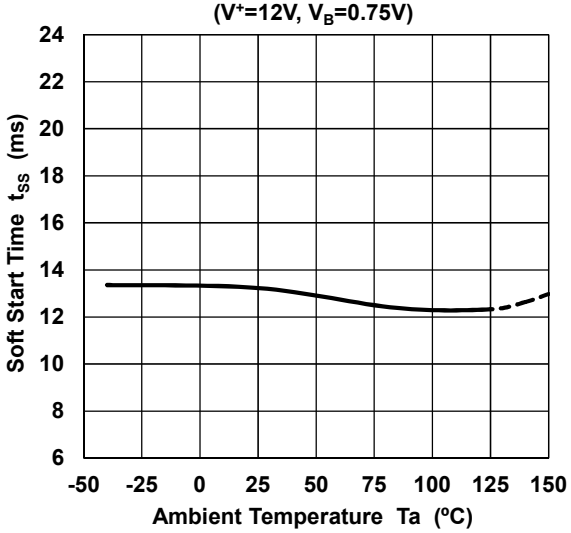
Reference Voltage vs. Temperature
(V^+=12V)



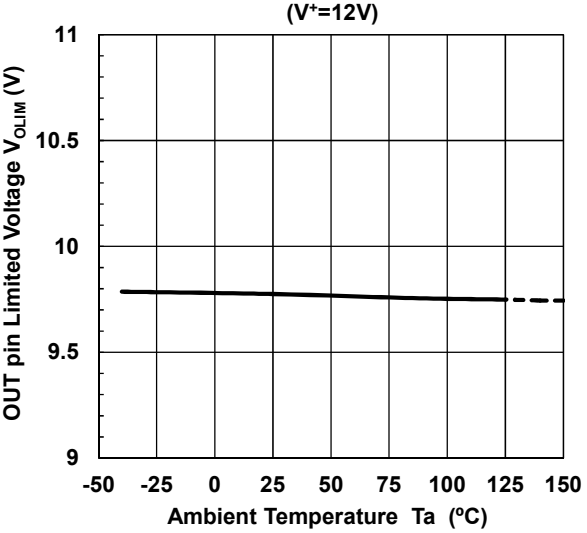
Current Limit Detection Votage vs.Temperature
(V^+=12V)



Soft Start Time vs. Temperature
(V^+=12V, V_B=0.75V)

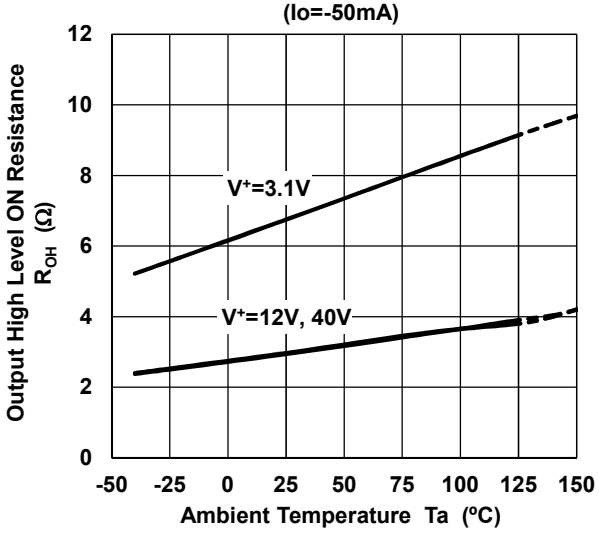


OUT pin Limiting Voltage vs.Temperature
(V^+=12V)

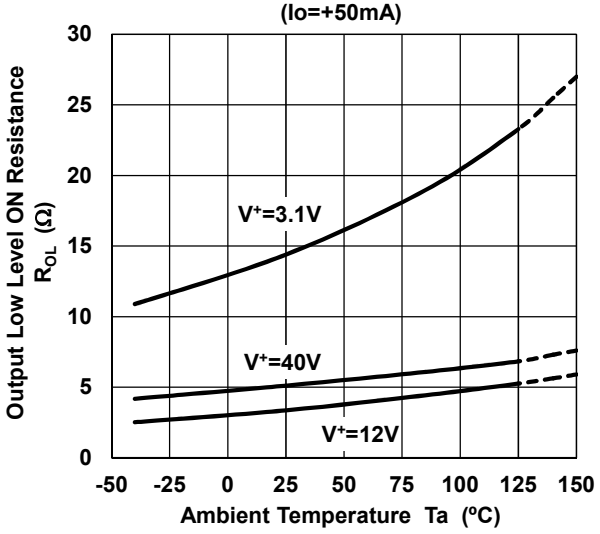


■ TYPICAL CHARACTERISTICS

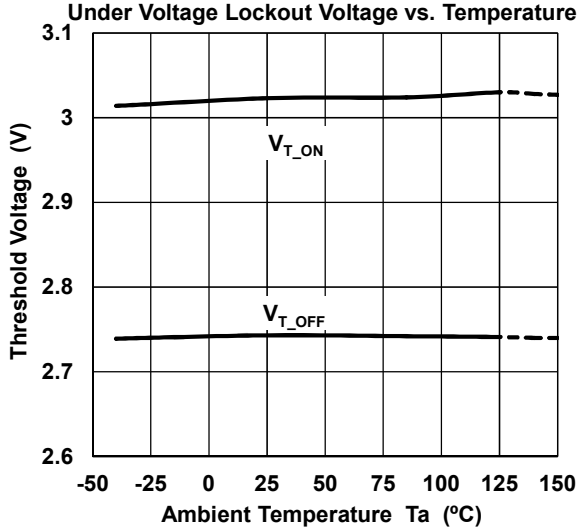
Output High Level ON Resistance vs.Temperature
(Io=-50mA)



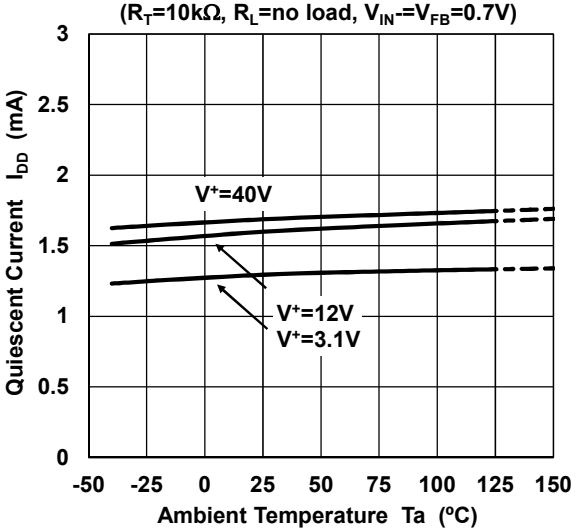
Output Low Level ON Resistance vs.Temperature
(Io=+50mA)



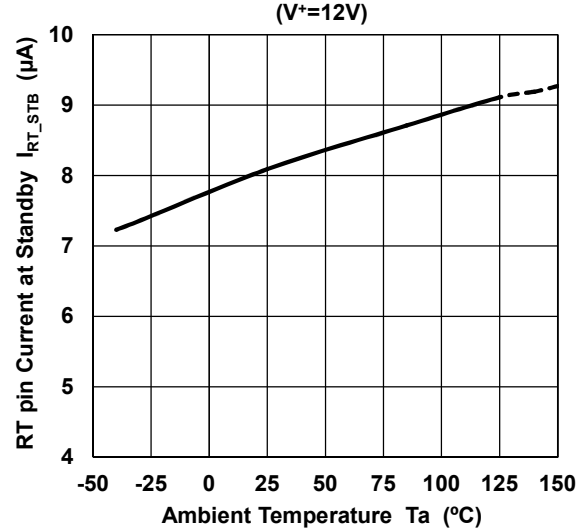
Under Voltage Lockout Voltage vs. Temperature



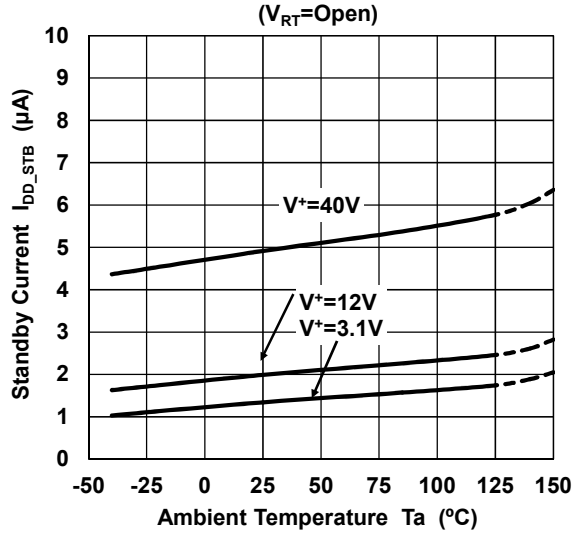
Quiescent Current vs. Temperature
(R_T=10kΩ, R_L=no load, V_{IN}-=V_{FB}=0.7V)



RT pin Current at Standby vs. Temperature
(V+=12V)



Standby Current vs. Temperature
(V_{RT}=Open)



■ Description of Block Features

1. Basic Functions / Features

● Error Amplifier Section (Error AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (IN- pin). If requires output voltage over 0.8V, inserts resistor divider.

This AMP section has high gain and external feedback pin (FB pin). It is easy to insert a feedback resistor and a capacitor between the FB pin and the IN- pin, making possible to set optimum loop compensation for each type of application.

● Oscillating Circuit Section (OSC)

Oscillating frequency can be set by inserting resistor between the RT pin and GND. Referring to the sample characteristics in "Timing Resistor and Oscillating Frequency", set oscillation between 50kHz and 1MHz.

NJW4161 becomes the standby mode when make RT pin open. Refer to the description of the standby function

● PWM Comparator Section (PWM)

PWM comparator receives the signal of the error amplifier and the triangular wave, and controls the duty ratio between 0% and 100%. The timing chart is shown in Fig.1.

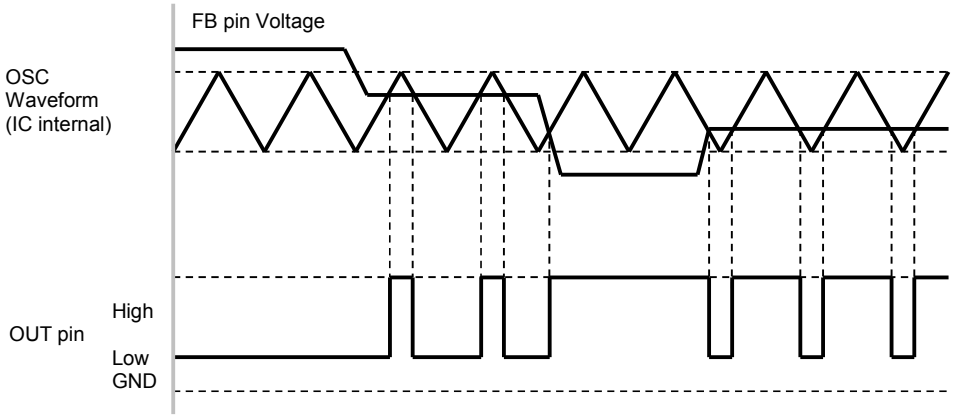


Fig. 1. Timing Chart PWM Comparator and SW pin

● PWM/PFM Control Feature (PWM/PFM Control: Only C version)

NJW4161 C version features automatic PWM/PFM control, improving power efficiency at light load.

Most of the application circuit loss occurs when the switching element performs, and therefore, the switching pulse is skipped to minimize unnecessary switching loss at times of low load.

When PWM comparator duty is no greater than 10% typ., switching output is stopped and switching is skipped to next period. In the case of high step-down ratio applications, a duty of steady operation may fall to 10% or less. Under such conditions, the PWM/PFM switch feature always operates. Therefore for high step-down ratio applications, use the PWM control type (A version or B version).

● Power Supply, GND pin (V^+ and GND)

In line with MOSFET drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor more than 0.1μF close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.

■ Description of Block Features (Continued)

● Driver Section , 10V Regulator Section (Driver, 10V Regulator)

The output driver circuit is configured a totem pole type, it can efficiently drive a Pch MOSFET switching device. When the output is low level, the OUT pin voltage is clamped with V^+ -10V (typ.) by the internal regulator to protect gate of Pch MOSFET. (Ref. Fig.2. OUT pin)

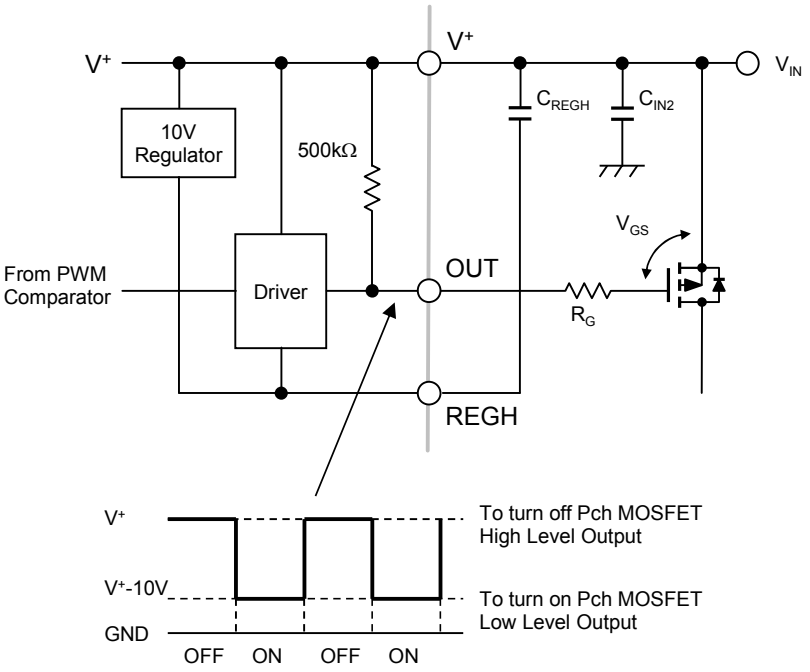


Fig. 2. Driver Circuit and the OUT pin Voltage

When supply voltage is decreasing, gate drive voltage output from the OUT pin is also decreasing. Fig.3. shows the example of the "OUT pin Differential Voltage vs. supply voltage" characteristic

The optimum drive ability of MOSFET depends on the oscillating frequency and the gate capacitance of MOSFET.

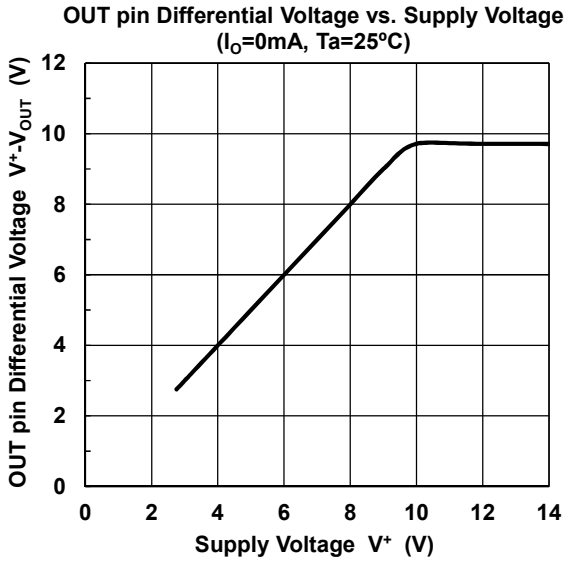


Fig. 3. OUT pin Differential Voltage vs. Supply Voltage Characteristic

■ Description of Block Features (Continued)

2. Additional and Protection Functions / Features

● Under Voltage Lockout (UVLO)

The UVLO circuit operating is released above V^+=3.0V(typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 300mV width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 15ms (typ.). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V. The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown.

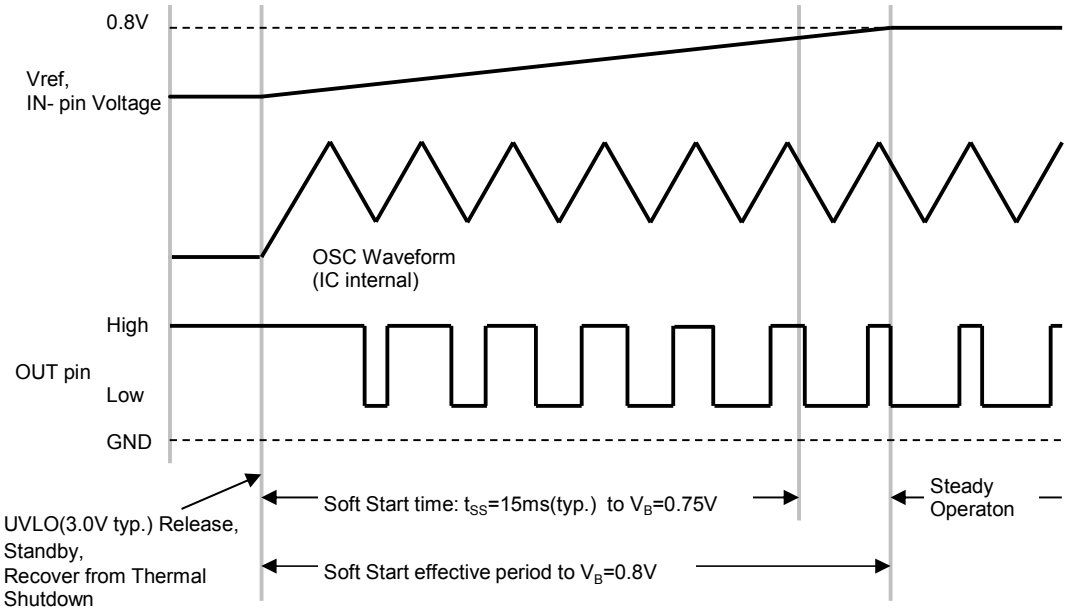


Fig. 4. Startup Timing Chart

■ Description of Block Features (Continued)

● Over Current Protection Circuit

At when the potential difference between the V^+ pin and the SI pin becomes 120mV or more, the over current protection circuit is stopped the switch output. The switching current is detected by inserted current sensing resistor (R_{SENSE}) between the V^+ pin and the SI pin.

There are Hiccup type of the automatic return and Latch type of the switching stop in NJW4161.

Hiccup Type: A version, C version
Latch Type: B version

● Hiccup Type (A version, C version)

The NJW4161-A and -C output returns automatically along with release from the over current condition.

Fig.5. shows the timing chart of the Hiccup type over current protection detection.

When the IN- pin voltage is 0.5V or lower(less), the switching operation stops after the overcurrent detection continued 8 pulses.

After NJW4161 switching operation was stopped, it restarts by soft start function after the cool down time of approx. 60ms (typ.).

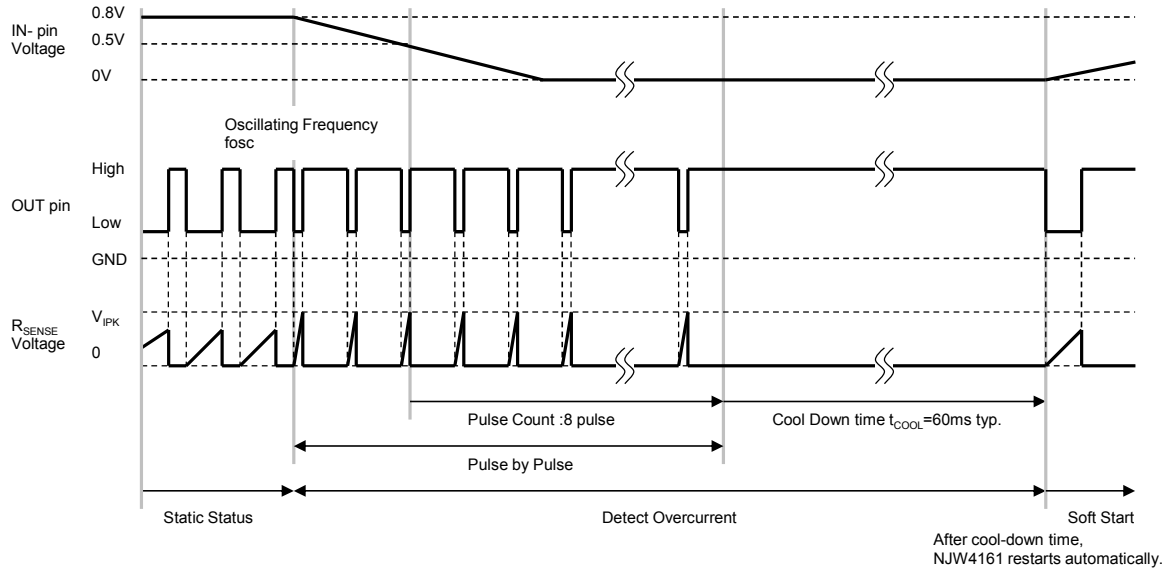


Fig. 5. Hiccup Type Timing Chart at Over Current Detection
(A version, C version)

■ Description of Block Features (Continued)

● Latch Type (B version)

When an overcurrent continues, NJW4161-B stops and maintains a stop state.

Fig.6. shows the timing chart of the Latch type over current protection detection.

When the IN- pin voltage is 0.5V or lower(less), the switching operation stops after the overcurrent detection continued 10ms.

After NJW4161 stopped, it restarts with a soft start by UVLO or standby input.

It does not latch, when it operation stops by thermal shutdown.

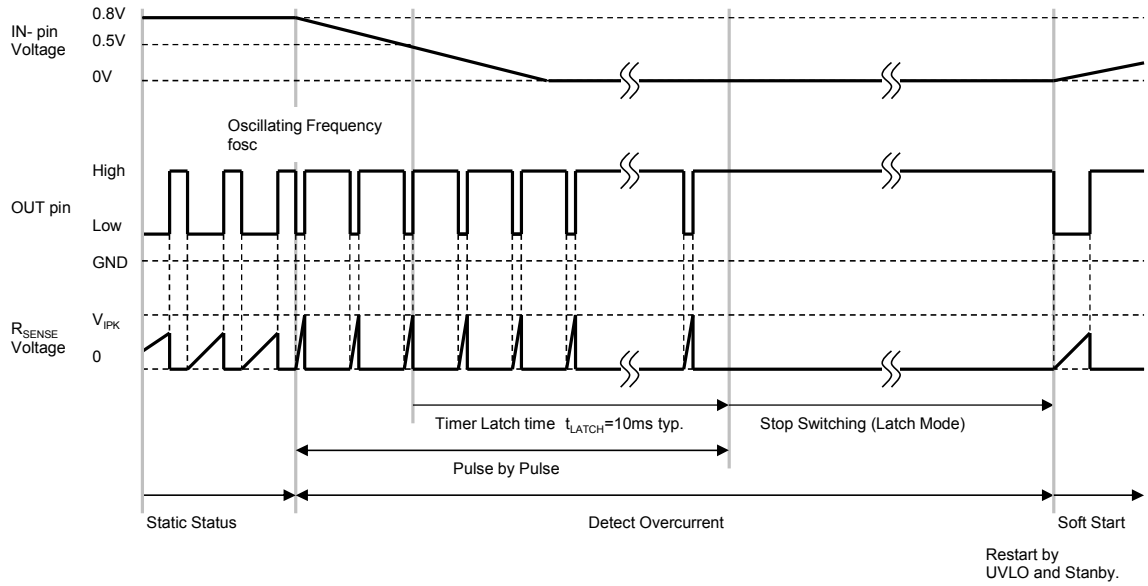


Fig. 6. Latch Type Timing Chart at Over Current Detection
(B version)

The current waveform contains high frequency superimposed noises due to the parasitic elements of MOSFET, the inductor and the others. Depending on the application, inserting RC low-pass filter between current sensing resistor (R_{SENSE}) and the SI pin to prevent the malfunction due to such noise. The time constant of RC low-pass filter should be equivalent to the spike width ($t \leq R_{LF} \times C_{LF}$) as a rough guide (Fig. 7). Or the insertion is effective with a bypass capacitor near the source pin of the MOSFET, too.

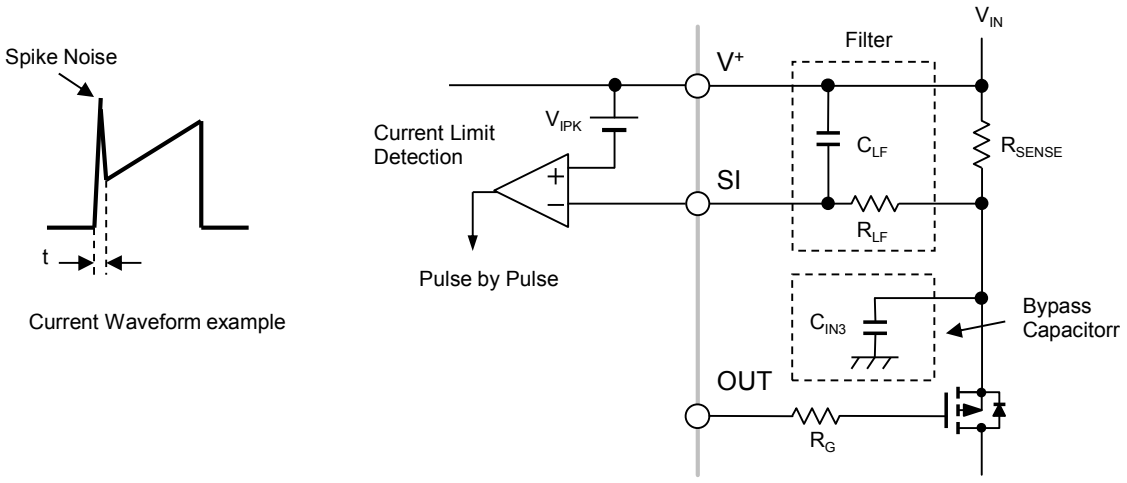


Fig. 7. Current Waveform and Filter Circuit

■ Description of Block Features (Continued)

● Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4161 exceeds the 160°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation returns with soft start operation.

The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. You should make sure to operate within the junction temperature range rated (150°C). (* Design value)

● Standby Function

To set the NJW4161 to standby status, insert MOSFET or others between the timing resistor RT and GND in order to set high impedance. (Fig. 8.)

It is necessary to make RT pin current less than I_{RT_STB}=5μA to a standby mode, therefore choose MOSFET of the small leak current.

If large capacitor is connected to RT pin when using a standby function, it becomes impossible to shift to an operating state from standby. When connect a bypass capacitor to RT pin, use capacitor of 100 pF or less.

Moreover, when changing from operation to a standby state, ON time may occur about 2μs by circuit delay.

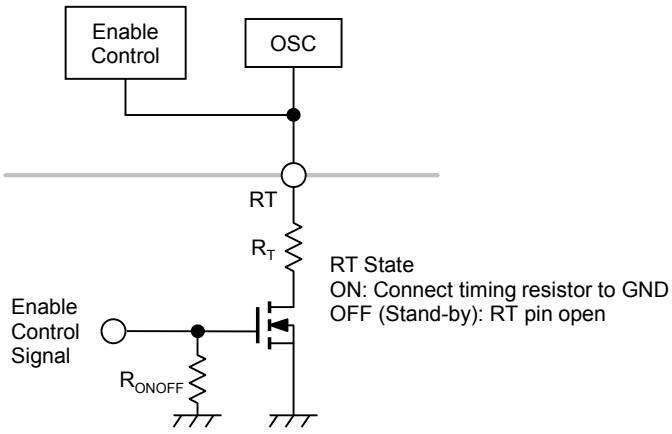


Fig. 8. When using a standby function

■ Application Information

● Inductors

Large currents flow into inductor, therefore you must provide current capacity that does not saturate.

Reducing L, the size of the inductor can be smaller. However, peak current increases and adversely affecting efficiency.

On the other hand, increasing L, peak current can be reduced at switching time. Therefore conversion efficiency improves, and output ripple voltage reduces. Above a certain level, increasing inductance windings increases loss (copper loss) due to the resistor element.

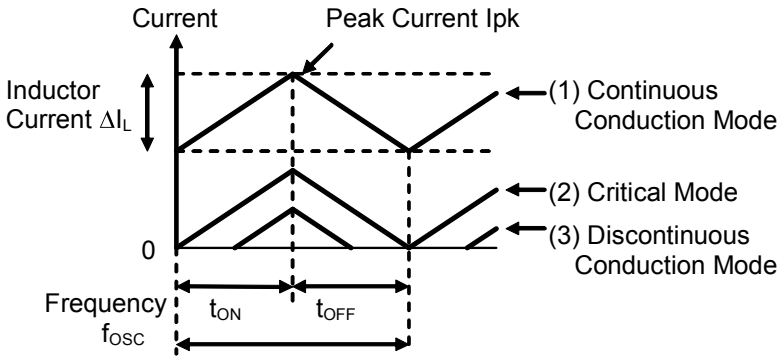


Fig. 9. Inductor Current State Transition

Ideally, the value of L is set so that inductance current is in continuous conduction mode. However, as the load current decreases, the current waveform changes from (1) CCM: Continuous Conduction Mode → (2) Critical Mode → (3) DCM: Discontinuous Conduction Mode (Fig. 9.).

In discontinuous mode, peak current increases with respect to output current, and conversion efficiency tend to decrease. Depending on the situation, increase L to widen the load current area to maintain continuous mode.

● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

An SBD also has a short reverse recovery time. If the reverse recovery time is long, through current flows when the switching transistor transitions from OFF cycle to ON cycle. This current may lower efficiency and affect such factors as noise generation.

● Switching Element

You should use a switching element (Pch MOSFET) that is specified for use as a switch. And select sufficiently low R_{ON} MOSFET at less than V_{GS}=10V because the NJW4161 OUT pin voltage is clamped V^+-10V (typ.).

However, when the supply voltage of the NJW4161 is low, the OUT pin voltage becomes low. You should select a suitable MOSFET according to the supply voltage specification. (Ref. Driver section)

Large gate capacitance is a source of decreased efficiency. That is charge and discharge from gate capacitance delays switching rise and fall time, generating switching loss.

The spike noise might occur at the time of charge/discharge of gate by the parasitic inductance element. You should insert resistance between the OUT pin and the gate and limit the current for gate protection when gate capacitance is small. However, it should be noted that the efficiency might decrease because the shape of waves may become duller when resistance is too large. The last fine-tuning should be done on the actual device and equipment.

■ Application Information (Continued)

● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4161 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible.

● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

Also, the ambient temperature affects capacitors, decreasing capacitance and increasing ESR (at low temperature), and decreasing lifetime (at high temperature). Concerning capacitor rating, it is advisable to allow sufficient margin.

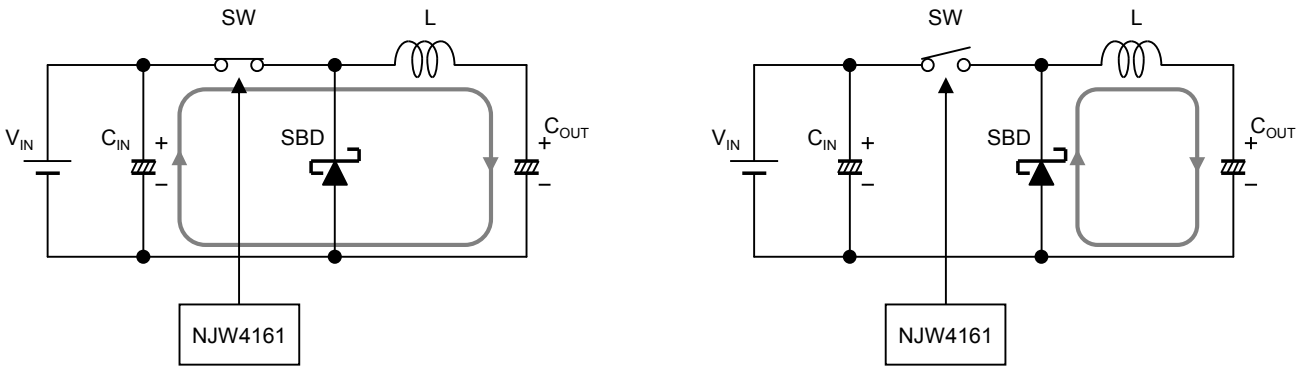
Output capacitor ESR characteristics have a major influence on output ripple noise. A capacitor with low ESR can further reduce ripple voltage. Be sure to note the following points; when ceramic capacitor is used, the capacitance value decreases with DC voltage applied to the capacitor.

■ Application Information (Continued)

● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillating frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig. 10. shows a current loop at step-down converter.



(a) Buck Converter SW ON (b) Buck Converter SW OFF

Fig. 10. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 11. shows example of wiring at buck converter. Fig. 12 shows the PCB layout example.

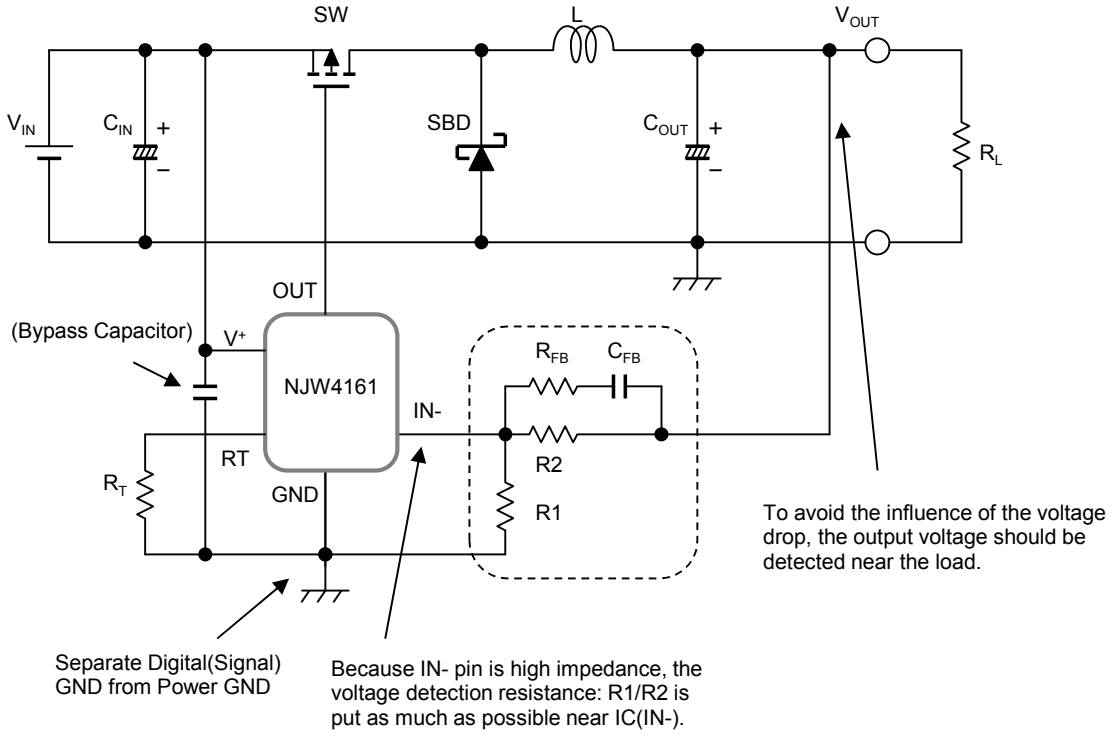
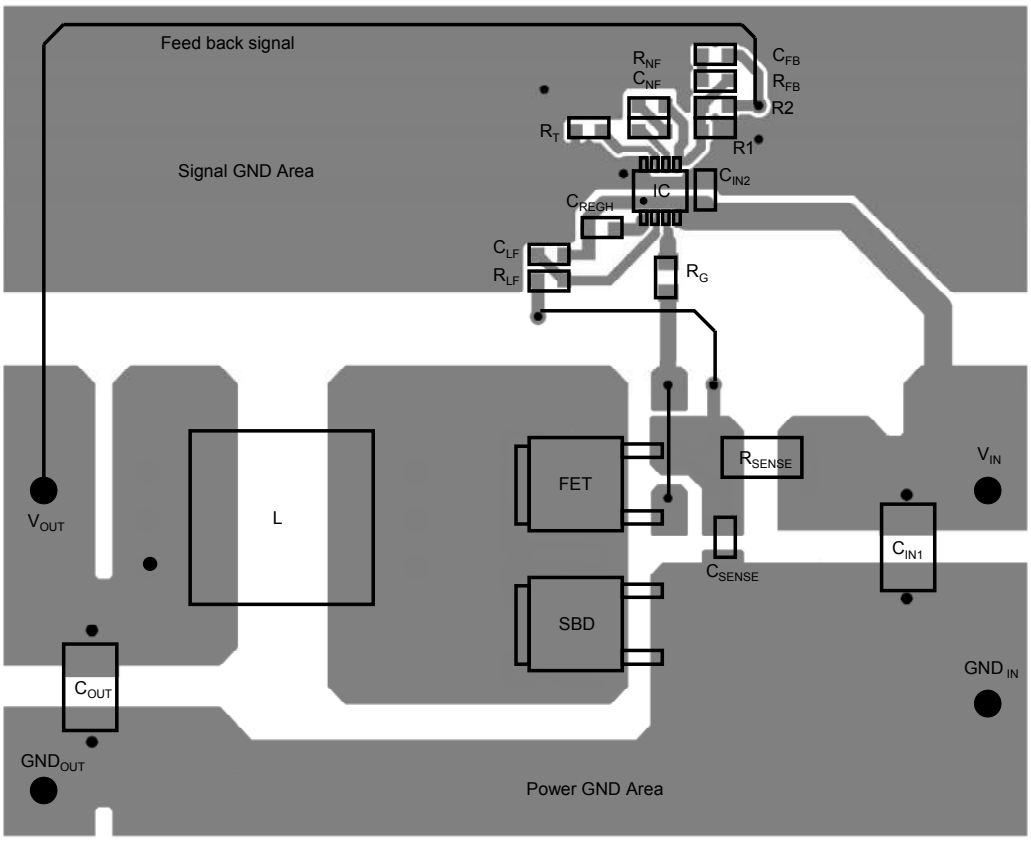


Fig. 11. Board Layout at Buck Converter

■ Application Information (Continued)



Connect Signal GND line and Power GND line on backside pattern

Fig. 12. Layout Example (top view)

■ Calculation of Package Power

You should consider derating power consumption under using high ambient temperature.
Moreover, you should consider the power consumption that occurs in order to drive the switching element.

Supply Voltage:	V^+
Quiescent Current:	I_{DD}
Oscillating Frequency:	f_{OSC}
Gate charge amount:	Qg

The gate of MOSFET has the character of high impedance. The power consumption increases by quickening the switching frequency due to charge and discharge the gate capacitance. Power consumption: P_D is calculated as follows.

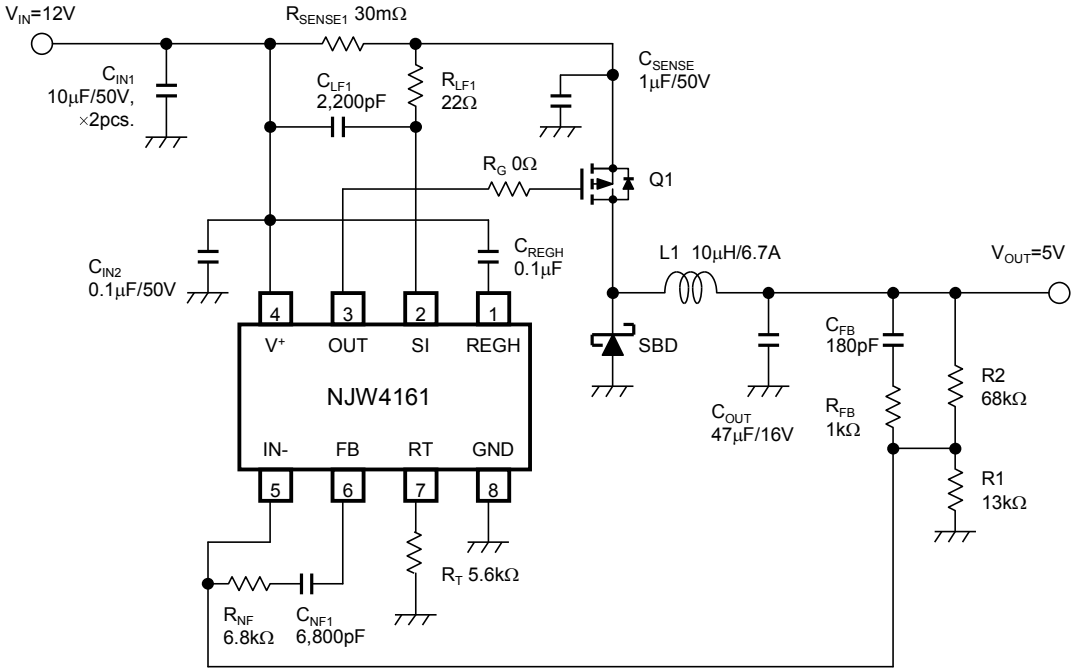
$$P_D = (V^+ \times I_{DD}) + (V^+ \times Qg \times f_{OSC}) \text{ [W]}$$

You should consider temperature derating to the calculated power consumption: P_D.
You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics.

■ Application Design Examples

● Step-Down Application Circuit

Input Voltage: V_{IN}=12V
Output Voltage: V_{OUT}=5V
Output Current: I_{OUT}=3A
Oscillation frequency: fosc=345kHz



Reference	Qty.	Part Number	Description	Manufacturer
IC1	1	NJW4161R	MOSFET Drive Switching Regulator for Buck Converter IC	New JRC
Q1	1	FDD4243	Pch MOSFET 40V, 14A	Fairchild
L1	1	CLF12555T-100M	Inductor 10μH, 6.7A	TDK
SBD	1	DE5SC4M	Schottky Diode 40V, 5A	Shindengen
C_{IN1}	2	UMK325BJ106MM-P	Ceramic Capacitor 3225 10μF, 50V, X5R	Taiyo yuden
C_{IN2}	1	0.1μF	Ceramic Capacitor 1608 0.1μF, 50V, B	Std.
C_{OUT}	1	GRM32EB31C476KE15L	Ceramic Capacitor 3225 47μF, 16V, B	Murata
C_{REGH}	1	0.1μF	Ceramic Capacitor 1608 0.1μF, 25V, B	Std.
C_{NF1}	1	6,800pF	Ceramic Capacitor 1608 6,800pF, 50V, B	Std.
C_{FB}	1	180pF	Ceramic Capacitor 1608 180pF, 50V, CH	Std.
C_{LF1}	1	2,200pF	Ceramic Capacitor 1608 2,200pF, 50V, B	Std.
C_{SENSE}	1	UMK212BJ105KG-T	Ceramic Capacitor 2012 1μF, 50V, B	Taiyo yuden
R1	1	13kΩ	Resistor 1608 13kΩ, ±1%, 0.1W	Std.
R2	1	68kΩ	Resistor 1608 68kΩ, ±1%, 0.1W	Std.
R_{NF}	1	6.8kΩ	Resistor 1608 6.8kΩ, ±5%, 0.1W	Std.
R_{FB}	1	1kΩ	Resistor 1608 1kΩ, ±5%, 0.1W	Std.
R_G	1	0Ω (Short)	Resistor 1608 0Ω, 0.1W	Std.
R_{SENSE1}	1	LPS1R030FE	Current Sense Resistor 30mΩ, ±1%, 1W	Hokuriku Electric Industry
R_{LF1}	1	22Ω	Resistor 1608 22Ω, ±5%, 0.1W	Std.
R_T	1	5.6kΩ	Resistor 1608 5.6kΩ, ±1%, 0.1W	Std.

■ Application Design Examples (Continued)

● Setting Oscillation Frequency

From the Oscillation frequency vs. Timing Resistor Characteristic, R_T=5.6 [kΩ], t=2.9 [μs] at fosc=345kHz.

Step-down converter duty ratio is shown with the following equation:

$$\text{Duty} = \frac{V_{OUT} + V_F}{V_{IN}} \times 100 = \frac{5 + 0.4}{12} \times 100 = 45\ [\%]$$

Therefore, t_{ON}=1.31 [μs], t_{OFF}=1.59 [μs]

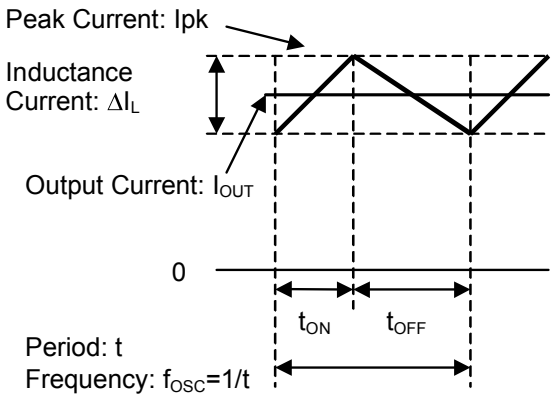


Fig. 13. Inductor Current Waveform

● Selecting Inductance

ΔI_L is Inductance ripple current. When to ΔI_L= output current 30%:

$\Delta I_L = 0.3 \times I_{OUT} = 0.3 \times 3 = 0.9$ [A]

This obtains inductance L. V_{DS_RON} is drop voltage by MOSFET on resistance.

$$L = \frac{V_{IN} - V_{DS-RON} - V_{OUT}}{\Delta I_L} \times t_{ON} = \frac{12 - 0.2 - 5}{0.9} \times 1.31\mu = 10\ [\mu H]$$

Inductance L is a theoretical value. The optimum value varies according such factors as application specifications and components. Fine-tuning should be done on the actual device.

This obtains the peak current Ipk at switching time.

$$Ipk = I_{OUT} + \frac{\Delta I_L}{2} = 0.3 + \frac{0.9}{2} = 3.45\ [A]$$

The current that flows into the inductance provides sufficient margin for peak current at switching time.
In this application circuit example, use L=10μH/6.7A.

● Setting Over Current Detection

In this application circuit example, current limitation value: I_{LIMIT} is set to Ipk=4A.

$I_{LIMIT} = V_{IPK} / R_{SC}$ = 120mV / 30mΩ =4 [A]

The limit value increases slightly according to the response time between the overcurrent detection with the SI pin and the OUT pin outputs stop signal.

$$I_{LIMIT\_DELAY} = I_{LIMIT} + \frac{V_{IN}}{L} \times t_{DELAY} = 4.0 + \frac{12}{10\mu} \times 80n = 4.1\ [A]$$

■ Application Design Examples (Continued)

● Selecting the Input Capacitor

The input capacitor is an important component to decrease power line impedance. The input capacitor selection should be determined by the input ripple current and the maximum input voltage of the capacitor rather than its capacitance value.

The effective input current can be expressed by the following formula:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ [A]}$$

In the above formula, the maximum current is estimated when $V_{IN} = 2 \times V_{OUT}$, and the result in this case is:

$I_{RMS} = I_{OUT\,(MAX)} \div 2$.

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

● Selecting the Output Capacitor

The output capacitor is an important component that determines output ripple noise. Equivalent Series Resistance (ESR), ripple current and capacitor breakdown voltage are important in determining the output capacitor.

The output ripple noise can be expressed by the following formula:

$$V_{ripple\,(p-p)} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right) \text{ [V]}$$

When selecting output capacitance, select a capacitor that allows for sufficient ripple current.

The effective ripple current that flows in a capacitor (I_{rms}) is calculated by the following equation:

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} = \frac{0.9}{2\sqrt{3}} = 260 \text{ [mArms]}$$

Considering sufficient margin, use a capacitor that fulfills the above spec.

In this application circuit example, use C_{OUT}=47μF/16V.

● Setting Output Voltage

The output voltage V_{OUT} is determined by the relative resistances of R1, R2. The current that flows in R1, R2 must be a value that can ignore the bias current that flows in ER AMP.

$$V_{OUT} = \left(\frac{R2}{R1} + 1 \right) \times V_B = \left(\frac{68k}{13k} + 1 \right) \times 0.8 = 4.98 \text{ [V]}$$

■ Compensation design example

A switching regulator requires a feedback circuit for stable output. Because the frequency characteristics of the application change according to an inductance, an output capacitor and so on, the ideal compensation constant is to keep the necessary phase for stable operation and to obtain the maximum band.

The tuning with an actual application is important to determine the compensation constants. Therefore, to finally select the constants with measurement in consideration of the application specifications.

● Feedback and Stability

Basically, the feedback loop should be designed as the open loop phase shift at the point where the loop gain is 0 dB is less than -180°. Furthermore, the loop characteristics should have margin in consideration of ringing and oscillation tolerance caused by load fluctuations. The feedback circuit of the NJW4161 can be arbitrarily be designed. Therefore to enable optimizing the poles and zeros which are important parameters for loop compensation.

The characteristics of the poles and zeros are shown in Fig. 14.
Poles: The gain has a slope of -20 dB/dec, and the phase shifts -90°.
Zeros: The gain has a slope of +20 dB/dec, and the phase shift +90°.

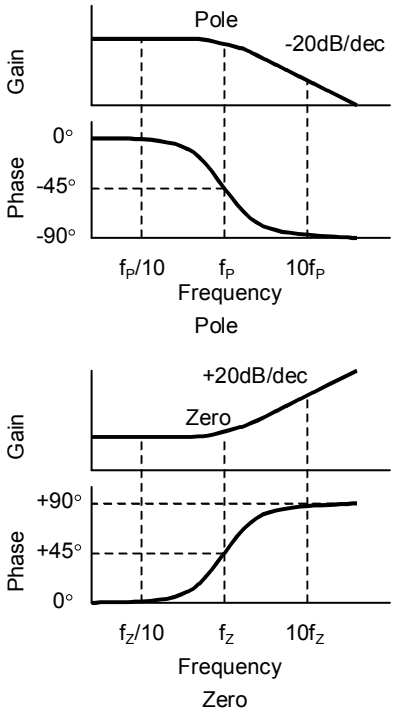


Fig. 14. Characteristics of Pole and Zero

If the number of factors constituting poles is defined as “n”, the change in the gain and phase will be “n”-fold. This also applies to zeros as well. The poles and zeros are in a reciprocal relationship, so if there is one factor for each pole and zero, they will cancel each other.

● Configuration of the compensation circuit

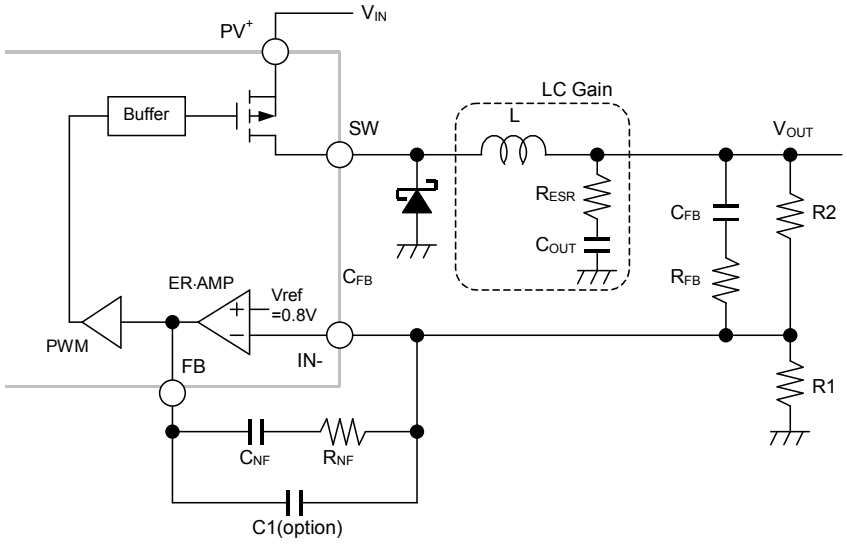


Fig. 15. Compensation Circuit Configuration

■ Compensation Design (Continued)

● Poles and zeros due to the inductance and output capacitor

Double poles $f_{P(LC)}$ are generated by the inductance and output capacitor. Simultaneously, single zeros $f_{Z(ESR)}$ are generated by the output capacitor and ESR. Each pole and zero is expressed by the following formula:

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}} \qquad f_{P(LC)} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

If the ESR of the output capacitor is high, $f_{Z(ESR)}$ will be located in the vicinity of $f_{P(LC)}$. In such application, the zero $f_{Z(ESR)}$ compensates the double poles $f_{P(LC)}$ and it has tendency for stability accordingly.

However, if the ESR of the output capacitor is low, $f_{Z(ESR)}$ shifts to the high frequency and the phase is shifted -180° by $f_{P(LC)}$. The NJW4161 compensation circuit can compensate by using zeros of f_{Z1} and f_{Z2}.

● Poles and zeros due to error amplifier

The single poles and zeros generated by the error amplifier are obtained using the following formula.

Zero	Pole
$f_{Z1} = \frac{1}{2\pi C_{NF} R_{NF}}$	$f_{P1} = \frac{1}{2\pi C_{NF} A_V \left(\frac{R1 R2}{R1 + R2} \right)}$ (Av: Amplifier Open Loop Gain=80dB)
$f_{Z2} = \frac{1}{2\pi C_{FB} R2}$	$f_{P2} = \frac{1}{2\pi C_{FB} \left(R_{FB} + \frac{R1 R2}{R1 + R2} \right)}$
	$f_{P3} = \frac{1}{2\pi C1 R_{NF}}$ (Option)

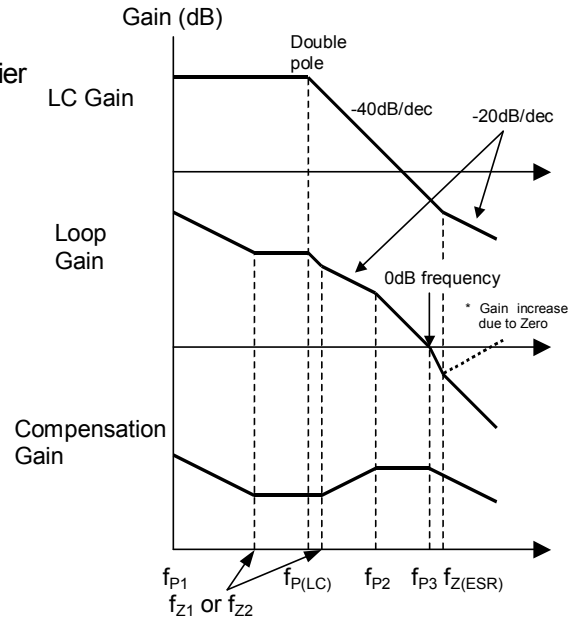


Fig16. Loop Gain examples

f_{Z1} and f_{Z2} are located on both sides of $f_{P(LC)}$.

Because the inductance and the output capacitor vary, they are each set using the following as a rough guide:

$f_{P(LC)} \times$ 0.5-fold to 0.9-fold

$f_{P(LC)} \times$ 1.1-fold to 2.0-fold

There is also a method in which f_{Z1} and f_{Z2} are located at positions lower than $f_{P(LC)}$. Because there is a tendency to increase the phase shift and the gain becomes high, it can be expected that the response will improve.

However, there is a tendency for the phase margin to become insufficient, so care is necessary.

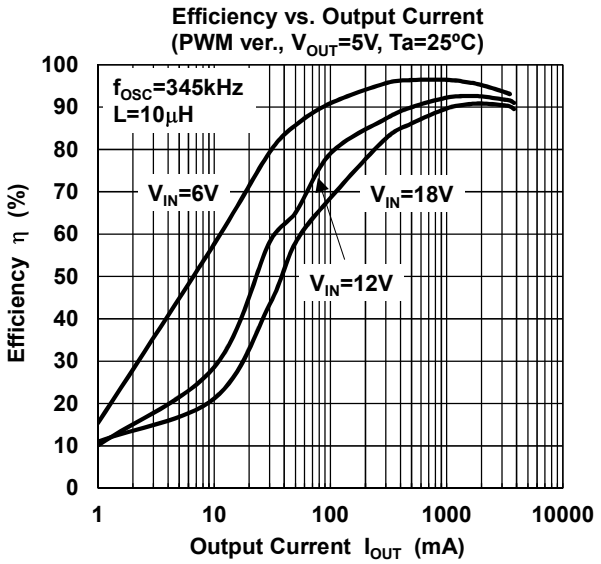
The f_{P1} creates poles in the low frequency band due to the Miller effect of the error amplifier. The stability becomes better as f_{P1} becomes lower. On the other hand, the frequency characteristics do not improve, so the response is adversely affected. The f_{P1} is set a frequency gain of $f_{P(LC)}$ is 20dB as a rough guide.

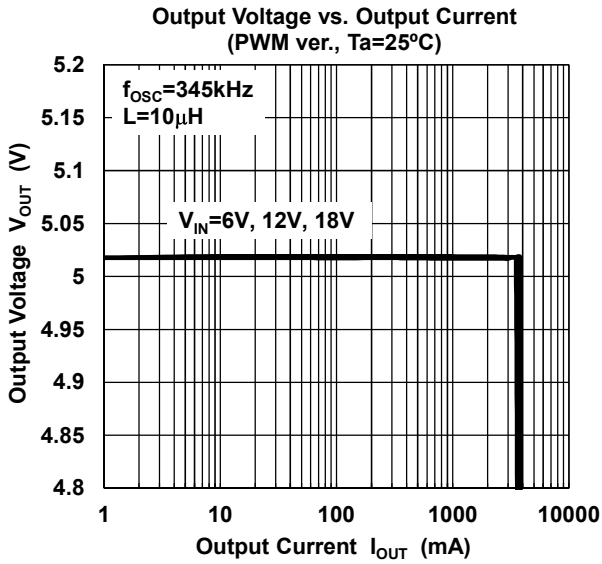
If the open loop gain of the error amplifier is made 80 dB, design is carried out using $f_{P1} < f_{P(LC)} \div 10^3$ (= 60 dB) as a rough guide.

Above several 100 kHz, various poles are generated, so the upper limit of the frequency range where the loop gain is 0 dB is set to fifth (1/5) to tenth (1/10) of oscillation frequency. The $f_{Z(ESR)}$ in the high frequency region sometimes causes a loop gain to be generated (See Fig.16 Loop Gain “). Using f_{P2} and f_{P3}, perform adjustment with the NJW4161 in an actual application, so as to adequately reduce the loop gain in the high frequency region.

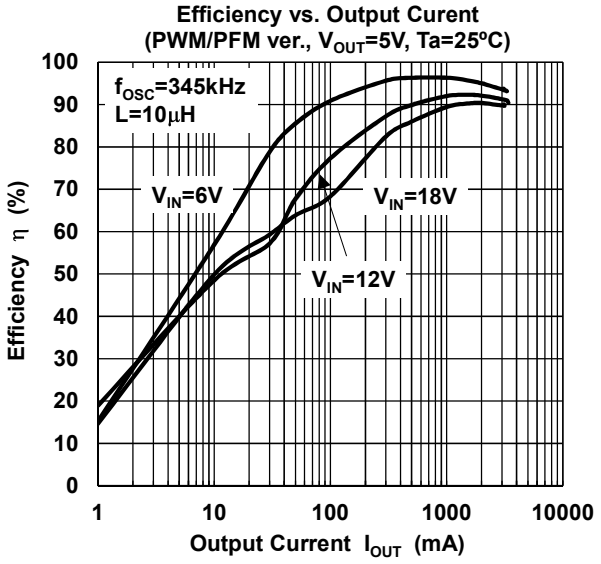
■Application Characteristics

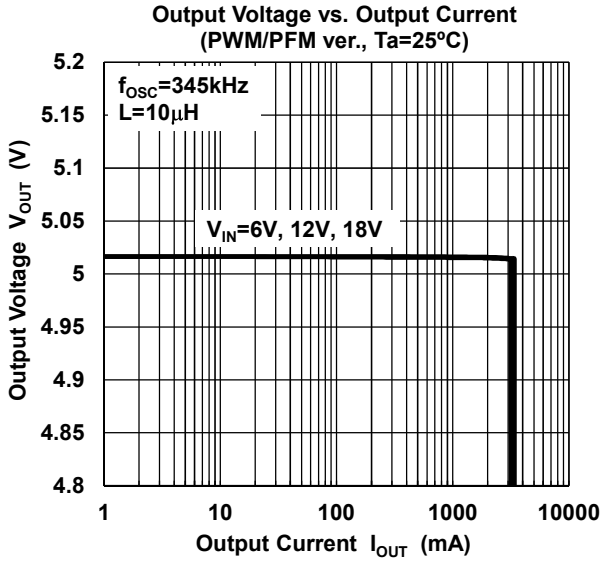
● PWM control : A version, B version





● PWM/PFM Control : C version





MEMO

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