FUSB251

Type-C CC and SBU Protection IC

ON Semiconductor®

www.onsemi.com

WLCSP15, 1.49x2.06x0.574
CASE 567WV

PRODUCT SUMMARY

General Description

The FUSB251 is an I2C controlled switch with over voltage protection on CC and SBU pins in Type−C interface port. The device has SPST switches on CC1/2 and SBU1/2 which enable automatically with valid VDD so that Type−C/PD controller can use the over voltage protected CC path. The FUSB251 has dead battery mode, CC pulled down with Rd, where Source device can provide Vbus for battery charging. Another feature in FUSB251 is moisture detection on both CC and SBU paths with ADC detection. Once moisture is detected, and Interrupt is generated and the corresponding register is updated to notify host. The device has on−chip IEC protection with surge protection on both CC and SBU. Both CC and SBU ports are 24 V DC tolerant. Package type is WLCSP with 15 ball 3x5 array.

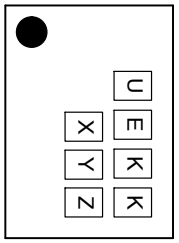
Features

- Low Ron SPST Switches on both CC1/2 and SBU1/2 Path for Type−C
- Dead Battery Mode Provides Default Rd Presenting on CC1/2
- 24 V DC Tolerant on CC and SBU
- ±35 V Surge Protection on CC and SBU
- Over Voltage Protection on CC and SBU
- I2C Interface with Processor with Interrupt for event Notification
- Moisture Detection on CC and SBU Pins
- On−chip IEC ESD Protection with External Capacitor on CAP Pin
- CC Ron 0.3 Ω Typical
- SBU Ron 3 Ω Typical
- 50 MHz Bandwidth on SBU Switch
- 15 ball WLCSP

Applications

- Smart Phones
- Tablets, Netbooks, Ultra−Mobile PCs
- Gaming Devices and E−books
- Portable Devices with Li−ion Battery
- Car Cigarette Jack
- External USB Storage

MARKING DIAGRAM



UE	= 2−digit Device Identifier
KK	= 2−digit Lot Run Code
XY	= 2−digit Date Code
Z	= 1−digit Plant Code
●	= Pin A1 Mark

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

APPLICATION DIAGRAM

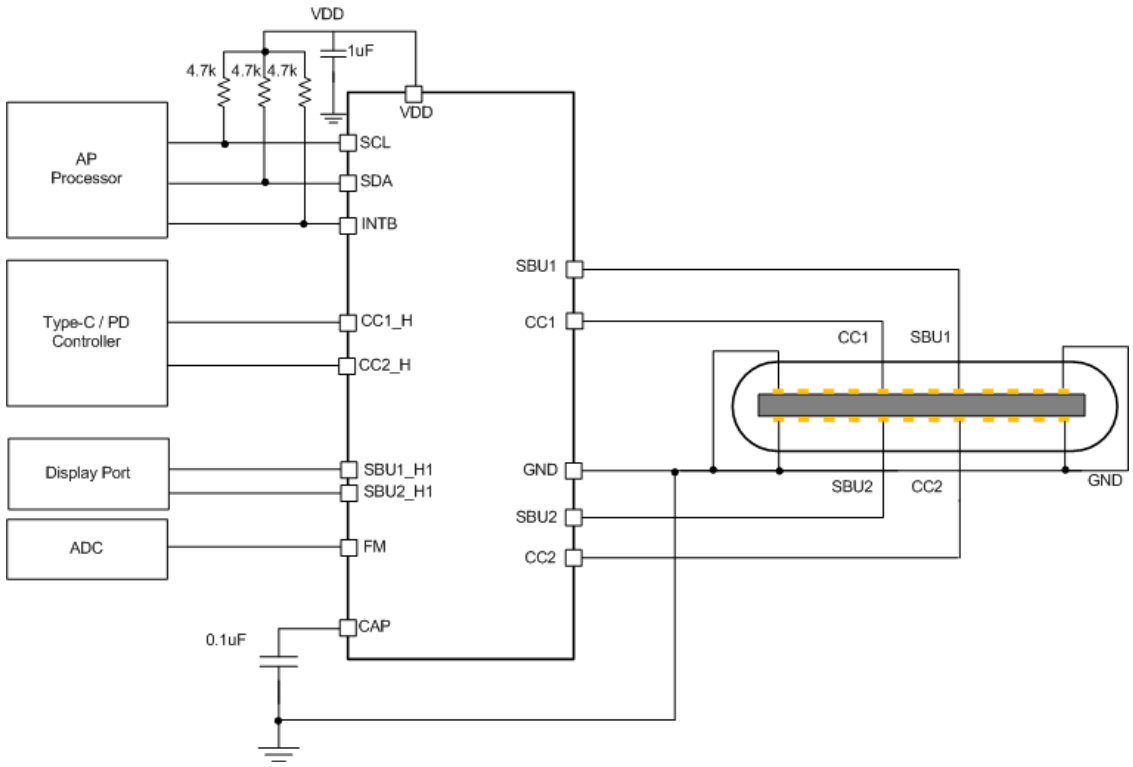


Figure 1. Application Diagram

PART NUMBERING

ORDERING INFORMATION

Part Number	Temperature Range	Package	Packing Method †
FUSB251UCX	−40 to 85°C	WLCSP, 3 x 5 array, 15 ball, 1.49 mm x 2.06 mm	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PRODUCT PIN ASSIGNMENTS

Pin Configuration

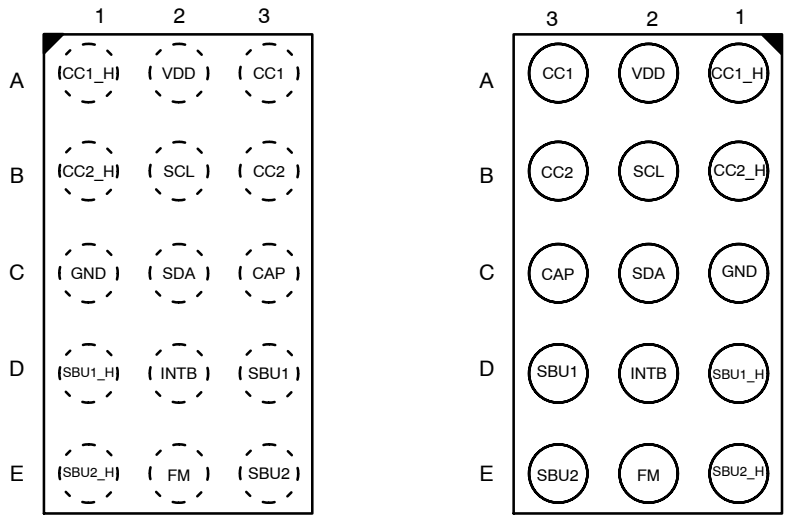


Figure 2. Pin Configuration

Pin Descriptions

PIN DESCRIPTIONS

Pin#	Name	Type	Description
C1	GND	Ground	GND
A2	VDD	Power	Power
A3	CC1	I/O	Type−C CC interface. Connect to USB Type−C connector CC1 pin
B3	CC2	I/O	Type−C CC interface. Connect to USB Type−C connector CC2 pin
A1	CC1_H	I/O	Type−C CC Host interface, Connect to USB Type−C controller CC1 pin
B1	CC2_H	I/O	Type−C CC Host interface, Connect to USB Type−C controller CC2 pin
D3	SBU1	I/O	Type−C SBU interface, Connect to USB Type−C connector SBU1 pin
E3	SBU2	I/O	Type−C SBU interface, Connect to USB Type−C connector SBU2 pin
D1	SBU1_H	I/O	Type−C SBU Host Interface, Connect to Host side SBU1 application pin
E1	SBU2_H	I/O	Type−C SBU Host Interface, Connect to Host side SBU2 application pin.
E2	FM	I/O	Factory test mode pin, Connect to ADC input of host processor. If not used, connect to GND. FM can be switched over to one of SBU.
C3	CAP	O	Capacitor pin, Connect to 0.1 μF capacitor to GND
B2	SCL	Open Drain Input	I^2C interface, Pull up to Vdd is required, Connect to SCL pin of Processor
C2	SDA	Open Drain I/O	I^2C interface, Pull up to Vdd is required, Connect to SDA pin of Processor
D2	INTB	Open Drain Output	Interrupt for Host alert, Pull−up to VDD required, Connect to processor Interrupt input

PRODUCT BLOCK DIAGRAM

Block Diagram

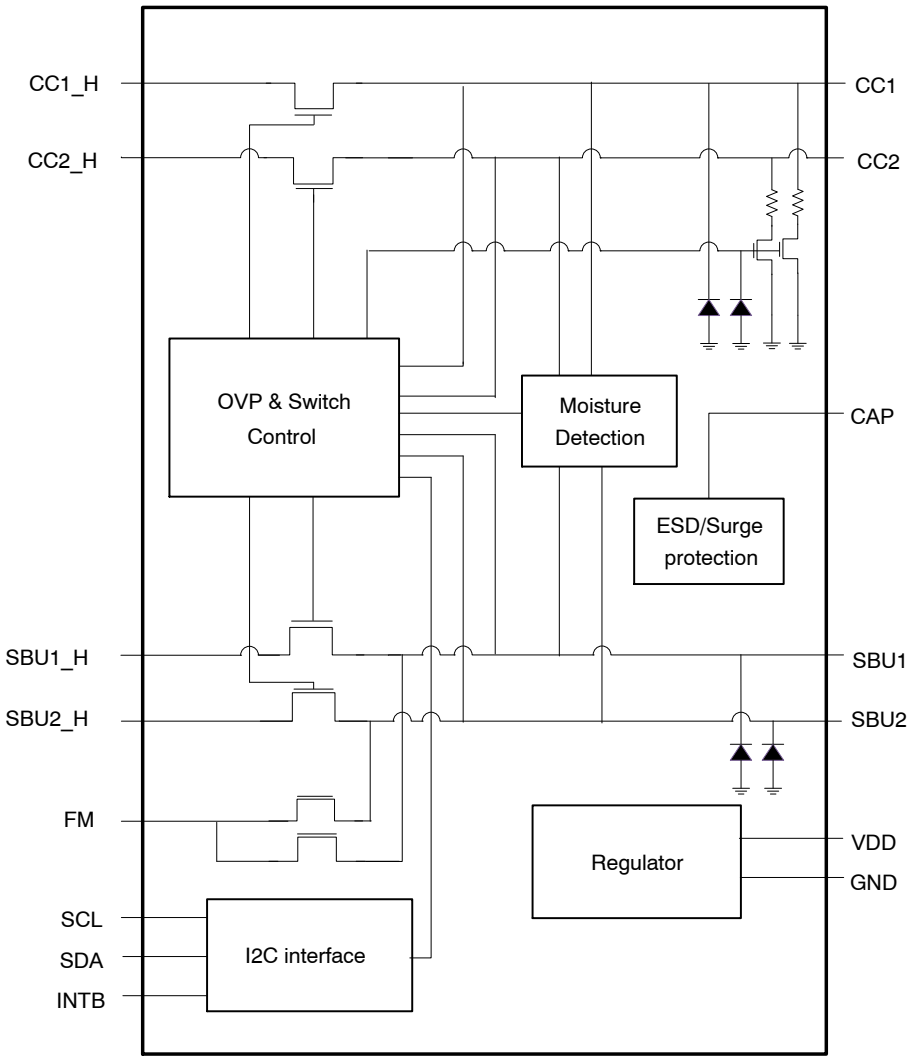


Figure 3. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_J	Junction Temperature		−40		+150	°C
T_{STG}	Storage Temp		−65		+150	°C
VDD	Supply voltage	Slew Rate 2 V/μs (rising), 1 V/μs (falling)	−0.5		12.0	V
VCC	Vccx to GND		−0.5		24	V
VSBU	VSBUx to GND		−0.5		24	V
VCCx_H and VSBUx_H	VCCX_H, VSBUx_H to GND		−0.5		6.0	V
ICCSW	DC CC switch current				1.25	A
ISBUSW	DC SBU switch current				100	mA
IIK	DC input diode current		−50			mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ESD RATINGS – JEDEC / IEC SPECIFICATION

Electro Static Discharge (ESD) Specifications	Condition		Value	Unit
Human Body Model, JEDEC JESD22−A114	CCx and SBUx pins to GND		±5000	V
	Other pins		±2000	
Charged Device Model, JEDEC JESD22−C101	All pins		±1000	
IEC 61000−4−2 System ESD	CCx and SBUx pins to GND	Air−gap Discharge	±15000	
		Contact Discharge	±8000	
IEC 61000−4−5 Lightning and Surge	CCx and SBUx pins to GND		±35	

OPERATING CONDITIONS

Symbol	Parameter	Conditions	MIn	Typ	Max	Unit
VDD	Supply Voltage Range		2.7	3.8	5.5	V
T_A	Operating Ambient Temperature		−40		+85	°C
T_{IN} + 0.3	Junction Temperature		−40		+125	°C
VCCx, VCCx_H	CC1 CC2, CC1_H, CC2_H voltage		0		5.5	V
VSBUx, VSBUx_H	SBU1, SBU2, SBU1_H, SBU2_H voltage		0		4.2	V
C_CAP	External capacitor capacitance			0.1	1.0	μF
VPU	Pull up resistor power rail of SDA, SCL and INTB		1.7		VDD	V
ICCSW	CC switch current	T_A = 25°C and T_A = 85°C			1000 (T_A = 25°C), 800 (T_A = 85°C)	mA
ISBU	SBU switch current				50	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL SPECIFICATION TABLE Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and VDD = 3.8 V unless otherwise specified.

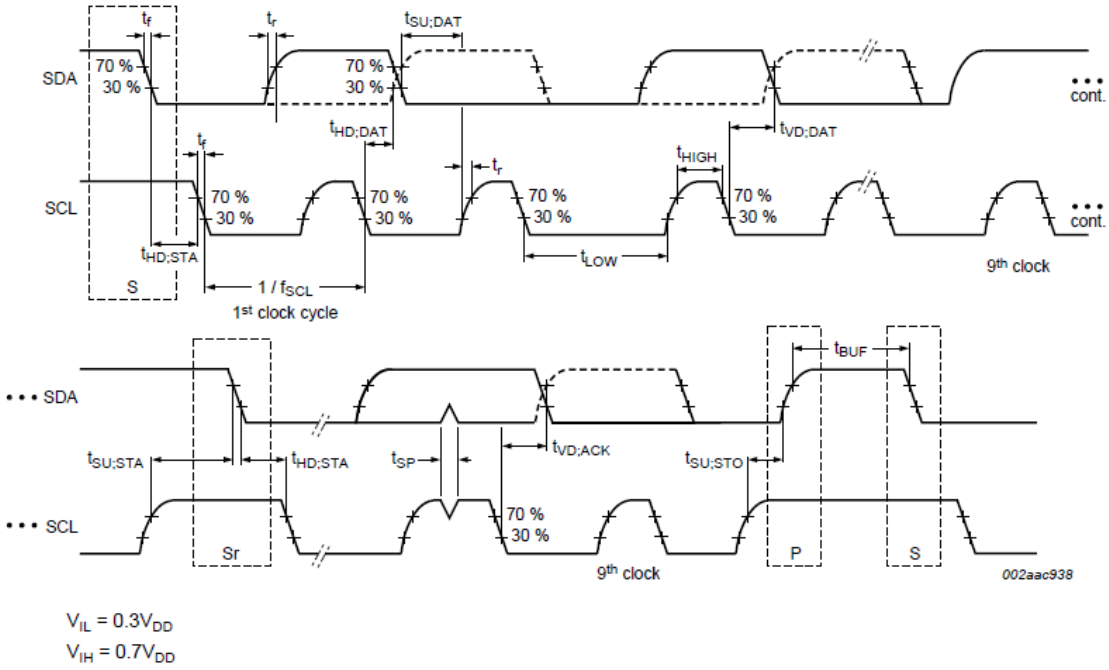
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent supply current	VDD = 2.7 to 5.5 V, Switch is closed, no load, moisture detection is not enabled		15		μA
I_{MOS}	Current with moisture detection enabled	VDD = 2.7 to 5.5 V, Switch is closed, CC toggle and CC moisture detection is enabled, Avg for 1 sec		30		μA
I_{DRY}	Current consumption when Dry check is working on	VDD = 2.7 to 5.5 V, Moisture detected, and Dry check enabled, T(PD, period) = 4 sec		15		μA
I_{OFF}	Power off leakage current	VDD = 0 V, Except CC1/CC2		1		μA
V_{UVLO}	Under voltage Lockout	VDD Rising, VDD Falling		2.45 (Rising), 2.40 (Falling)	2.55 (Rising)	V
T_{SD}	Thermal Shut down	Shutdown Threshold/ Return from Shutdown/ Hysteresis		150°C (shutdown), 130°C (Return), 20°C (Hysteresis)		
I_{CC_LEAK}	CC ON leakage current	VDD = 2.7 to 5.5 V, CC Switch closed, CCx_H float, measure leakage from CCx with 3.3 V			0.5	μA
R_{ON_CC}	CC1, CC2 RON resistance	VDD = 2.7 to 5.5 V, IOUT = 200 mA		300		mΩ
$R_{Flatness\_CC}$	VDD = 2.7 to 5.5 V, Vcc swing = 0 V – 1.2 V			10		mΩ
V_{OVP_CC}	CC over voltage protection threshold	VDD = 2.7 to 5.5 V, VCC rising	5.70	5.85	6.00	V
$V_{OVP\_CC\_FALL}$	CC recover threshold when voltage on CC is falling	VDD = 2.7 V to 5.5 V		5.70		V
$V_{OV\_HYS\_CC}$	CC OVP threshold Hysteresis	VDD = 2.7 to 5.5 V			0.15	V
t_{CC_OVP}	CC OVP Trip time (Note 1)	VDD = 2.7 to 5.5 V, CCx rise from 4 V to 6 V with 1 V/ns slew rate, RL = 30 Ω on CCx_H		250		ns
Rd_CC	Dead battery pull down resistance	VDD = 0 to UVLO, Dead battery resistance / Voltage on pin	4.1	5.1	6.1	kΩ
V_{OVP_SBU}	SBU over voltage threshold	VDD = 2.7 to 5.5 V, SBU Rising	4.4	4.5	4.7	V
$V_{OVP\_SBU\_FALL}$	SBU OVP recovery threshold when voltage on SBU is falling	VDD = 2.7 V to 5.5 V		4.35		V
$V_{OV\_SBU\_HYS}$	SBU OVP Hysteresis	VDD = 2.7 to 5.5 V, Measure difference between SBUX rising and falling OVP threshold			0.15	V
$I_{SBU\_ON\_LEAK}$	SBU ON leakage current	VDD = 2.7 to 5.5 V, Switch closed, SBUx_H floating, measure leakage @1 V SBU Note (SBU ON leakage spec is different depending on temperature) (Note 1)		1	5 @85°C, 15 @100°C	nA
$I_{SBU\_OFF\_LEAK}$	SUB OFF leakage from SBUx	VDD = 2.7 to 5.5 V, Switch open, Measure leakage current from SBUx with 0 – VDD	−0.5		0.5	μA
R_{ON_SBU}	SBU1, SBU2 Switch ON resistance	VDD = 2.7 to 5.5 V, VSW_SBU = VDD, ISBU_ON = −8mA		3	5	Ω
$R_{Flatness\_SBU}$	SBU RON Flatness	VDD = 2.7 to 5.5 V, VSBU Swing = 0 – VDD		0.1		Ω
T_{OVP_SBU}	SBU OVP response time (Note 1)	VDD = 2.7 to 5.5 V, SBUx rise from 4 V to 6 V with 1 V/ns. RL = 30 Ω on SBUx_H		0.5		μs
R_{ON_FM}	FM to SBU1 or SBU2 ON resistance	VDD = 2.7 to 5.5 V, Close FM to SBU1 or SBU2 switch, VSW_SBU = VDD, ISBU_ON = −8 mA		15		Ω
$R_{Flatness\_FM}$	FM to SBU1/SBU2 switch Rflatness	VDD = 2.7 to 5.5 V, VSBU_Swing = 0 – VDD		0.1		Ω
C_{ON_CC}	CC Switch ON capacitance (Note 1)	VDD = 2.7 to 5.5 V, VCC_SW = 0 – 1.2 V, f = 400 kHz		50		pF

ELECTRICAL SPECIFICATION TABLE Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and VDD = 3.8 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ON_SBU}	SBU Switch ON capacitance (Note 1)	VDD = 2.7 to 5.5 V, Capacitance from SBUx or SBUx_H to GND. Switch closed, VSW = 0 – VDD,		25		pF
BW_{CC}	CC channel bandwidth (Note 1)	VDD = 3.6 V, –3 dB bandwidth, RL = 50 Ω, CL = 200 pF		25		MHz
BW_{SBU}	SBU switch Bandwidth (Note 1)	VDD = 3.6 V, –3 dB bandwidth between SBUx and SBUx_H. Singled ended, RL = 50 Ω		30		MHz
T_{CC_MOS}	Timer of CC moisture detection (Note 1)	VDD = 2.7 to 5.5 V, Timer for searching both CC rise. Timer reset at both CC rising.	108	120	132	ms
T_{DRY}	Dry check period (Note 1)	VDD = 2.7 to 5.5 V, Timer period of SBU moisture detection for Dry check, Programmable	0.1		10	s
T_{SBU_PRD}	Time between SBU1 and SBU2 moisture detection (Note 1)	VDD = 2.7 to 5.5 V, SBU moisture detection enabled and measure time voltage source on from SBU1 to SBU2	0.9	1.0	1.1	ms
$V_{CC\_RISE\_MOS}$	Moisture detection start voltage when both CC1 and CC2 rise	VDD = 2.7 to 5.5 V	130	200	270	mV
V_{OUTL_INTB}	INTB output Low voltage	VDD = 2.7 to 5.5 V			0.4	V
V_{IH_I2C}	SDA, SCL High level input voltage	VDD = 2.7 to 5.5 V	1.2			V
V_{HYS_I2C}	SDA, SCL Hysteresis of Schmitt Trigger Inputs	VDD = 2.7 to 5.5 V	200			mV
I_{I2C}	Input Current of SDA and SCL Pins	VDD = 2.7 to 5.5 V, Input Voltage 0 to VDD	–0.5		0.5	μA
ICCT_I2C	VDD current when SDA or SCL is HIGH	Input voltage is 1.8 V	–0.5		2.5	μA
V_{OL_SDA}	Low–Level Output Voltage	VDD = 2.7 to 5.5 V, 2 mA sink current, Pull up to VDD	0		0.3	V
C_{I2C}	Capacitance on SDA and SCL (Note 1)	VDD = 2.7 to 5.5 V			10	pF
f_SCL	I2C SCL clock frequency				400	kHz
tHD ; STA	Hold Time (Repeated) START Condition		0.6			μs
tLOW	LOW Period of I2C_SCL Clock		1.3			μs
tHIGH	High Period of I2C_SCL Clock		0.6			μs
tSU ; STA	Set–up Time for Repeated START Condition		0.6			μs
tHD ; DAT	Data Hold Time		0		0.9	μs
tSU ; DAT	Data Set–up Time		100			ns
tR	Rise Time of I2C_SDA and I2C_SCL Signals		20 × (VDD/5.5 V)		250	ns
tF	Fall Time of I2C_SDA and I2C_SCL Signals		20× (VDD/5.5 V)		250	ns
tSU ; STO	Set–up Time for STOP Condition		0.6			μs
tBUF	BUS–Free Time between STOP and START Conditions		1.3			μs
tSP	Pulse Width of Spikes that Must Be Suppressed by the Input Filter		0		50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by Design, Characterization, not Production tester.



$V_{IL} = 0.3V_{DD}$

$V_{IH} = 0.7V_{DD}$

Figure 4. Definition of Timing for Full−Speed Mode Devices on the I2C Bus

FUNCTIONAL SPECIFICATIONS

POR and Reset

The FUSB251 closes both CC and SBU switches with a valid VDD supply after Power On reset. Until valid VDD is supplied, FUSB251 presents Rd on both CC1 and CC2 so that a source device can provide Vbus and Type−C controller can present Rd continuously after POR so VBUS will be consistent. At UVLO condition which is 2.4 volt (falling), CC and SBU switches get open again and Rd will be presented on both CC.

There is device reset register, bit0 in 0x0B register. If the register bit is set, all registers in the device are set to default, so momentarily both switches will be open and closed back.

CC and SBU Switch Characteristics

The FUSB251 has 2x SPST switches on both CCx and SBUx with OVP feature. Both CC and SBU switch paths are closed automatically with valid Vdd supply. CC switch is used for Type−C / PD communication channel. Also Vconn can be provided through the switch from CCx_H to CCx. Up to 1A Vconn current can be provided over the low Ron(0.3 Ω) path. Both CCx and SBUx pins are 24 volt DC−tolerant. SBU switch can be used for DisplayPort Aux channels following USB PD Alternative mode or UART.

Dead Battery Mode

Upon dead battery condition, the both CC1/2 ports present Rd(5.1 kΩ) pull down to allow a Type−C source device to attach and provide Vbus to the sink which is under dead battery mode. Once system power comes back and valid VDD supplied to FUSB251, the dead battery Rd is removed and both CC switches are closed. Then, Type−C / PD controller can detect the attached Type−C source device.

Over Voltage Protection

When an over−voltage event is detected on either CCx or SBUx, the FUSB251 will activate OVP circuit to open the switch within tOVP. The OVP event is independent between CC and SBU. Any CC channel OVP opens the CC1 and CC2 switch path only, and SBU switch is keep closed. OVP on SBU opens the SBU switch only. Upon the detection of an over−voltage event, the INTB pin is asserted low to notify processor with register update.

When OVP condition is removed from the port, the switch path is closed automatically and OVP recovery interrupt is generated to notify processor. Getting interrupt service is not required to close the switch back. OVP function is only working on the connector face ports, CCx and SBUx.

FM Pin

FM pin is for Factory test Mode (FM) purpose. When Factory test mode is used over Type−C connector and if host device needs to detect Factory Test fixtures by using ID with ADC function, the FM can be used by connecting FM to ADC input port in the processor. Without any external pull down on FM PIN, FM can be switched to one of SBU pins, default is SBU1 and it can be manually switched over to SBU2 if needed. The other SBU2 or SBU1 pin will be open.

If Factory test mode is not needed, pull down(less than 10 kΩ) or direct connecting to GND makes switch close between SBUx_H and SBUx after POR or reset.

Manual Mode Control

For switch, there is manual mode switch control for CC and SBU switches. Processor can manually open or close the switch paths in the FUSB251 even though both switches are closed in default with valid VDD. Manual mode switch configuration overrides the auto switch control. However, there are exceptions, such as during moisture detection process and OVP event because switch has to be open in these cases. The switch configuration has to be set in the switch control register and then, bit 0 of control register has to be set.

Surge and ESD Protection

The FUSB251 connector facing ports, CCx and SBUx, are designed to endure up to ±35volt surge protection. The voltage can occur when 20 volt DC voltage from VBUS touches the CC and SBU pins with the inductance inside cable. Also, system ESD protection, IEC61000−4−2, is supported with the external capacitor on CAP pin.

Capacitor Recommendation

The CAP pin needs an external capacitor ranges 0.1 μF to 1.0 μF. Recommended capacitor type is X7R which has low capacitance variation with temperature change and 0603 or larger size. Also the capacitor rated voltage is important because the voltage on the CAP could be greater than 35 volt with Surge or hot plug in the Type−C cable so 50 volt or larger rated capacitor is recommended.

Interrupt Service

FUSB251 has INTB pin to notify processor the status change in the device. Any change in the Interrupt register will trigger the INTB pin which is open drain output. INTB is ready after POR or reset without any register set. Once INTB pin is triggered to low, the pin stays low until the interrupt register is read by processor. The interrupt mask registers are default disabled. If any interrupt mask bit is set, the corresponding interrupt register bit won't set, so INTB pin won't be triggered.

I2C Interface

The FUSB251 includes a full I2C slave controller. The I2C slave fully complies with the I2C specification version 6 requirements. This block is designed for fast mode signals. Examples of an I^{2}C write and read sequence are shown in below figures respectively.

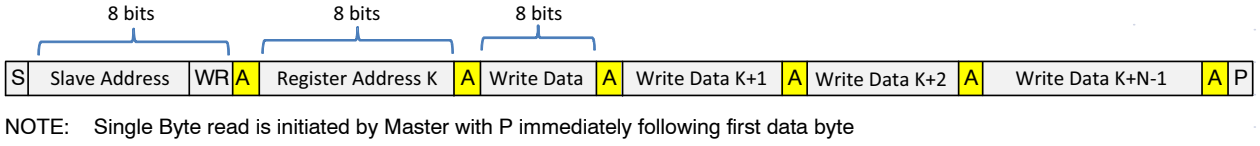


Figure 5. I^{2}C Write Example

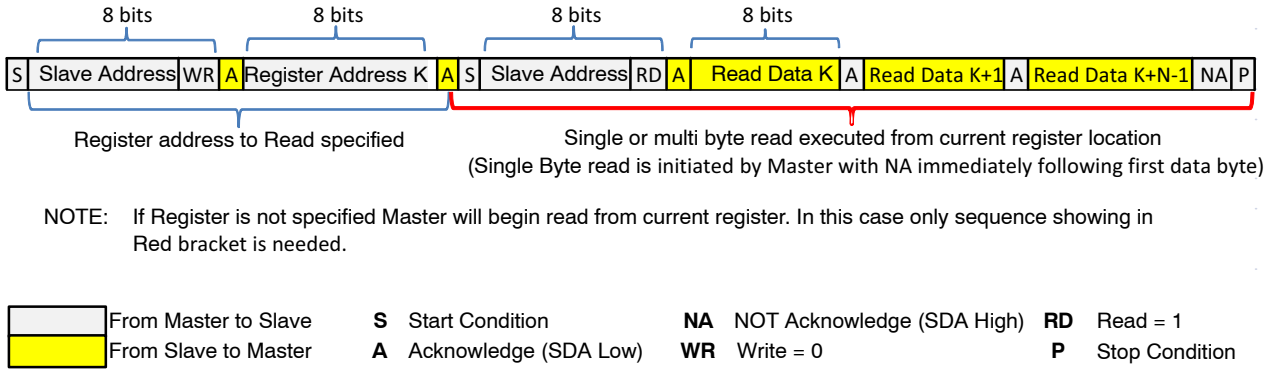


Figure 6. I^{2}C Read Example

SLAVE ADDRESS

Part Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUSB251UCX	0	1	0	1	0	0	0	R(1)/W(0)

Moisture Detection

CC Moisture Detection

Moisture detection is default disabled. Once CC moisture detection is enabled, voltage of both CC1_H and CC2_H are monitored to see if both CCs rise above 170 mV. If they rise above the voltage, moisture detection started on one of the CC first, and moisture detection on the other CC is occurred at the next both CC rising. If only one of CCs rises up above the threshold, in case of source device attach, CC moisture detection does not start.

If both CCs cross the threshold, both CC switches are open momentarily, and FUSB251 supplies 1volt source onto one of CCs with 320 kΩ pull up. And ADC detection is enabled to measure the voltage of the CC channel. Since moisture in connector can make leakage path between the CC pin and other pins including GND, there will be resistance between CC and GND and it can be detected by ADC. Once moisture detection is finished on one CC, the other CC channel is also tried at the next both CC rise. If there is no both CC rise on either CC within 120 ms from the last detection, it will go to timer expire. If source or sink device is attached, the timer will expire. Timer expire is interrupted to host and CC moisture detection stops and moisture detection is continued on SBU float voltage detection instead. To be determined as moisture presence, both CC channels have to be tried and moisture has to be detected on either of channel with no timer expire. If moisture is detected, the result is updated in the register and interrupt is triggered to processor. Regardless of moisture presence on CC, once detection is finished, both CC switches are closed again for Type−C controller to use the CC channel. Moisture detection range can be changed by I2C register, Threshold1 in 0x08. Once the measured resistance is less than the threshold, it will be detected as moisture.

If sink device is attached while host with FUSB251 is on DRP toggle, both CC will rise together, So, CC moisture detection will happen. And, FUSB251 can find the Rd in sink device because the Rd, 5.1 kΩ, is in moisture detection range. But the other CC channel detection will end up as timer expire because there will be no both CC rise after attach. So, the final result will be timer expire and moisture detection will continue on SBU pins.

To support audio and debug accessories which have two terminations on both CC, there is a register bit in the control register, bit7 in 0x02. The register bit makes moisture detection occur on every other both CC rising so moisture detection skips for Type−C detection can happen during the time.

Detection time on CC moisture is dependent on the settling time and number of ADC read, default is 1 time ADC and 400 μs settle time. They can be programmed in Timer2 register, 0x0C.

SBU Moisture Detection

If CC port is on DRP or Source mode, moisture inside connector can make leakage path from CC to SBU, which makes SBU can have float voltage similar to the shape of CC. So the SBU float voltage can be detected if moisture is present while CC is on toggle or SRC mode. SBU float voltage detection can be started with the EN_SBUFT register set. If the bit is set, FUSB251 starts monitoring voltage on both SBU1 and SUB2, and if the voltage on either port is the same or above the threshold, the moisture_status register (0x06, bit 4 and/or 5) is set with an interrupt. With the interrupt, processor can turn off the CC and SBU switch path to protect from corrosion, or processor could further moisture check using force SBU detection.

SBU float voltage detection also can be enabled when CC moisture detection result is timer expire, which can happen where there is no DRP toggle on CC. For example, if CC moisture detection is enabled where Type−C accessory is already plugged−in, the moisture detection will end up timer expire and so SBU float voltage detection will be started instead.

Once SBU float voltage detection is enabled, it keeps monitoring until moisture found. If device is reset or both EN_CC and EN_SBUFT are disabled, the floating detection stops and goes back to disable mode which is idle mode.

Force SBU detection is initiated by EN_SBU or Auto_EN_SBU bit. Auto_EN_SBU bit is for pre−set before moisture is detected, EN_SBU can be set at anytime when SBU moisture detection is needed. After either CC or SBU float voltage detection detected moisture, if Auto_EN_SBU bit is set, FUSB251 goes to moisture detection on SBU with the same way of CC moisture detection, using 1volt source with 320 kΩ pull up, which is secondary moisture detection using SBU. So, Host processor can use force SBU detection in case CC moisture or SBU float voltage detection result is not enough and additional moisture detection is needed.

Force SBU detection makes open the both CC and SBU switches and detects moisture on SBU. Opening CC switch will disconnect the Type−C device and will remove Vbus from Type−C source. The detection time of SBU force detection is 1msec. Device reset or moisture reset bit can be used to close the CC and SBU switch again.

If moisture is present in connector and if source device provides VBUS, there could be OVP interrupt on SBU by leakage path between Vbus and SBU.

Dry Check

Dry check routine can be started after moisture is detected by force SBU detection. After moisture detected on SBU, if EN_DRY bit is enabled, dry check routine is started which is keep checking moisture on SBU every second or up to 10second. The Dry check timer can be set in the register, 0x0A, timer register. Also, the moisture threshold can be set in the Threshold2 register, 0x09. If Dry condition is reached, Interrupt is generated to let host know the change, then processor has to disable all the moisture detection or moisture reset to go to idle mode. If moisture reset bit is set after Dry condition reached, the moisture detection state machine will restart based on control register bits.

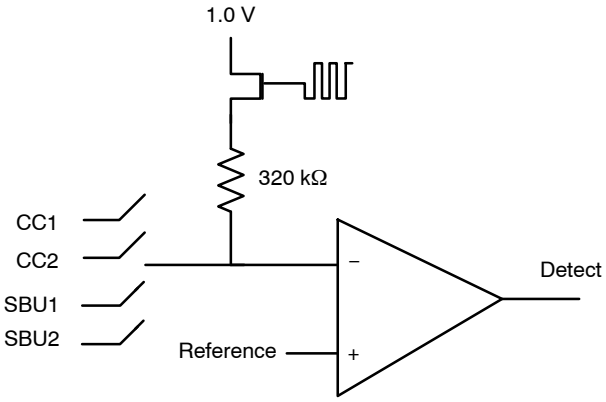


Figure 7. Moisture Detection with ADC

ADC TABLE FOR MOISTURE DETECTION

	Bit	Pull up (kΩ) to 1 V	Moisture resistance (kΩ)	Voltage (V)
0	0	320	17	0.05
1	1	320	36	0.1
2	10	320	56	0.15
3	11	320	80	0.2
4	100	320	107	0.25
5	101	320	137	0.3
6	110	320	172	0.35
7	111	320	213	0.4
8	1000	320	262	0.45
9	1001	320	320	0.5
10	1010	320	391	0.55
11	1011	320	480	0.6
12	1100	320	594	0.65
13	1101	320	747	0.7
14	1110	320	960	0.75
15	1111	320	1,280	0.8

REGISTER MAPPING TABLE

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x01	Product ID	Device ID				Product ID		Revision ID	
0x02	Control	Debug_Acc	NU	EN_DRY	Auto_EN_SBU	EN_SBUFT	EN_SBU	EN_CC	MAN_SW
0x03	Interrupt	NU		CC2_Timer	CC1_Timer	DRY_CHG	MOS_CHG	OVP_REC	OVP
0x04	Interrupt_Mask	NU		Mask_CC2_Timer	Mask_CC1_Timer	Mask_DRY_CHG	Mask_MOS_CHG	Mask_OVP_Rec	Mask_OVP
0x05	Status	LOOK4CC	LOOK4SBU	LOOK4DRY	NU			OVP_SBU	OVP_CC
0x06	Moisture Status	Fault		SBU2_FT	SBU1_FT	SBU2_MOS	SBU1_MOS	CC2_MOS	CC1_MOS
0x07	Switch control	NU					SBU		CC
0x08	Threshold1	SBU_MOS_DET				CC_MOS_DET			
0x09	Threshold2	NU	SBU_Float_DET		VDRY				
0x0A	Timer	NU					TDRY(DRY timer)		
0x0B	RESET	NU						MOS Reset	Device reset
0x0C	Timer2	NU				Number of ADC Read		CC settle time	

DEVICE ID
Address: 01h
Reset Value: 0x100X_XXXX
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	Device ID	R	4	1000 : OPT_A
3:2	Product ID	R	2	00 : FUSB251UCX(Default)
1:0	Revision ID	R	2	00 : RevA 01 : RevB 10 : RevC 11 : RevD

CONTROL
Address: 02h
Reset Value: 0x0000_0000
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7	Debug_Acc	R/W	1	1 : Support Debug_Accessory detection
6	NU	R	1	1 : Do not use
5	EN_DRY	R/W	1	1 : Enable Dry check
4	AUTO_EN_SBU	R/W	1	1 : Enable Auto_EN_SBU
3	EN_SBUFT	R/W	1	1 : Enable float voltage detection on SBU
2	EN_SBU_MOS	R/W	1	1 : Enable moisture detection on SBU with voltage source
1	EN_CC_MOS	R/W	1	1 : Enable moisture detection on CC with voltage source
0	MAN_SW	R/W	1	1 : Enable manual mode switch control

INTERRUPT
Address: 03h
Reset Value: 0x0000_0000
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	NU	R	2	Do not use
5	CC2_TIMER	R	1	1 : CC2 Timer interrupt
4	CC1_TIMER	R	1	1 : CC1 Timer interrupt
3	DRY_CHG	R	1	1 : Dry status change interrupt
2	MOS_CHG	R	1	1 : Moisture status change interrupt
1	OVP_REC	R	1	1 : OVP Recovery interrupt
0	OVP	R	1	1 : OVP interrupt

INTERRUPT_MASK
Address: 04h
Reset Value: 0x0000_0000
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	NU	R/W	2	Do not use
5	Mask_CC2_Timer	R/W	1	1 : Mask CC2 Timer interrupt
4	Mask_CC1_Timer	R/W	1	1 : Mask CC1 Timer interrupt

INTERRUPT_MASK
Address: 04h
Reset Value: 0x0000_0000
Type: Read / Write

3	Mask_Dry_Detect	R/W	1	1 : Mask DRY status change interrupt
2	Mask_MOS_Detect	R/W	1	1 : Mask Moisture status change interrupt
1	Mask_OVP_REC	R/W	1	1 : Mask OVP recovery interrupt
0	Mask_OVP	R/W	1	1 : Mask OVP Interrupt

STATUS
Address: 05h
Reset Value: 0x0000_0000
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7	LOOK4CC	R	1	1 : Device is monitoring moisture on CC1 or CC2
6	LOOK4SBU	R	1	1 : Device is monitoring moisture on SBU1 or SBU2 using float voltage detection
5	LOOK4DRY	R	1	1 : Monitoring Dry check on SBU1 and SBU2
3:2	NU	R	1	Do not use
1	OVP_SBU	R	1	1 : OVP conditions on SBU1 or SBU2
0	OVP_CC	R	1	1 : OVP conditions on CC1 or CC2

MOISTURE_STATUS
Address: 06h
Reset Value: 0x0000_0000
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	FAULT	R	2	These bits are set when moisture detection on SBU using voltage source didn't detect moisture. "01" and "10" will be set with other register bit such as bit0/1 or bit4/5 00 : No moisture detection tried on SBU 01 : Moisture was detected on CC but not found on SBU 10 : Moisture was detected by SBU Float voltage detection(SBUFT) but not found on SBU 11 : No moisture detected on both CC and SBU
5	SBUF2_FT	R	1	1 : Float voltage detected on SBU2
4	SBU1_FT	R	1	1 : Float voltage detected on SBU1
3	SBU2_MOS	R	1	1 : Moisture detected on SBU2
2	SBU1_MOS	R	1	1 : Moisture detected on SBU1
1	CC2_MOS	R	1	1 : Moisture detected on CC2
0	CC1_MOS	R	1	1 : Moisture detected on CC1

SWITCH CONTROL
Address: 07h
Reset Value: 0x0000_0000
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:3	NU	R/W	5	Do not use

SWITCH CONTROL
Address: 07h
Reset Value: 0x0000_0000
Type: Read / Write

2:1	SBU	R/W	2	00 : Open both SBU1 and SBU2 switches 01 : SBU1 and SBU2 close to SBU1_H and SBU2_H 10 : SBU2 closes to FM, SBU1, SBU1_H and SBU2_H are open 11 : SBU1 closes to FM, SBU2, SBU1_H and SBU2_H are open
0	CC	R/W	1	0 : CC1 and CC2 switch are open 1 : CC1 and CC2 close to CC1_H and CC2_H

THRESHOLD 1
Address: 08h
Reset Value: 0x1011_1011
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	SBU_MOS_DET	R/W	4	0000 : 17 kΩ 0001 : 36 kΩ … 1011 : 480 kΩ … 1111 : 1280 kΩ
3:0	CC_MOS_DET	R/W	4	0000 : 17 kΩ 0001 : 36 kΩ … 1011 : 480 kΩ … 1111 : 1280 kΩ

THRESHOLD 2
Address: 09h
Reset Value: 0x0001_1101
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7	NU	R	1	Do not use
6:4	SBU_Float_DET	R/W	3	000 : 100 mV 001 : 200 mV 010 : 300 mV 011 : 400 mV 100 : 500 mV 101 : 600 mV 110 : 700 mV 111 : 800 mV
3:0	VDRY	R/W	4	0000 : 17 kΩ 0001 : 36 kΩ … 1101 : 747 kΩ … 1111 : 1280

TIMER
Address: 0Ah
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:3	NU	R	5	Do not use
2:0	TDRY	R/W	3	000 : 50 ms 001 : 100 ms 010 : 250 ms 011 : 1 sec 100 : 2 sec 101 : 4 sec 110 : 8 sec 111 : 10 sec

RESET
Address: 0Bh
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:2	NU	R	6	Do not use
1	MOS Reset	R/W/C	1	1 : Reset moisture detection state machine and clear moisture status, Read returns ‘0’. This register bit resets moisture detection state machine and moisture status register is cleared. Control register is not affected by this bit. If any moisture detection enable bit was set, moisture detection will restart by MOS Reset
0	Reset	R/W/C	1	1 : Reset the device, Read returns ‘0’ The Device Reset includes FM pin configuration so FM pin status is checked after this Reset

TIMER2
Address: 0Ch
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	NU	R	4	Do not use
3:2	Number of ADC Read	R/W	2	00 : 1 time 01 : 2 times 10 : 3 timers 11 : Do not use(no change)
1:0	CC Settle time	R/W	2	**00 : 400 μs** 01 : 300 μs 10 : 500 μs 11 : 600 μs

APPLICATION CIRCUIT

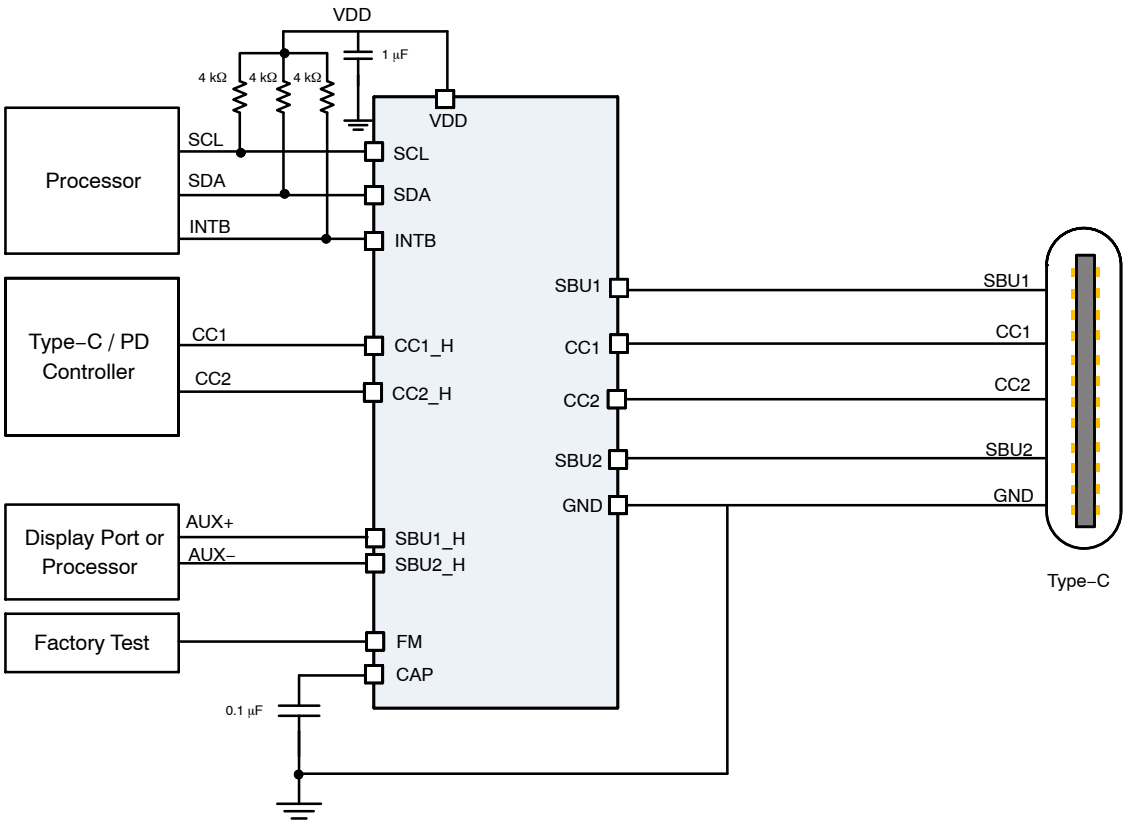
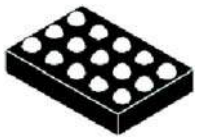


Figure 8. Application Circuit

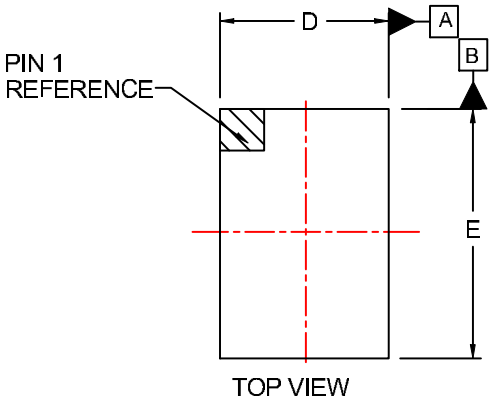
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

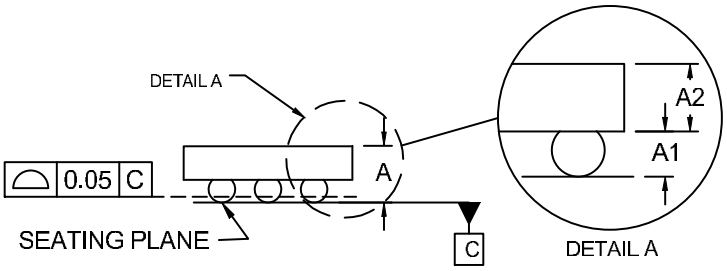


WLCSP15, 1.49x2.06x0.574
CASE 567WV
ISSUE O

DATE 12 JUL 2018



TOP VIEW

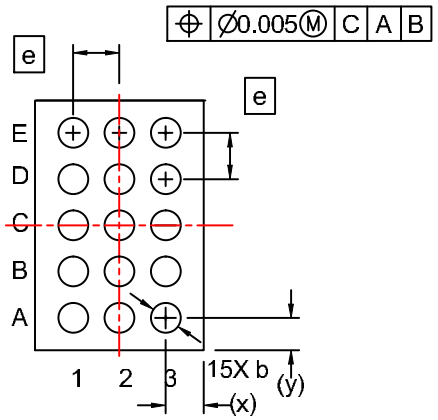


SIDE VIEW

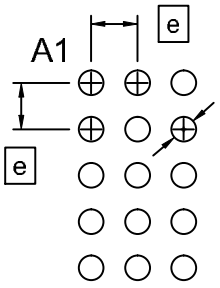
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.536	0.574	0.612
A1	0.178	0.196	0.214
A2	0.358	0.378	0.398
b	0.240	0.260	0.280
D	1.460	1.490	1.520
E	2.030	2.060	2.090
e	0.40 BSC		
x	0.330	0.345	0.360
y	0.215	0.230	0.245



BOTTOM VIEW



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