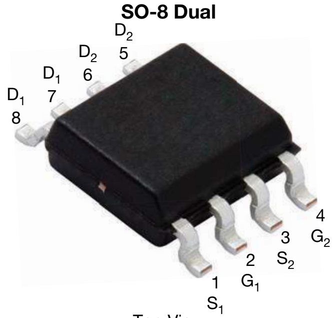
N- and P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A) [a]	Q_g (TYP.)
N-Channel	100	0.057 at V_{GS} = 10 V	5.6	4
		0.072 at V_{GS} = 4.5 V	5	
P-Channel	-100	0.183 at V_{GS} = -10 V	-3.4	11.6
		0.205 at V_{GS} = -4.5 V	-3.2	

SO-8 Dual



Top View

Ordering Information:
Si4590DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

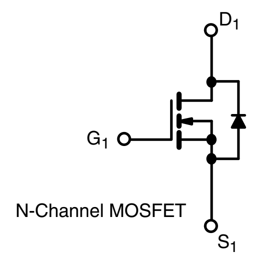
FEATURES

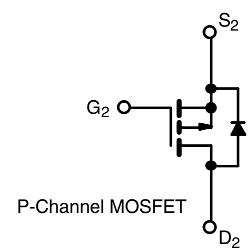
- TrenchFET® Power MOSFET
- 100 % R_g and UIS tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- H bridge / DC-AC inverter
  - Brushless DC motors





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-Source Voltage		V_{DS}	100	-100	V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current (T_J = 150 °C)	T_F = 25 °C	I_D	5.6	-3.4	A
	T_F = 70 °C		4.5	-2.7	
	T_A = 25 °C		4.5 [b,c]	-2.5 [b,c]	
	T_A = 70 °C		3.6 [b,c]	-2 [b,c]	
Pulsed Drain Current (100 µs Pulse Width)		I_{DM}	30	-20	
Source-Drain Current Diode Current	T_F = 25 °C	I_S	3	-3.5	
	T_A = 25 °C		2 [b,c]	-1.9 [b,c]	
Pulsed Source-Drain Current (100 µs Pulse Width)		I_{SM}	30	-20	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	5	-20	
Single Pulse Avalanche Energy		E_{AS}	1.3	20	mJ
Maximum Power Dissipation	T_F = 25 °C	P_D	3.6	4.2	W
	T_F = 70 °C		2.3	2.7	
	T_A = 25 °C		2.3 [b,c]	2.3 [b,c]	
	T_A = 70 °C		1.5 [b,c]	1.5 [b,c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum Junction-to-Ambient [b,d]	t ≤ 10 s	R_{thJA}	35	55	33	55	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	20	35	17	30	

Notes
a. Based on T_F = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 90 °C/W (n-channel) and 90 °C/W (p-channel).

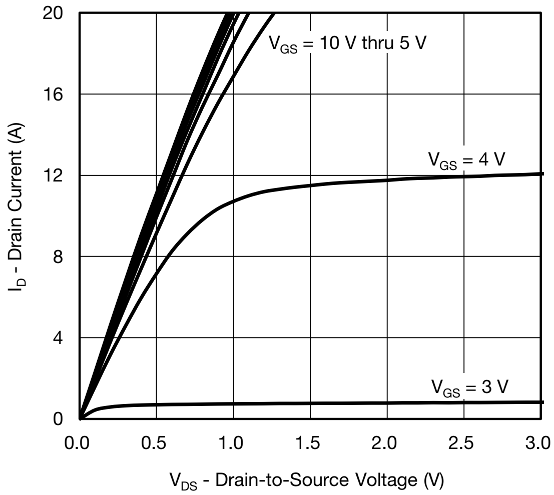
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	100	-	-	V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-100	-	-	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch	-	70	-	mV/°C
		I_D = -250 µA	P-Ch	-	-103	-	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch	-	-5.7	-	
		I_D = -250 µA	P-Ch	-	4.5	-	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	1.5	-	2.5	V
		$V_{DS} = V_{GS}$, I_D = -250 µA	P-Ch	-1.5	-	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch	-	-	100	nA
			P-Ch	-	-	-100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	N-Ch	-	-	1	µA
		V_{DS} = -100 V, V_{GS} = 0 V	P-Ch	-	-	-1	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch	-	-	10	
		V_{DS} = -100 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch	-	-	-10	
On-State Drain Current [b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N-Ch	10	-	-	A
		V_{DS} = -5 V, V_{GS} = -10 V	P-Ch	-10	-	-	
Drain-Source On-State Resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2 A	N-Ch	-	0.047	0.057	Ω
		V_{GS} = -10 V, I_D = -2 A	P-Ch	-	0.150	0.183	
		V_{GS} = 4.5 V, I_D = 1.5 A	N-Ch	-	0.059	0.072	
		V_{GS} = -4.5 V, I_D = -1 A	P-Ch	-	0.165	0.205	
Forward Transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 2 A	N-Ch	-	9	-	S
		V_{DS} = -15 V, I_D = -2 A	P-Ch	-	9.3	-	
Dynamic [a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = -50 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	-	360	-	pF
			P-Ch	-	1150	-	
Output Capacitance	C_{oss}		N-Ch	-	130	-	
			P-Ch	-	65	-	
Reverse Transfer Capacitance	C_{rss}		N-Ch	-	20	-	
			P-Ch	-	40	-	
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 4.5 A	N-Ch	-	7.5	11.5	nC
		V_{DS} = -50 V, V_{GS} = -10 V, I_D = -5 A	P-Ch	-	24	36	
		N-Channel V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 4.5 A P-Channel V_{DS} = -50 V, V_{GS} = -4.5 V, I_D = -5 A	N-Ch	-	4	6	
			P-Ch	-	11.6	18	
Gate-Source Charge	Q_{gs}		N-Ch	-	1.2	-	
			P-Ch	-	3.8	-	
Gate-Drain Charge	Q_{gd}		N-Ch	-	2	-	
			P-Ch	-	5	-	
Gate Resistance	R_g	f = 1 MHz	N-Ch	0.6	3.3	6.6	Ω
			P-Ch	3	13	26	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Dynamic [a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 50 V, R_L = 13.8 Ω $I_D \cong$ 3.6 A, V_{GEN} = 10 V, R_g = 1 Ω P-Channel V_{DD} = -50 V, R_L = 12.5 Ω $I_D \cong$ -4 A, V_{GEN} = -10 V, R_g = 1 Ω	N-Ch	-	5	10	ns
			P-Ch	-	7	15	
Rise Time	t_r		N-Ch	-	11	20	
			P-Ch	-	11	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	-	12	25	
			P-Ch	-	65	130	
Fall Time	t_f		N-Ch	-	6	15	
			P-Ch	-	20	40	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 50 V, R_L = 13.8 Ω $I_D \cong$ 3.6 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = -50 V, R_L = 12.5 Ω $I_D \cong$ -4 A, V_{GEN} = -4.5 V, R_g = 1 Ω	N-Ch	-	32	65	
			P-Ch	-	55	110	
Rise Time	t_r		N-Ch	-	73	150	
			P-Ch	-	80	160	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	-	14	30	
			P-Ch	-	42	85	
Fall Time	t_f		N-Ch	-	12	25	
			P-Ch	-	25	50	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_F = 25 °C	N-Ch	-	-	3	A
			P-Ch	-	-	-3.5	
Pulse Diode Forward Current [a]	I_{SM}		N-Ch	-	-	30	
			P-Ch	-	-	-20	
Body Diode Voltage	V_{SD}	I_S = 3.6 A	N-Ch	-	0.83	1.2	V
		I_S = -4 A	P-Ch	-	-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 3.6 A, dI/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = -4 A, dI/dt = -100 A/µs, T_J = 25 °C	N-Ch	-	30	60	ns
			P-Ch	-	42	85	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch	-	27	55	nC
			P-Ch	-	93	190	
Reverse Recovery Fall Time	t_a		N-Ch	-	19	-	ns
			P-Ch	-	36	-	
Reverse Recovery Rise Time	t_b		N-Ch	-	11	-	
			P-Ch	-	6	-	

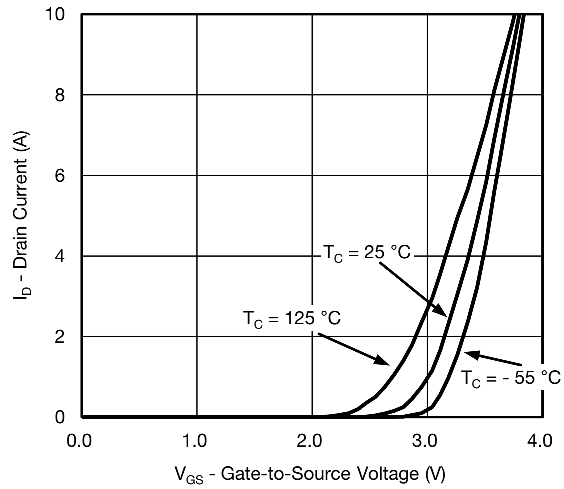
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

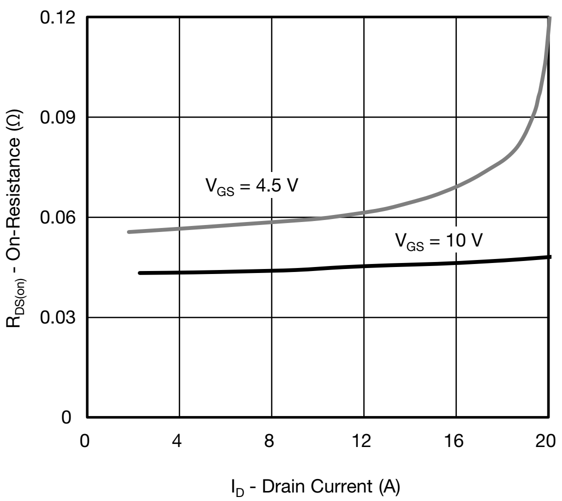
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



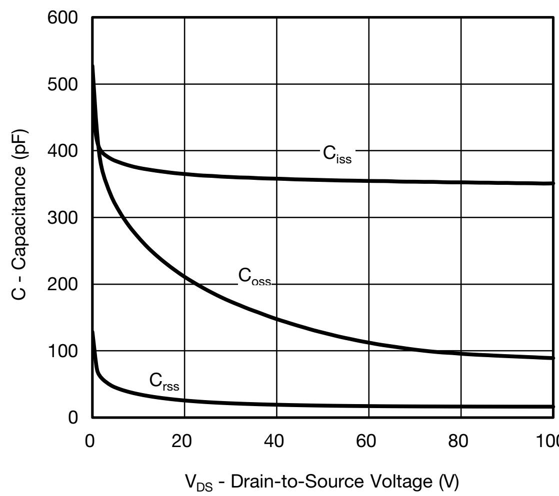
Output Characteristics



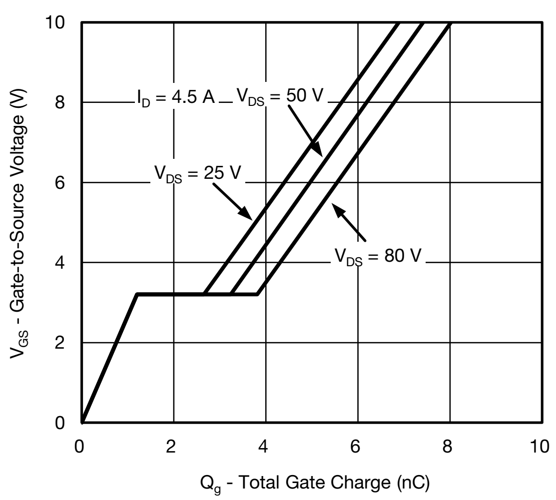
Transfer Characteristics



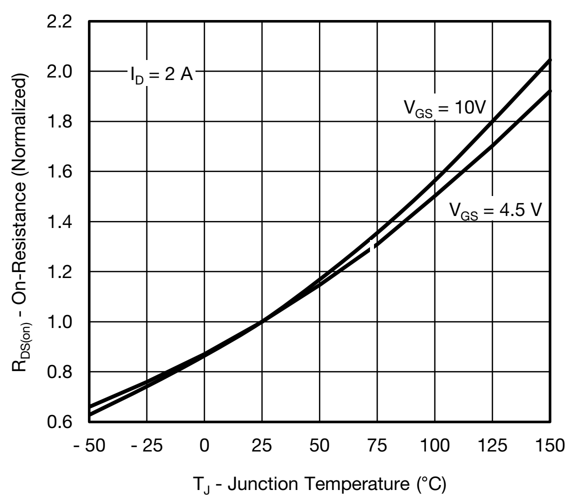
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

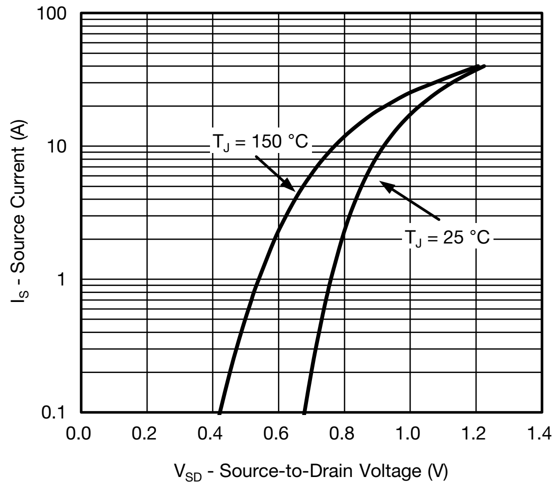


Gate Charge

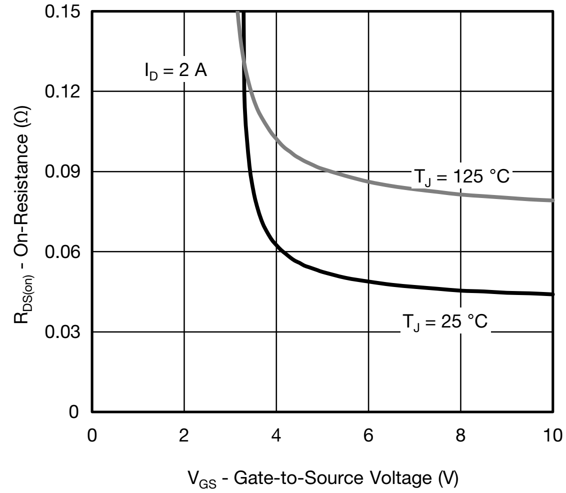


On-Resistance vs. Junction Temperature

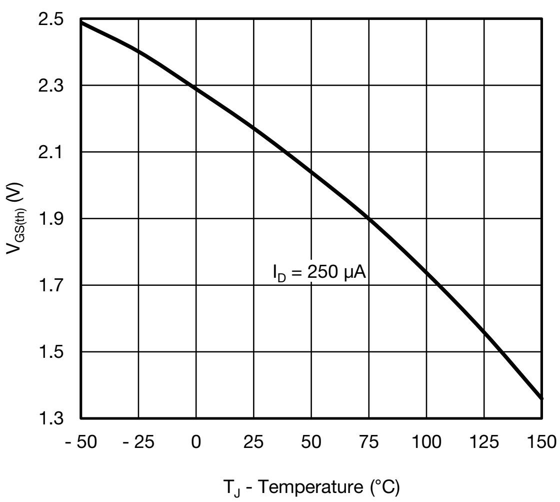
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



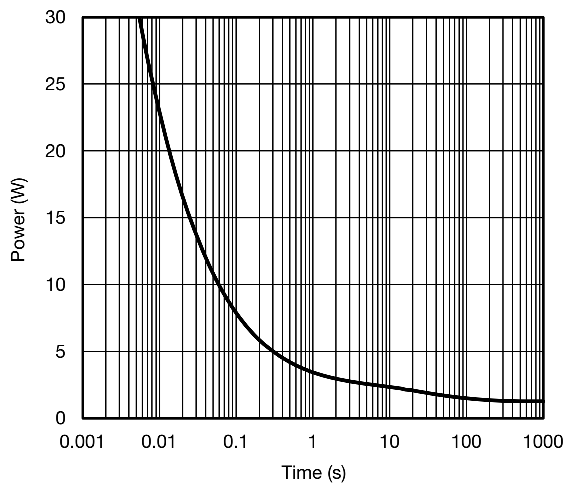
Source-Drain Diode Forward Voltage



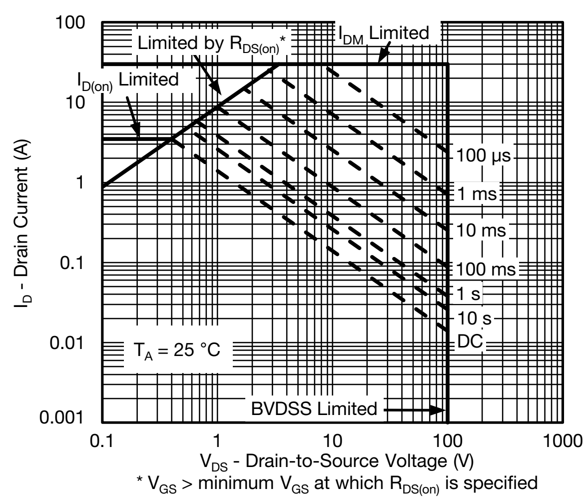
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

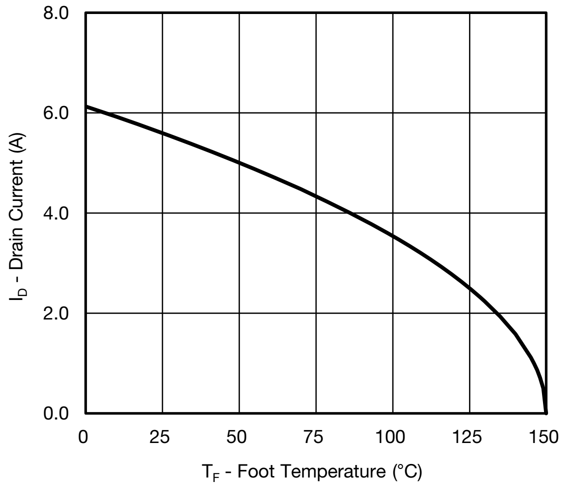


Single Pulse Power, Junction-to-Ambient

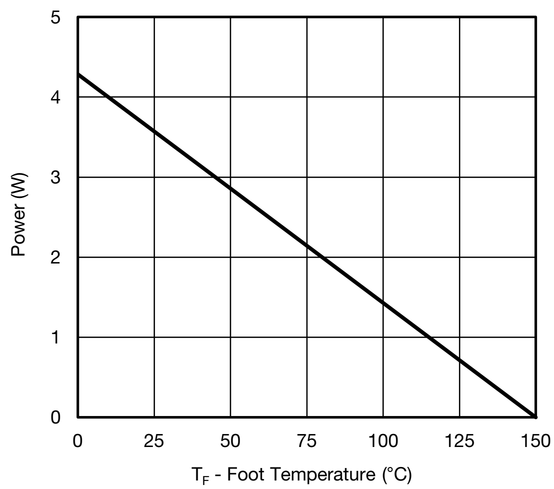


Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



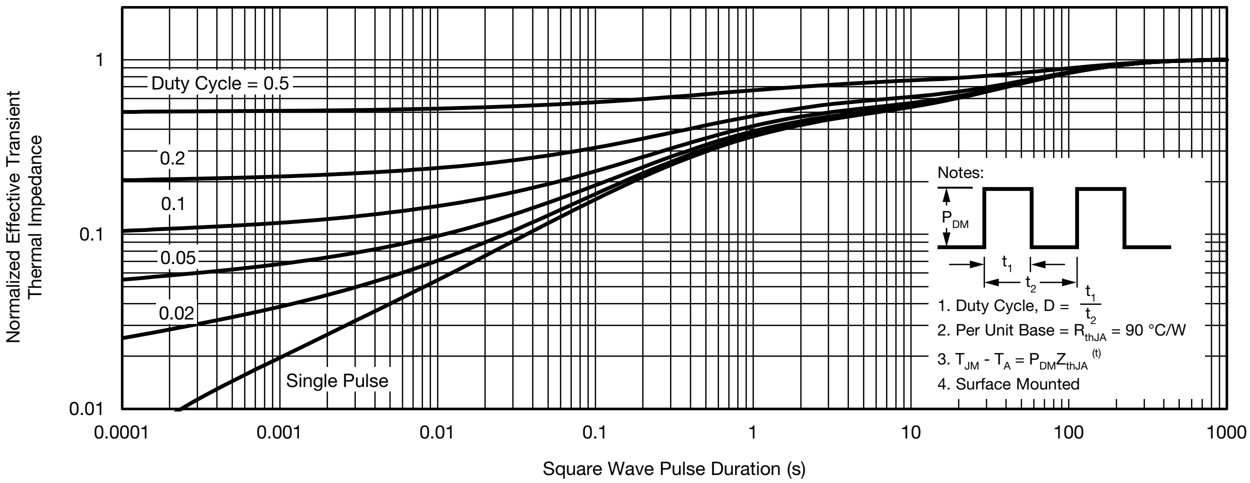
Current Derating*



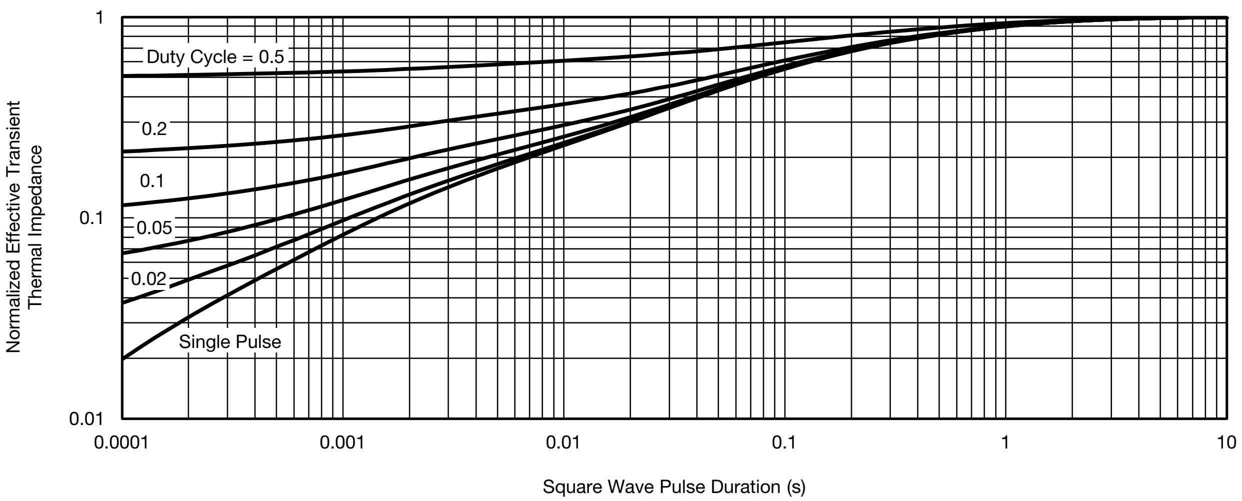
Power Derating, Junction-to-Foot

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

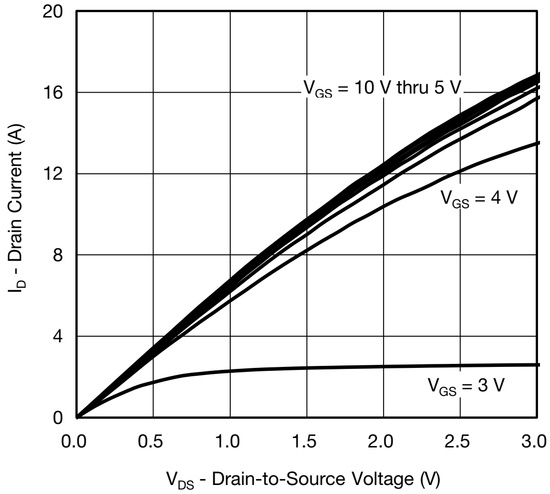


Normalized Thermal Transient Impedance, Junction-to-Ambient

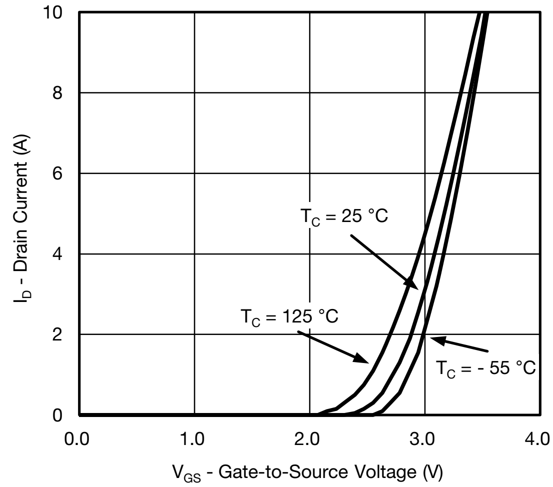


Normalized Thermal Transient Impedance, Junction-to-Foot

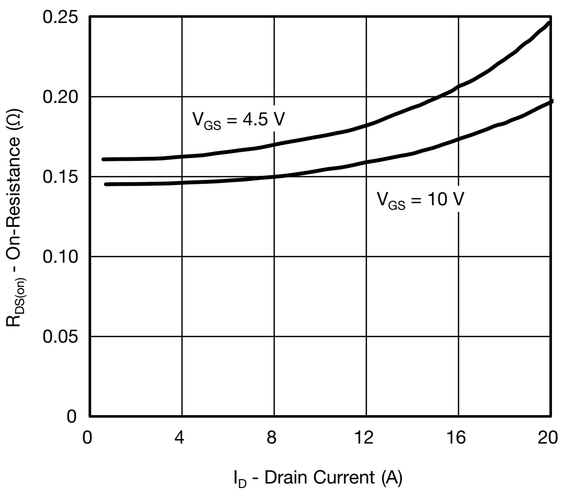
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



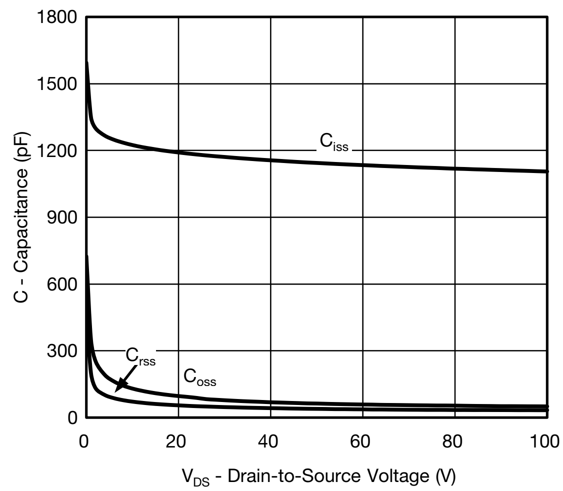
Output Characteristics



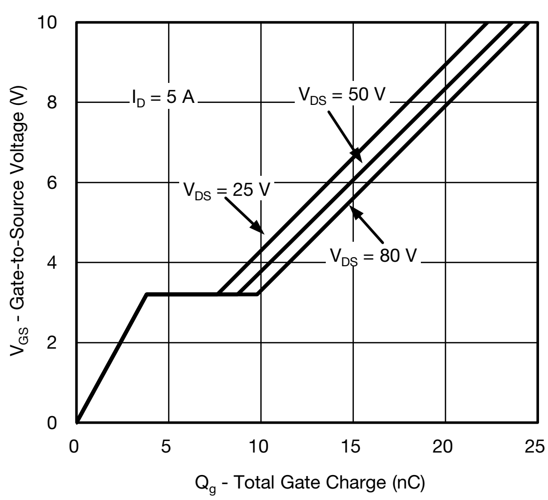
Transfer Characteristics



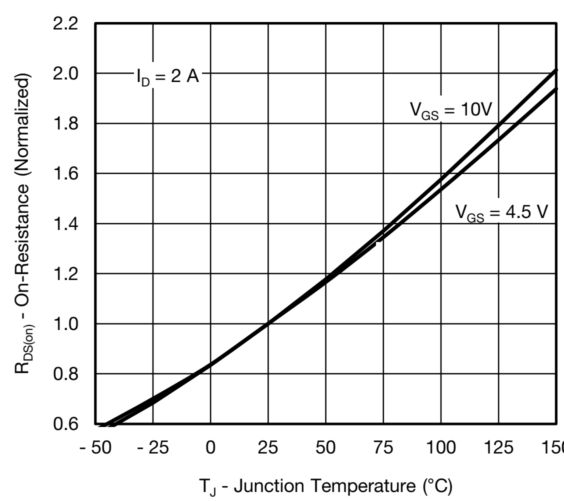
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

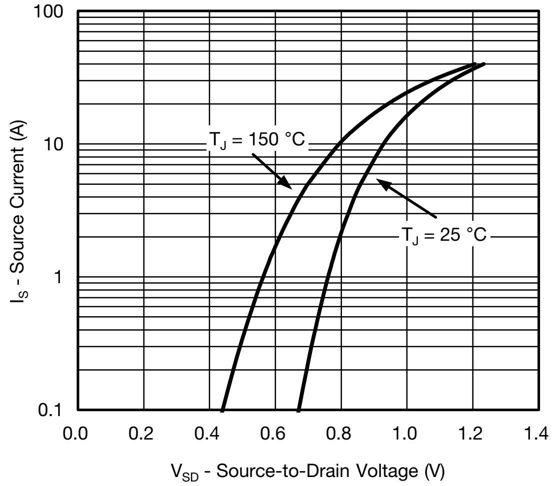


Gate Charge

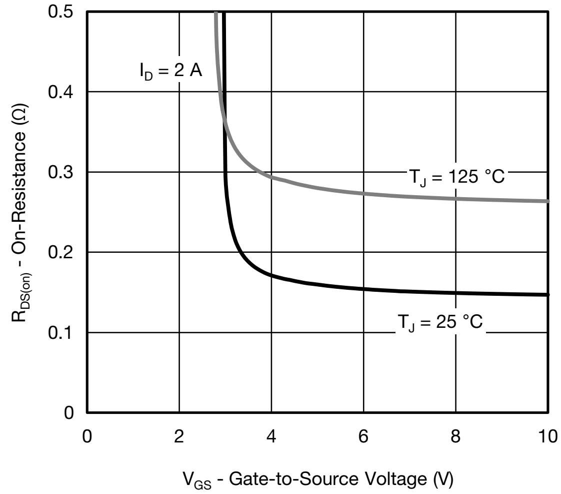


On-Resistance vs. Junction Temperature

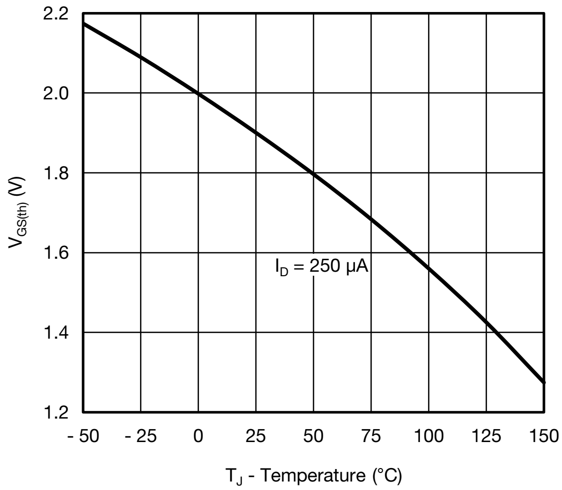
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, (unless otherwise noted)



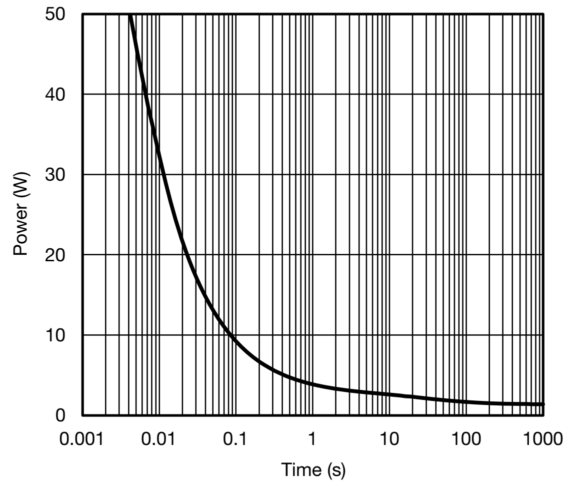
Source-Drain Diode Forward Voltage



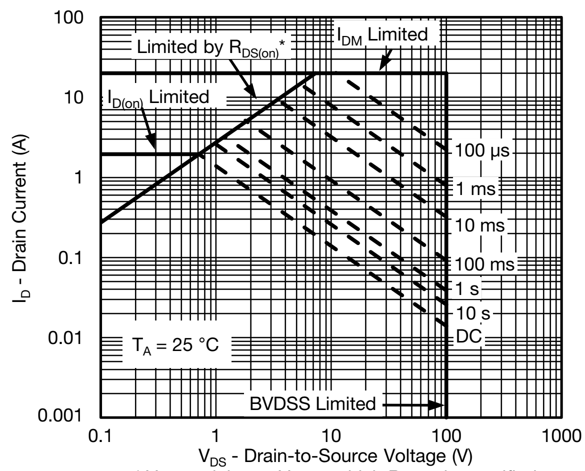
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



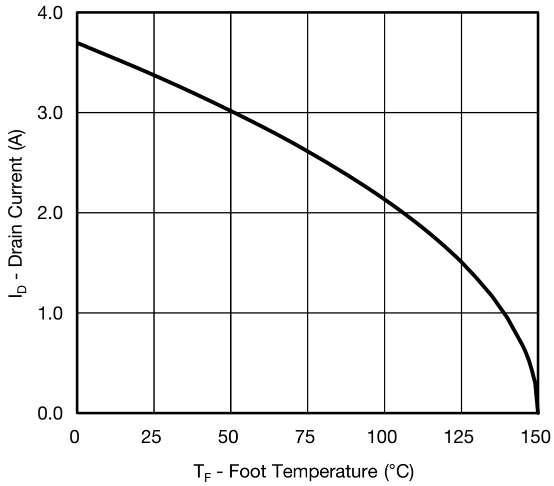
Single Pulse Power, Junction-to-Ambient



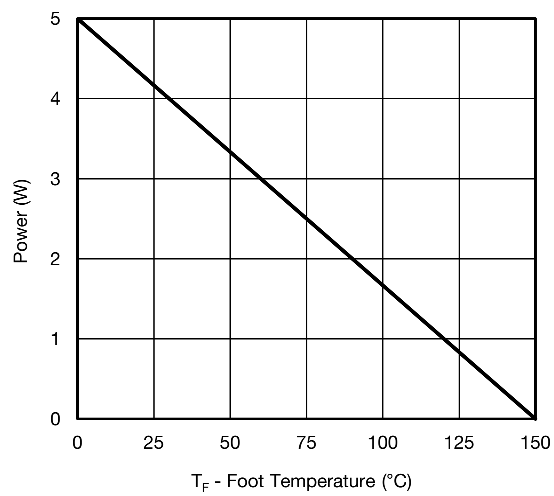
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



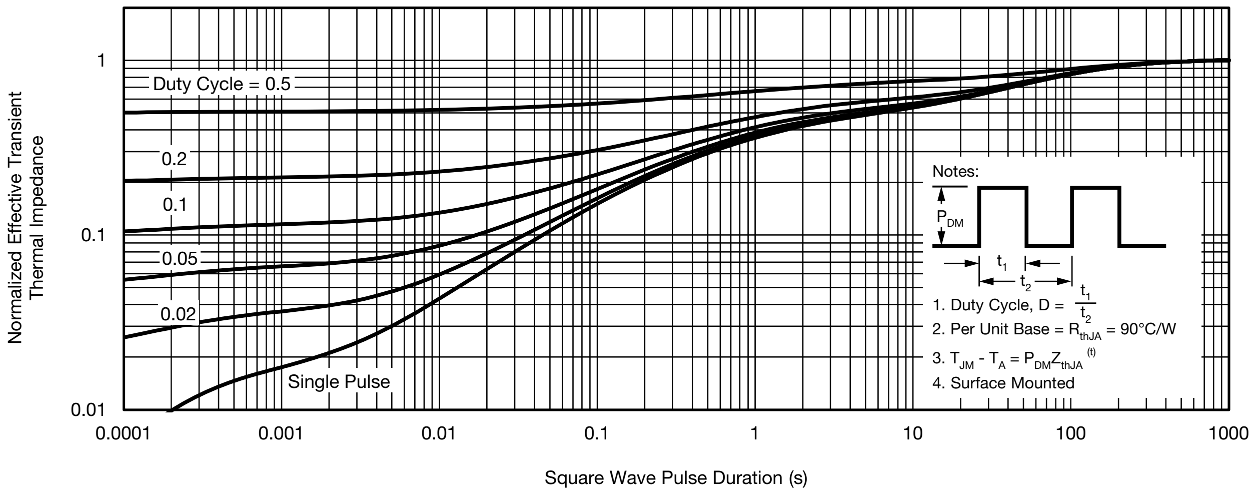
Current Derating*



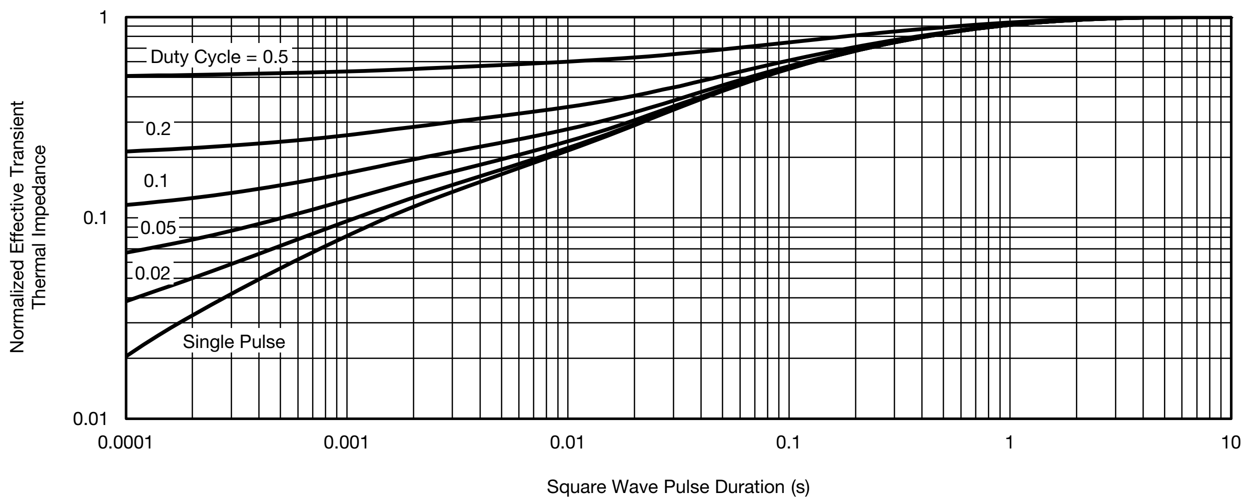
Power Derating, Junction-to-Foot

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



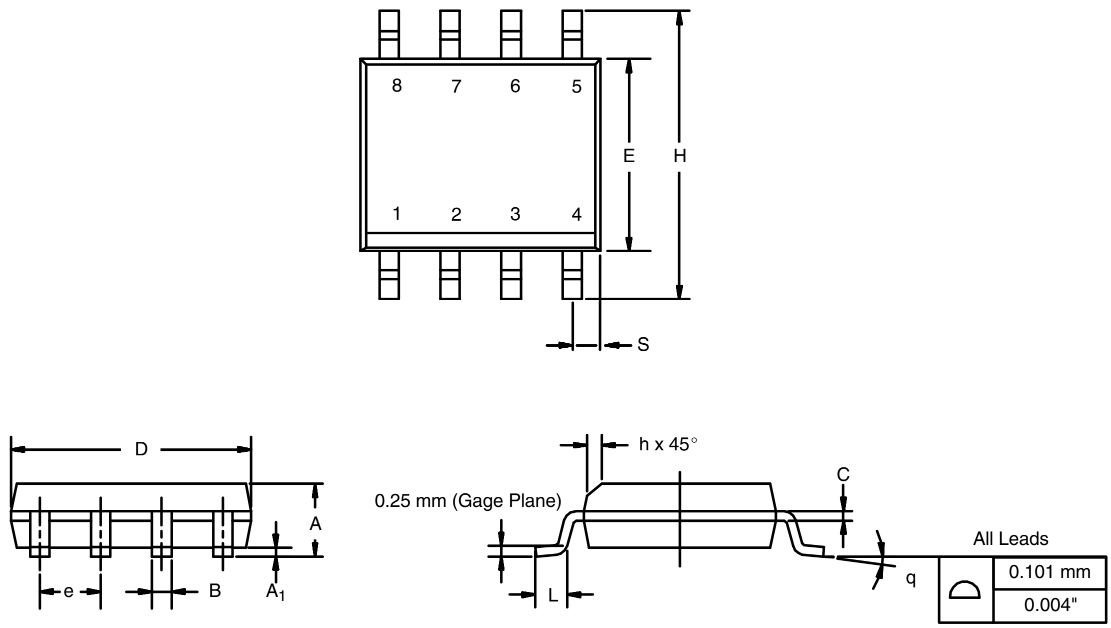
Normalized Thermal Transient Impedance, Junction-to-Ambien



Normalized Thermal Transient Impedance, Junction-to-Foot

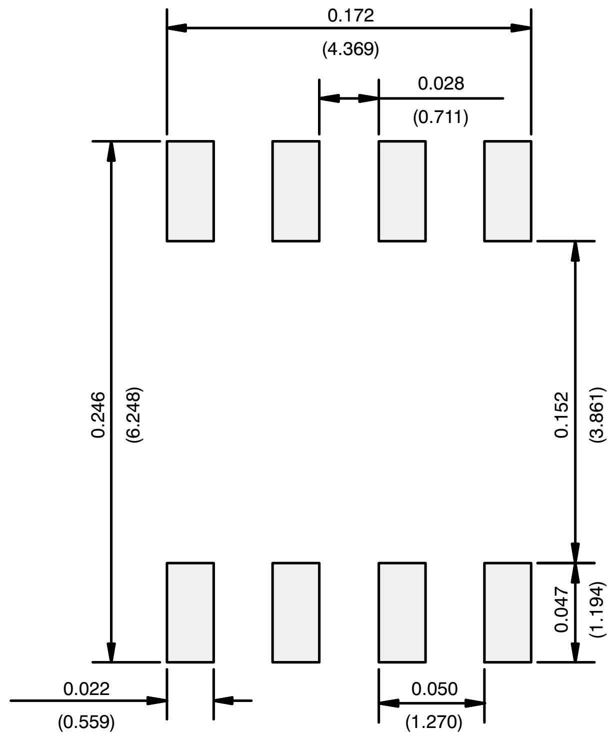
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62937.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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