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General Description

The 843002I is a 2 output LVPECL synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of thefamily of high performance clock solutions from IDT. Using a 26.5625MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz, and 53.125MHz. The 843002I uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 843002I is packaged in a small 20-pin TSSOP package.

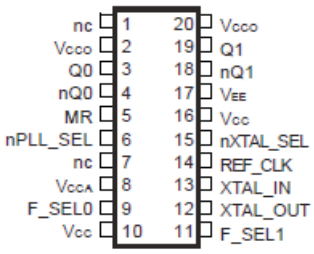
Features

- Two 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @212.5MHz (2.55MHz - 20MHz): 0.50ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package
- For functional replacement part use 8T49N242

Frequency Select Function Table

Inputs						Output Frequency (MHz)
Input Frequency	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
23.4375	0	0	24	3	8	187.5

Pin Assignment



843002I
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm
package body
G Package
Top View

Block Diagram

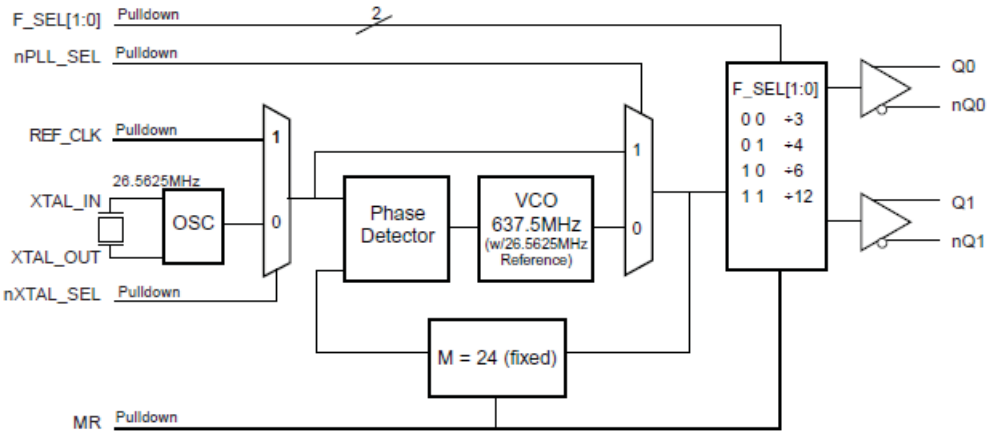


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V_{CCO}	Power		Output supply pins.
3, 4	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.
8	V_{CCA}	Power		Analog supply pin.
9, 11	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10, 16	V_{CC}	Power		Core supply pin.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	LVCMOS/LVTTL reference clock input.
15	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
17	V_{EE}	Power		Negative supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.

NOTE: refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{CCO}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				13	mA

Table 3B. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				115	mA
I_{CCA}	Analog Supply Current				12	mA

Table 3C. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% or 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	V_CC = V_{IN} = 3.63V or 2.625V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.67	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] =11	46.67		56.67	MHz
tsk(o)	Output Skew; NOTE 1, 2				30	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (2.55MHz - 20MHz)		0.50		ps
		159.375MHz, (1.875MHz - 20MHz)		0.54		ps
		106.25MHz, (637kHz - 5MHz)		0.68		ps
		53.125MHz, (637kHz - 5MHz)		0.70		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		650	ps
odc	Output Duty Cycle	F_SEL[1:0] ≠ 00	49		51	%
		F_SEL[1:0] = 00	43		57	%

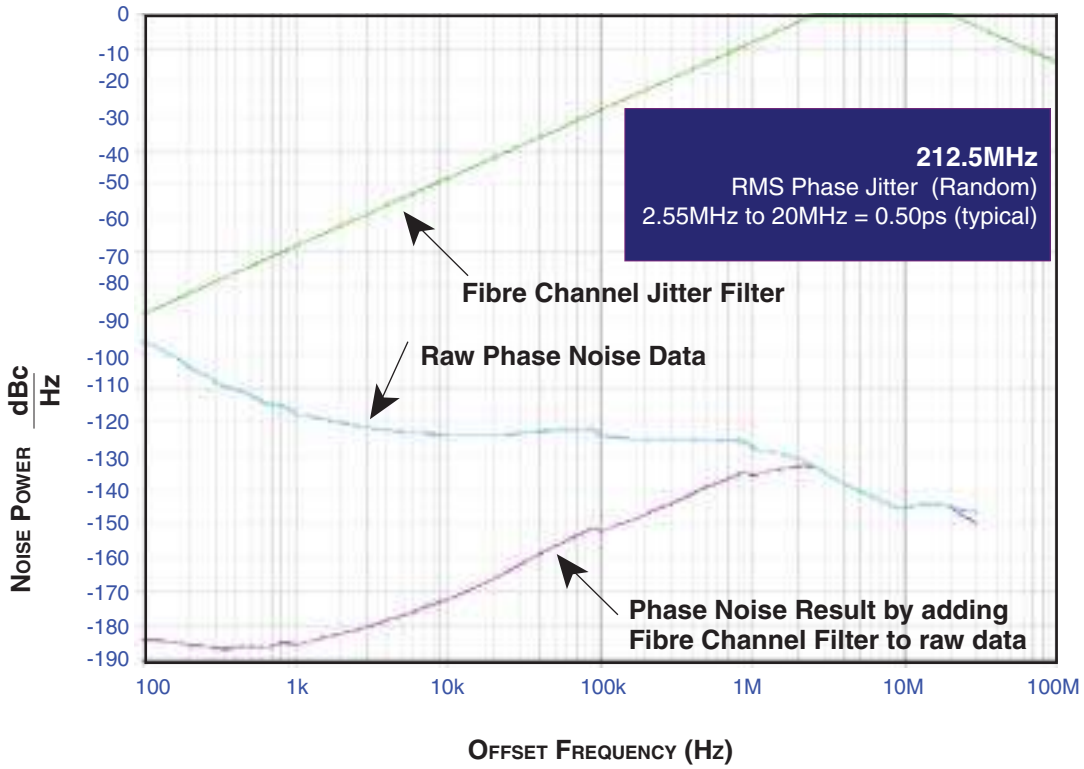
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Measured using crystal input.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, T_A = -40°C TO 85°C

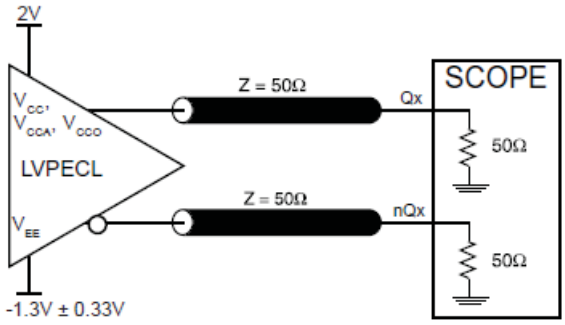
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.67	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] =11	46.67		56.67	MHz
tsk(o)	Output Skew; NOTE 1, 2				30	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (2.55MHz - 20MHz)		0.50		ps
		159.375MHz, (1.875MHz - 20MHz)		0.55		ps
		106.25MHz, (637kHz - 5MHz)		0.75		ps
		53.125MHz, (637kHz - 5MHz)		0.76		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		650	ps
odc	Output Duty Cycle	F_SEL[1:0] ≠ 00	49		51	%
		F_SEL[1:0] = 00	43		57	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Measured using crystal input.

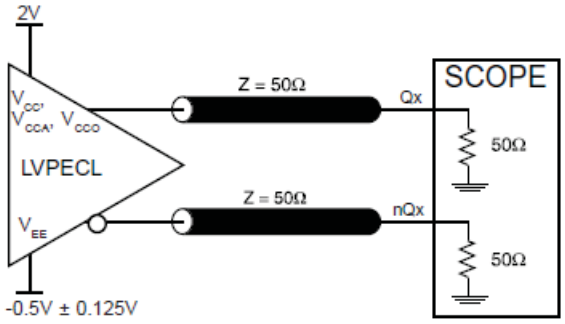
Typical Phase Noise at 212.5MHz @ 3.3V



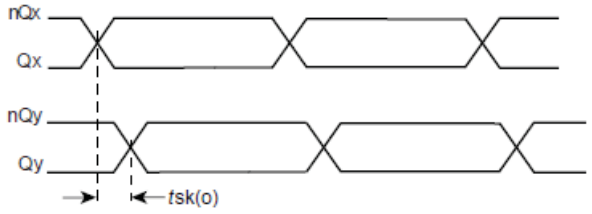
Parameter Measurement Information



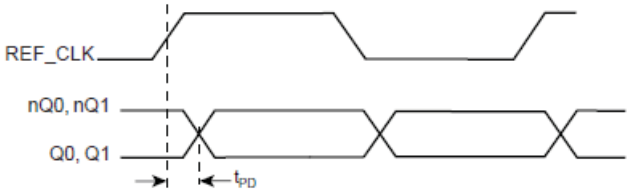
3.3V Core/3.3V Output Load AC Test Circuit



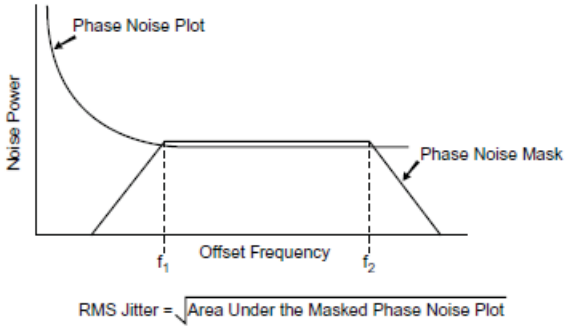
2.5V Core/2.5V Output Load AC Test Circuit



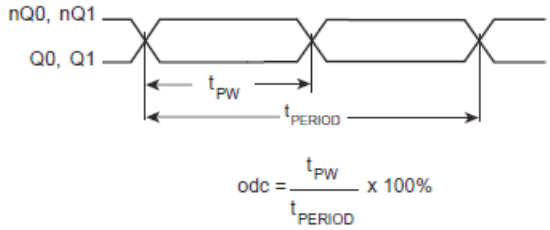
Output Skew



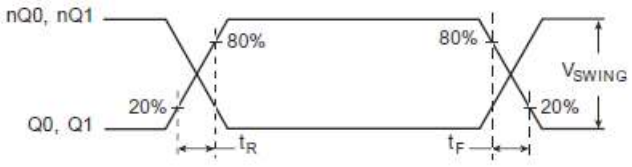
Propagation Delay



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843002I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

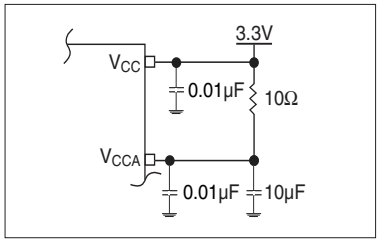


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 843002I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

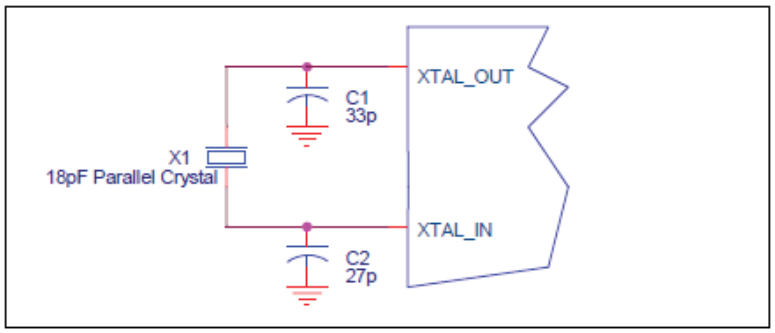


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note the device performance is guaranteed by using a quartz crystal.

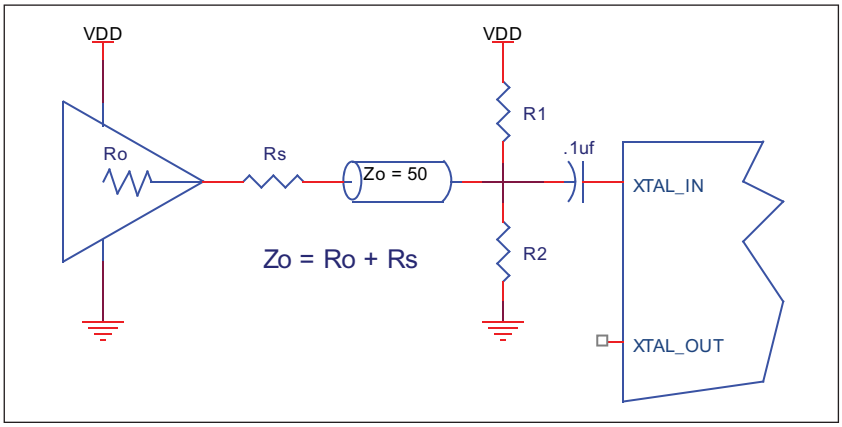


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

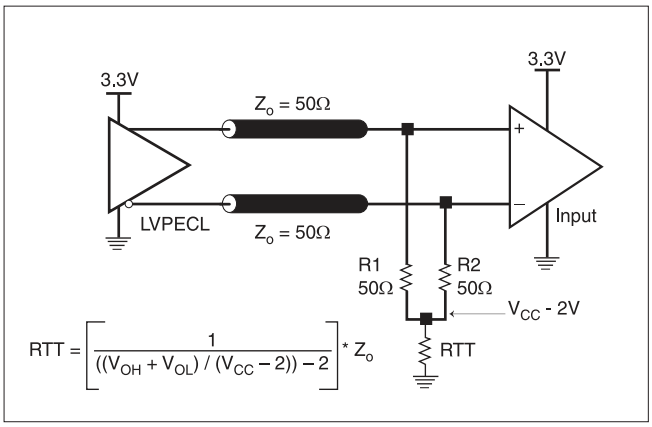


Figure 4A. LVPECL Output Termination

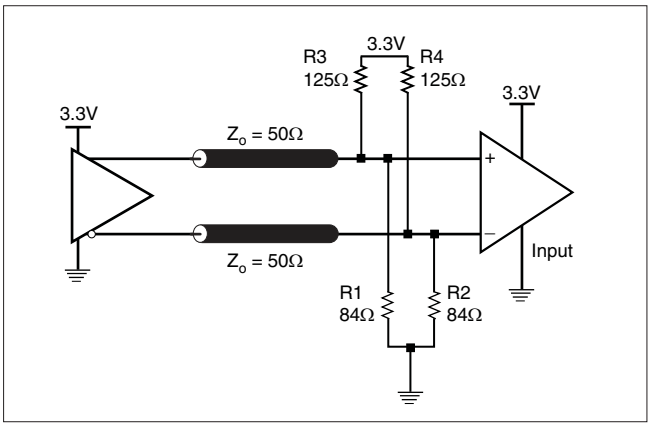


Figure 4B. LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

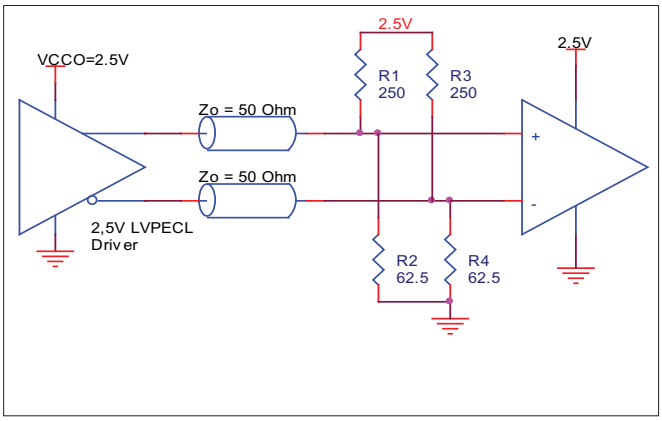


Figure 5A. 2.5V LVPECL Driver Termination Example

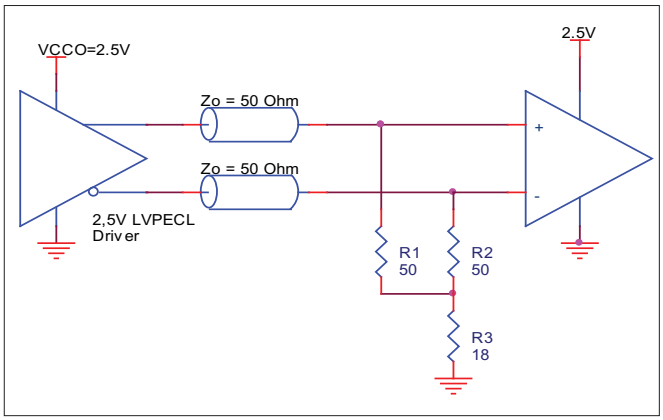


Figure 5B. 2.5V LVPECL Driver Termination Example

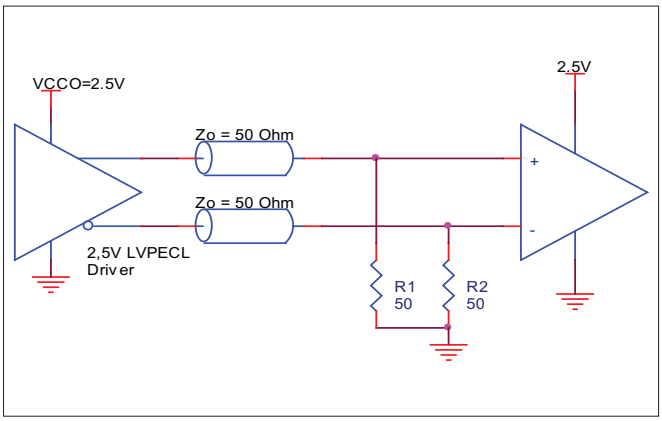


Figure 5C. 2.5V LVPECL Termination Example

Layout Guideline

Figure 6A shows a schematic example of the 843002I. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant 26.5625MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

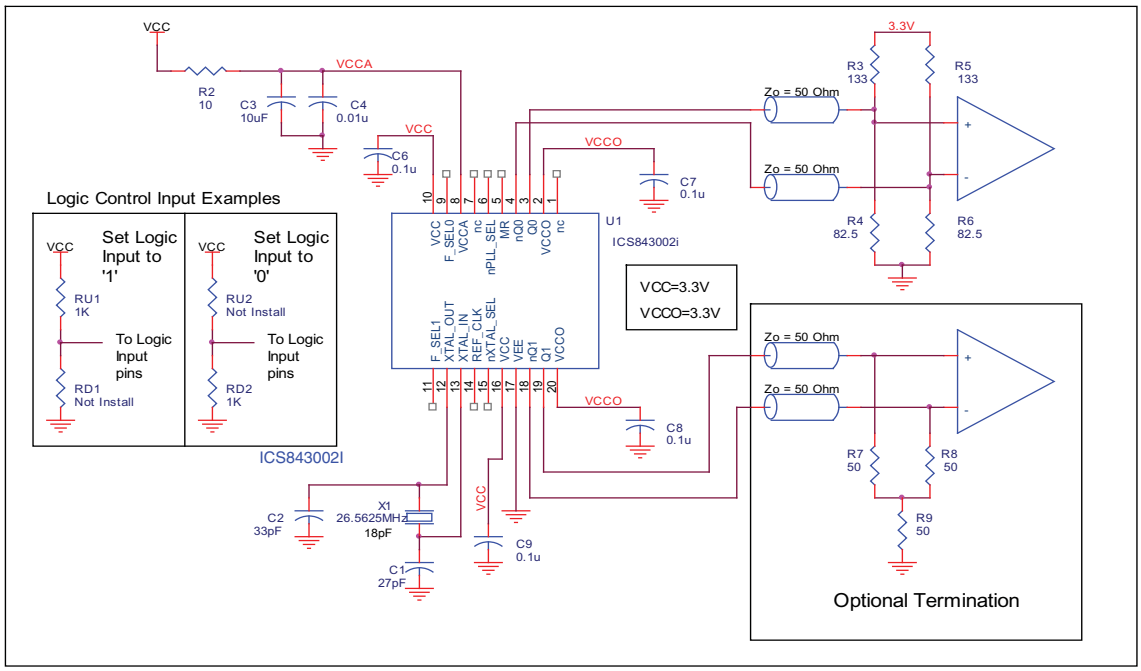


Figure 6A. 843002I Schematic Example

PC Board Layout Example

Figure 6B shows an example of 843002I P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

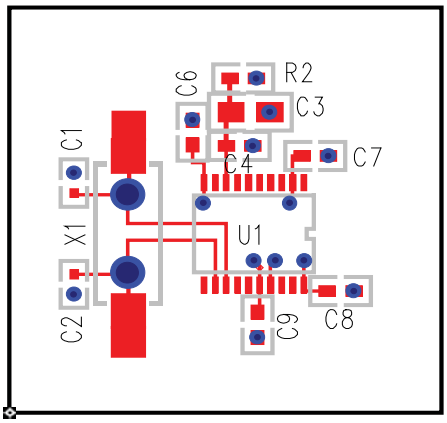


Figure 6B. 843002I PC Board Layout Example

Table 6. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5, C6, C7, C8	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843002I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843002I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 130mA = **471.9mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power $_{MAX}$ (3.63V, with all outputs switching) = 471.9mW + 60mW = **531.9mW**

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.532W * 66.6°C/W = 120.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

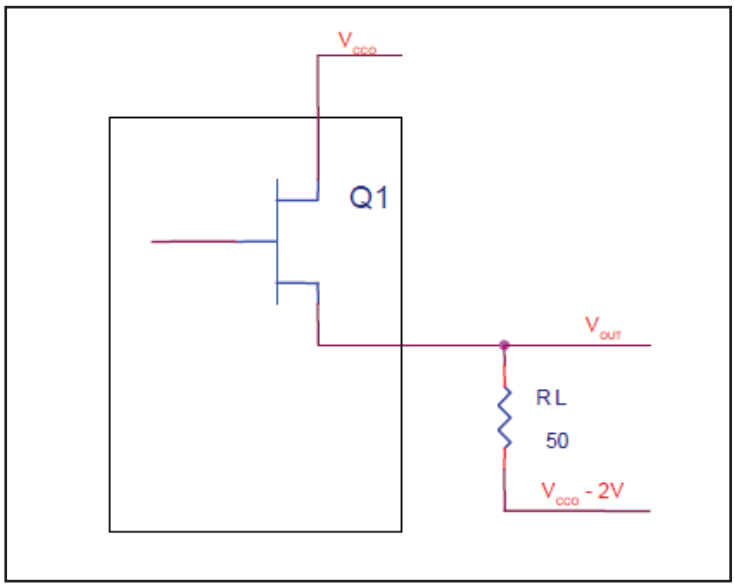


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 843002I is: 2578

Package Outline and Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

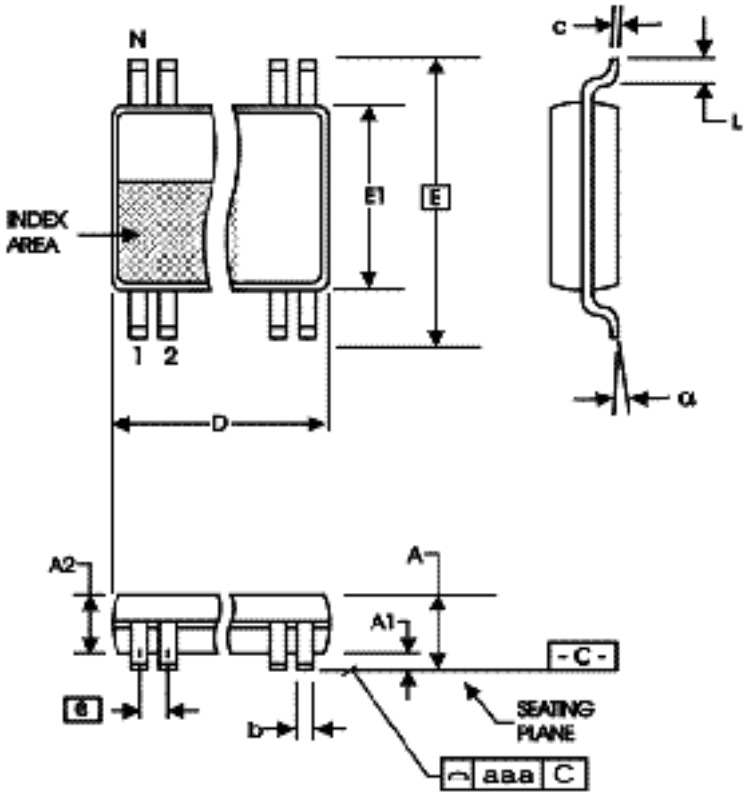


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843002AGILF	ICS843002AIL	20 lead “Lead Free” TSSOP	Tube	-40°C to +85°C
843002AGILFT	ICS843002AIL	20 lead “Lead Free” TSSOP	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T10	9 16	Changed the format of the datasheet to the new IDT header/footer. Added LVCMOS to Crystal Interface section. Ordering Information Table - corrected Lead-Free marking.	6/24/09
A	T10	1 8 13 16	Correctly positioned “pulldown” labels of block diagram. Removed last sentence in paragraph of Power Supply Filtering Techniques. Updated first paragraph under Junction Temperature. Ordering information - removed the F marking for the LF part number.	9/11/09
A	T10	1 1 16	Removed ICS from part numbers were needed. General Description - removed Hiperclocks Chip and Hiperclocks name. Features Section - removed reference to lead free part. Ordering Information - removed quantity in tape and reel and removed LF note below the table. Updated data sheet header and footer.	1/15/16
A			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/26/16

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