

NP160N055TUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0022EJ0100 Rev.1.00 Jul 01, 2010

Description

The NP160N055TUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 3.0 mΩ MAX. (V_{GS} = 10 V, I_D = 80 A)
- Low Ciss: Ciss = 6900 pF TYP. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP160N055TUJ -E1-AY *1	Pure Sn (Tin)	Tape 800 pcs/reel	TO-263-7pin, Taping (E1 type)
NP160N055TUJ -E2-AY *1			TO-263-7pin, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25$ °C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	55	٧
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±160	Α
Drain Current (pulse) *1	I _{D(pulse)}	±640	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	250	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Repetitive Avalanche Current *2	I _{AR}	54	Α
Repetitive Avalanche Energy *2	E _{AR}	291	mJ

Notes: *1. PW \leq 10 μ s, Duty Cycle \leq 1%

Thermal Resistance

^{*2.} $T_{ch(peak)} \le 150$ °C, $R_G = 25 \Omega$

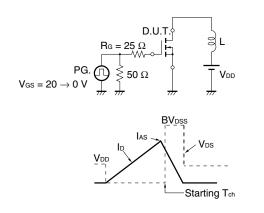
Electrical Characteristics (T_A = 25°C)

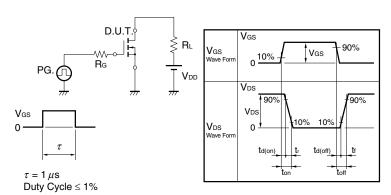
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 55 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	55	110		S	$V_{DS} = 5 \text{ V}, I_{D} = 80 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}		2.4	3.0	mΩ	V _{GS} = 10 V, I _D = 80 A
Input Capacitance	C _{iss}		6900	10350	pF	$V_{DS} = 25 V$,
Output Capacitance	Coss		760	1140	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		290	530	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		40	90	ns	$V_{DD} = 28 \text{ V}, I_D = 80 \text{ A},$
Rise Time	t _r		20	50	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		90	180	ns	$R_G = 0 \Omega$
Fall Time	t _f		10	30	ns	
Total Gate Charge	Q_G		115	180	nC	V _{DD} = 44 V,
Gate to Source Charge	Q_{GS}		28		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		36		nC	I _D = 160 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I _F = 160 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		57		ns	I _F = 160 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		115		nC	di/dt = 100 A/μs

Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



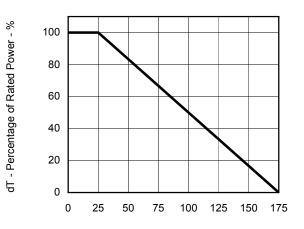


TEST CIRCUIT 3 GATE CHARGE

$$PG. \bigcirc \stackrel{\text{D.U.T.}}{\leqslant} S50 \ \Omega$$

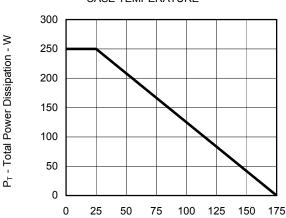
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



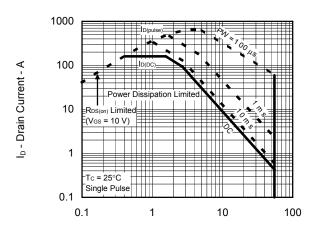
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



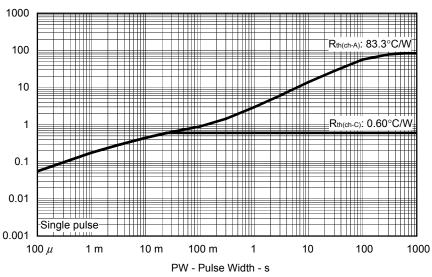
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



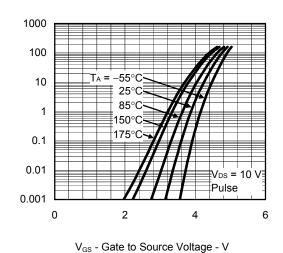
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





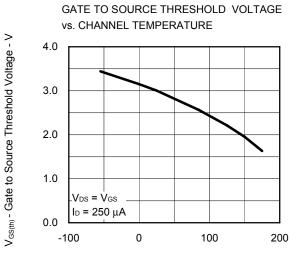
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 700 600 I_D - Drain Current - A 500 400 300 200 100 V_{GS} = 10 V Pulsed n 0 0.5 1.5 2 2.5 3 3.5



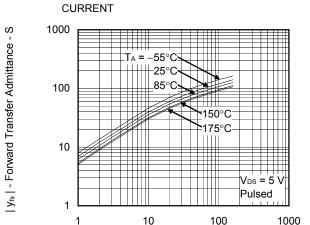
FORWARD TRANSFER ADMITTANCE vs. DRAIN

Ip - Drain Current - A

FORWARD TRANSFER CHARACTERISTICS

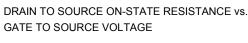


V_{DS} - Drain to Source Voltage - V

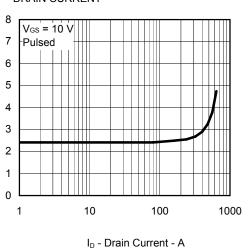


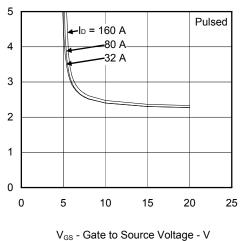


T_{ch} - Channel Temperature - °C



ID - Drain Current - A





RENESAS

 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

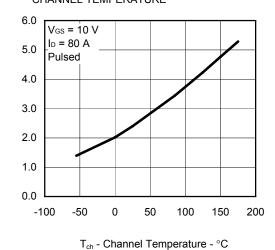
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

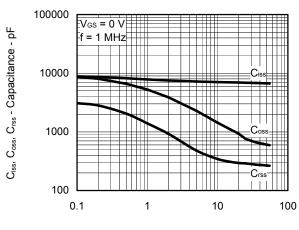
t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

I_F - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

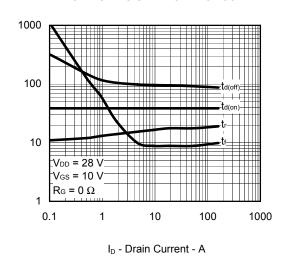


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

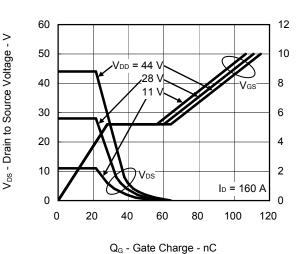


V_{DS} - Drain to Source Voltage - V

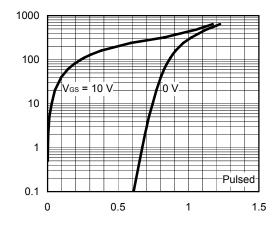
SWITCHING CHARACTERISTICS



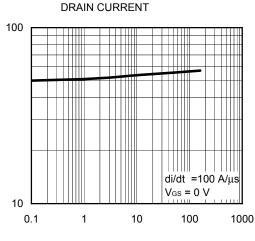
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs.



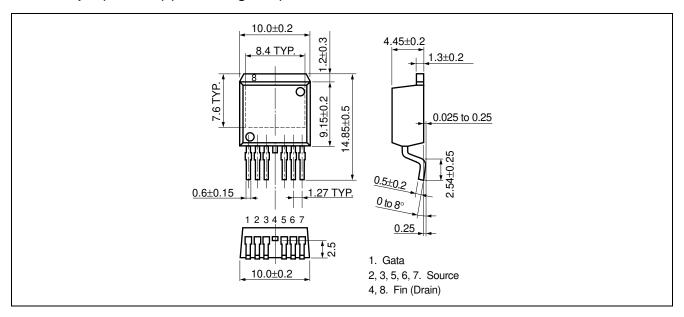
 $V_{F(S\text{-}D)}$ - Source to Drain Voltage - V

I_F - Drain Current - A

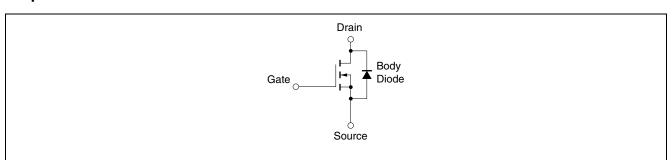
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

TO-263-7pin (MP-25ZT) (Mass: 1.5 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP160N055TUJ

		Description		
Rev.	Date	Page Summary		
1.00	Jul 01, 2010	-	First Eddition Issued	
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