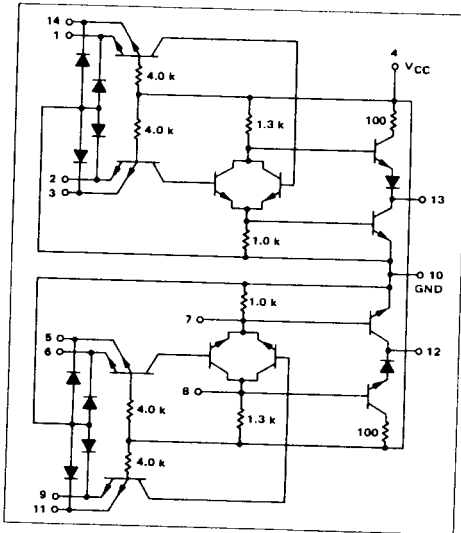


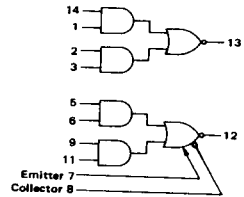
EXPANDABLE  
DUAL 2-WIDE 2-INPUT  
"AND-OR-INVERT" GATE

MTTL I MC500/400 series

MC520 • MC570  
MC420 • MC470



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC509 or MC510 expander series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$13 = (1 \cdot 14) + (2 \cdot 3)$$

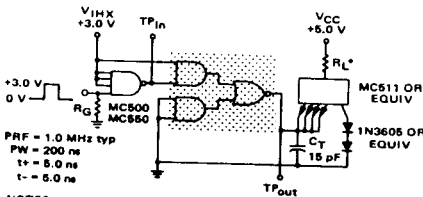
$$12 = (5 \cdot 6) + (8 \cdot 11) + (\text{Expander})$$

Total Power Dissipation = 40 mW typ/pkg  
Propagation Delay Time = 12 ns typ

TYPE NO.	INPUT LOADING FACTOR (I <sub>F</sub> )	OUTPUT DRIVE (I <sub>OL</sub> )	TEMPERATURE RANGE
MC520	1	15 MC500 series Gates (20 mA)	-55°C to +125°C
MC570	1	7 MC500 series Gates (10 mA)	
MC420	1	12 MC400 series Gates (20 mA)	0° to +75°C
MC470	1	6 MC400 series Gates (10 mA)	

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ

PW = 200 ns

t<sub>r</sub> = 5.0 ns

t<sub>f</sub> = 5.0 ns

NOTES:

R<sub>G</sub> = 50 ohms

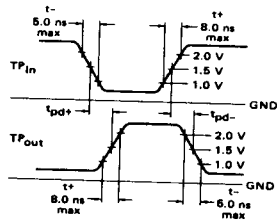
C<sub>T</sub> = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

When checking expander side, expander pins should be open.

\*MC520 - 260 Ω  
MC570 - 570 Ω  
MC420 - 330 Ω  
MC470 - 680 Ω



MC520, MC570/MC420, MC470 (continued)

**ELECTRICAL CHARACTERISTICS**

Test procedures are shown for only one gate. The other gates is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

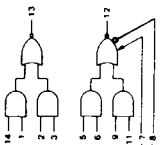


FIGURE 8

Characteristic	Symbol	Pin Under Test	MC520, MC570 Test Limits						MC420, MC470 Test Limits						Gnd†			
			-55°C		+25°C		+75°C		0°C		+25°C		+75°C					
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Input Forward Current	$I_F$	1	-1.33	-1.33	-1.33	-1.66	-1.66	-1.66	-1.66	max	-1.66	max	-	-	-	-	-	-
Leakage Current	$I_R$	1	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
Inverse Beta Current	$I_{BC}$	1	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
Breakdown Voltage	$BV_{in}^{(p)}$	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Output	$BV_{in}^{(T)}$	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Output Voltage	$V_{out}^{(p)}$	13	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
Leakage Current	$V_{out}^{(T)}$	13	2.5	2.5	2.4	2.3	2.3	2.4	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
Short-Circuit Current	$I_{SC}$	13	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45
Output Voltage	$V_{OH}$	13	2.6	0.40	0.40	0.45	0.40	0.40	0.40	0.40	0.40	0.45	0.40	0.45	0.40	0.45	0.40	0.45
Power (Total Device)	$I_{OH}$	13	3.2	3.35	3.0	3.1	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15
Power Supply Drain	$I_{max}$	4	-	10	-	-	10	-	-	10	-	-	10	-	-	10	-	-
Turn-On Delay	$t_{PDH}$	4	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
Turn-Off Delay	$t_{PDL}$	4	7.0	7.0	7.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0
Rise Time	$t_{pd}$	1,13	-	22	-	22	22	22	22	22	22	22	22	22	22	22	22	22
Fall Time	$t_{fd}$	1,13	-	22	-	22	22	22	22	22	22	22	22	22	22	22	22	22

\* Prime Pin-Out  
 † Ground inputs to gates not under test during ALL tests unless otherwise noted.  
 ‡ The inputs to all gates must be ungrounded.

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