HMC396

InGaP HBT GAIN BLOCK MMIC AMPLIFIER, DC - 8 GHz

Typical Applications

An excellent cascadable 50 Ohm Gain Block or LO Driver for:

- Microwave & VSAT Radios
- Test Equipment
- Military EW, ECM, C[3]I
- Space Telecom

Features

Gain: 12 dB

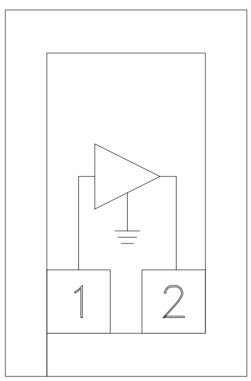
P1dB Output Power: +14 dBm

Stable Gain Over Temperature

50 Ohm I/O's

Small Size: 0.38 x 0.58 x 0.1 mm

Functional Diagram



General Description

The HMC396 die is a GaAs InGaP Heterojunction Bipolar Transistor (HBT) Gain Block MMIC DC to 8 GHz amplifier. This amplifier can be used as either a cascadable 50 Ohm gain stage or to drive the LO of HMC mixers with up to +16 dBm output power. The HMC396 offers 12 dB of gain and an output IP3 of +30 dBm while requiring only 56 mA from a +5V supply. The Darlington feedback pair used results in reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components. The HMC396 can easily be integrated into Multi-Chip-Modules (MCMs) due to its small (0.22mm^2) size. All data is with the chip in a 50 Ohm test fixture connected via 0.025mm (1 mil) diameter wire bonds of minimal length 0.5mm (20 mils).

Electrical Specifications, Vs= +5.0V, Rbias= 22 Ohm, T_A = +25° C

Parameter		Min.	Typ.	Max.	Units
Gain	DC - 4.0 GHz 4.0 - 8.0 GHz		12 11		dB dB
Gain Variation Over Temperature	DC - 4.0 GHz 4.0 - 8.0 GHz		0.004 0.015		dB/ °C dB/ °C
Input Return Loss	DC - 4.0 GHz 4.0 - 8.0 GHz		15 12		dB dB
Output Return Loss	DC - 4.0 GHz 4.0 - 8.0 GHz		19 17		dB dB
Reverse Isolation	DC - 8.0 GHz		16		dB
Output Power for 1 dB Compression (P1dB)	DC - 4.0 GHz 4.0 - 8.0 GHz		14 13		dBm dBm
Output Third Order Intercept (IP3)	DC - 4.0 GHz 4.0 - 8.0 GHz		30 24		dBm dBm
Noise Figure	DC - 8.0 GHz		6		dB
Supply Current (Icq)			56		mA

Note: Data taken with broadband bias tee on device output.

For price, delivery, and to place orders:
Analog Devices, Inc., One Analog Way, Wilmington, MA 01887
Phone: 781-937-1428 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

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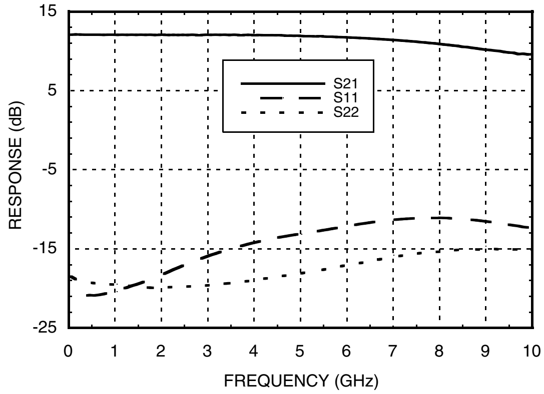
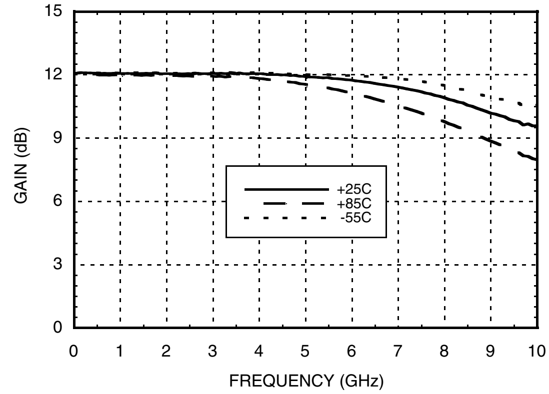
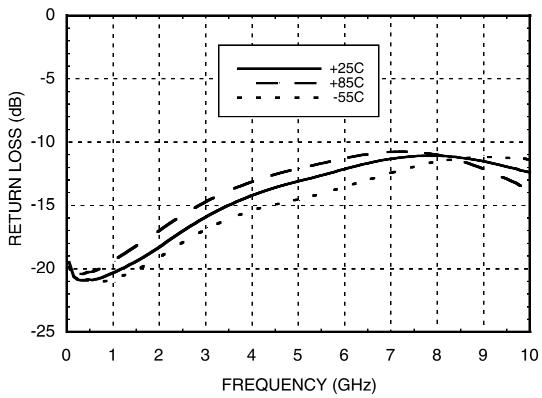
Gain & Return Loss



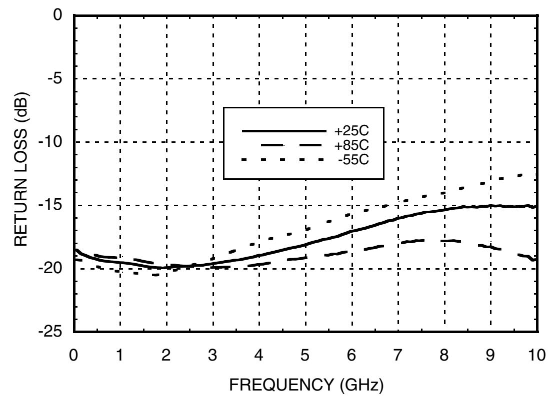
Gain vs. Temperature



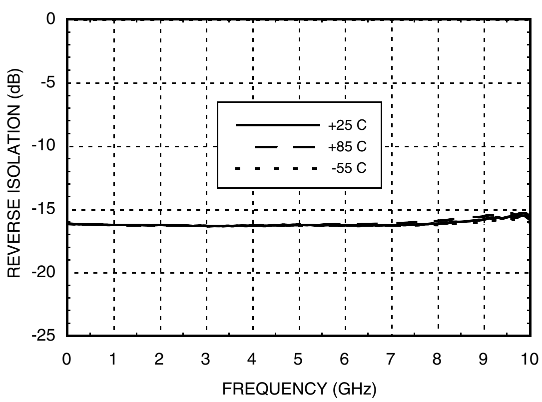
Input Return Loss vs. Temperature



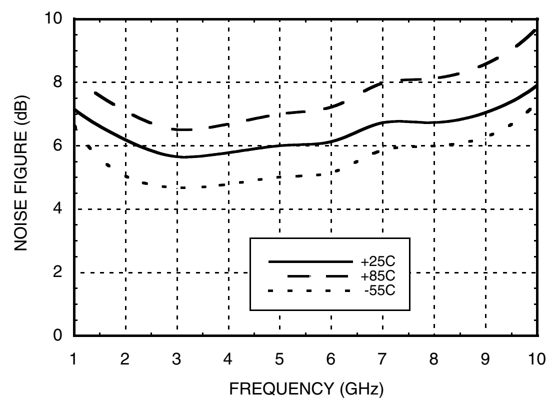
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



Noise Figure vs. Temperature



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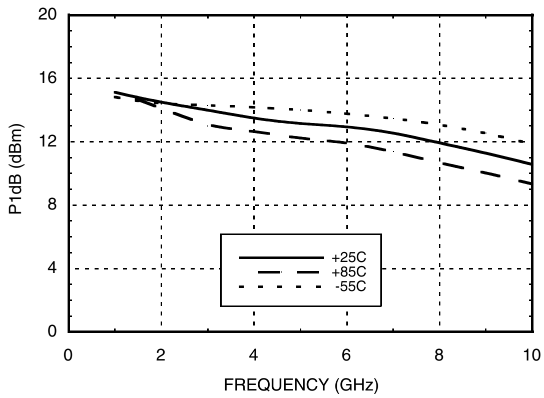
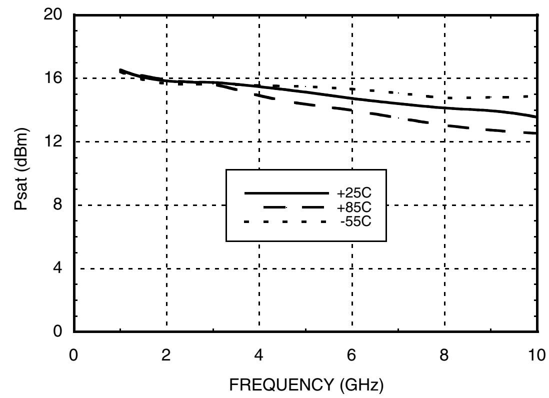
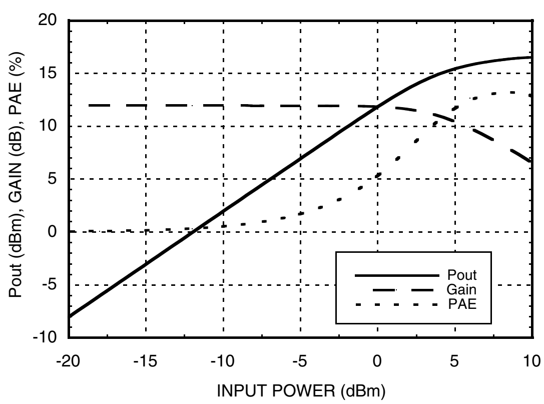
P1dB vs. Temperature



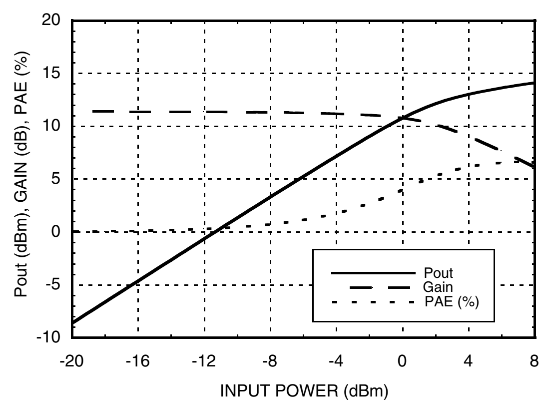
Psat vs. Temperature



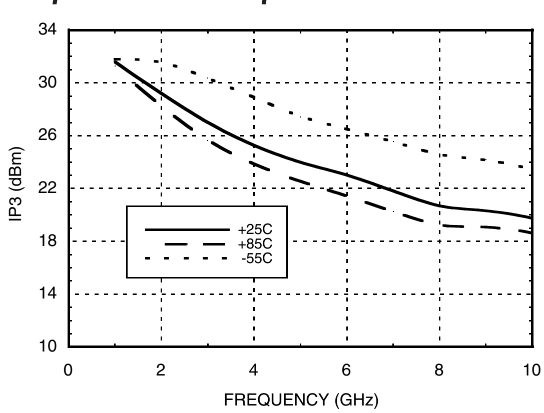
Power Compression @ 1 GHz



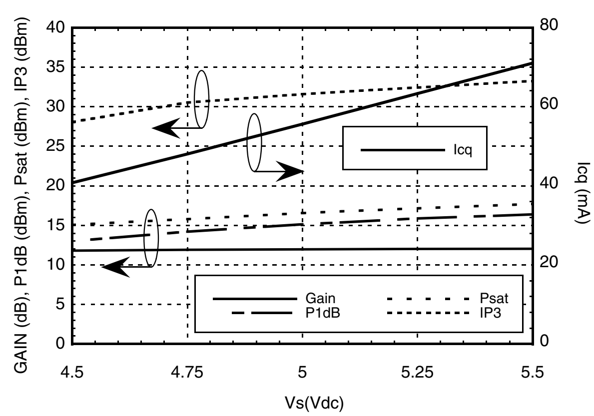
Power Compression @ 8 GHz



Output IP3 vs. Temperature



Gain, Power, OIP3 & Supply Current vs. Supply Voltage @ 1 GHz

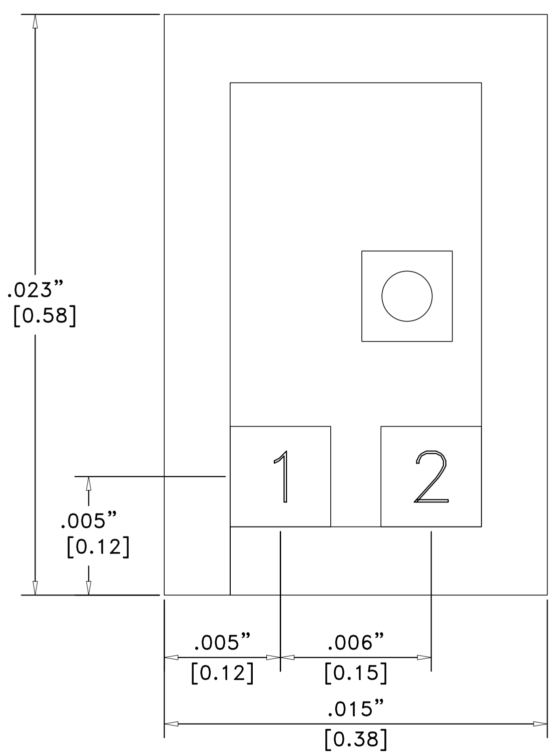


Absolute Maximum Ratings

Collector Bias Voltage (Vcc)	+7 Vdc
RF Input Power (RFIN)(Vcc = +5.0 Vdc)	+10 dBm
Junction Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 5.21 mW/°C above 85 °C)	0.339 W
Thermal Resistance (junction to die bottom)	192 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



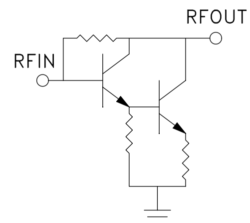
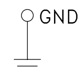
NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. ALL TOLERANCES ARE ±0.001 (0.025)
3. DIE THICKNESS IS 0.004 (0.100) BACKSIDE IS GROUND
4. BOND PADS ARE 0.004 (0.100) SQUARE
5. BOND PAD SPACING, CTR-CTR: 0.006 (0.150)
6. BACKSIDE METALLIZATION: GOLD
7. BOND PAD METALLIZATION: GOLD

Die Packaging Information [1]

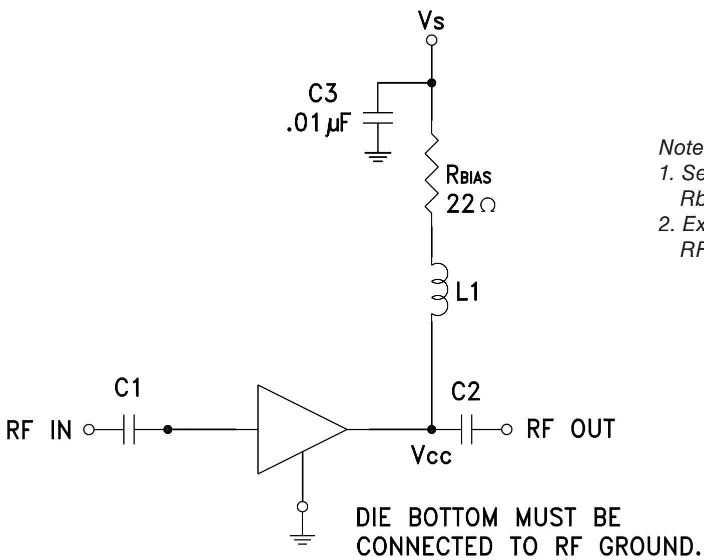
Standard	Alternate
GP-3 (Gel Pack)	[2]

[1] Refer to the “Packaging Information” section for die packaging dimensions.
[2] For alternate packaging information contact Analog Devices, Inc.

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
2	RFOUT	RF output and DC Bias for the output stage.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Application Circuit



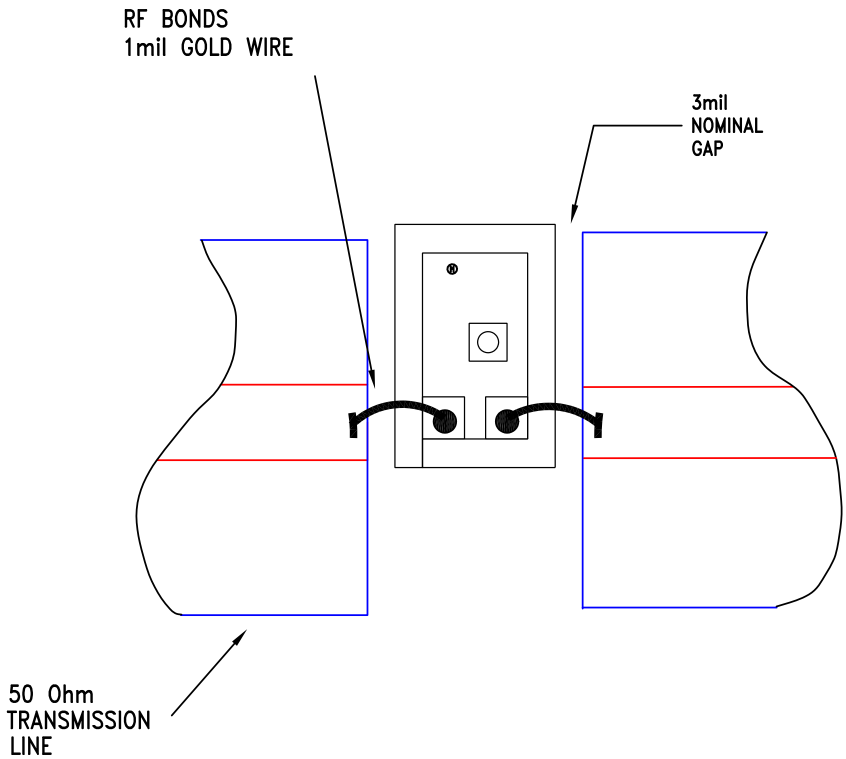
Note:
1. Select Rbias to achieve Icq using equation below, Rbias ≥ 22 Ohm.
2. External blocking capacitors are required on RFIN and RFOUT.

$$Icq = \frac{Vs - 3.9}{Rbias}$$

Recommended Component Values

Component	Frequency (MHz)			
	50	1000	4000	8000
L1	270 nH	56 nH	8.2 nH	2.2 nH
C1, C2	0.01 µF	100 pF	100 pF	100 pF

Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).