TEXAS INSTRUMENTS

Designing Low-Cost Buck Regulators Using The TL5001A

TL5001AEVM – 108/109/110

User's Guide

June 1999

Mixed-Signal Products

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Chapter 1

Hardware

The TL5001AEVM-108, TL5001AEVM-109, and TL5001AEVM-110 (SLVP108, SLVP109, and SLVP110) Buck Regulator DC/DC Converter Modules provide the user with a cost-effective solution for providing power to a high performance DSP such as the Texas Instruments TMS320C6201. The SLVP108 is a nominal 5-V input to 3.3-V output regulator. The SLVP109 is a 5-V to 2.5-V regulator, and the SLVP110 is a 5-V to 1.8-V regulator, all rated for up to 3-A output current. The SLVP108/109/110 converters provide a lower-cost replacement for the SLVP101/102/103 converters at the expense of 3% output voltage tolerance instead of the 1% for the latter modules. This chapter includes the following topics:

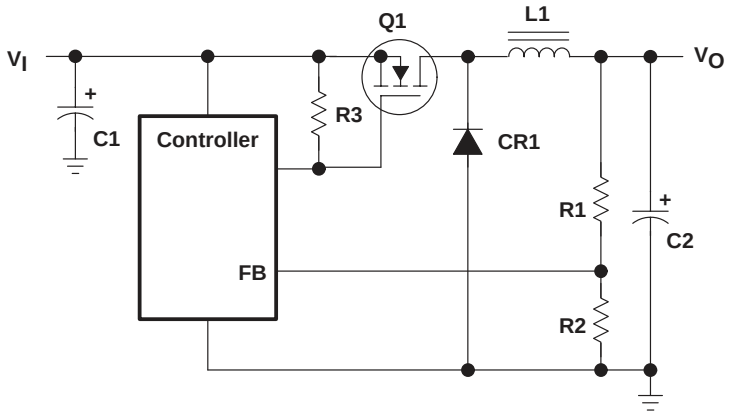
Topic **Page**

1.1 Introduction

Low cost and simplicity of design make buck converters popular solutions in dc/dc step-down applications where lack of isolation from the input source is not a concern.

Figure 1-1 shows a diagram of a typical buck converter. The converter passes a duty-cycle modulated pulse waveform through a low-pass output filter (L1, C2) to produce a dc voltage. An error amplifier senses the output voltage, compares it to a reference voltage and adjusts the width of the power switch (Q1) on time, to maintain the desired output voltage. A commutating diode (CR1) provides a path for inductor current to continue to flow when the power switch is turned off.

Figure 1–1. Typical Buck Converter Schematic Diagram



These Converter Modules are designed to provide I/O power (3.3 V) and Internal Core power (2.5 V, 1.8 V for Rev. 3 devices) to the Texas Instruments TMS320C6201 DSP. These modules satisfy all of the requirements for powering this high performance DSP such as low cost, low parts count, good transient response and excellent output voltage accuracy.

The TMS320C6201 DSP requires 3.3 V for I/O power and 2.5 V (1.8 V for Rev. 3) for Internal Core power. In order to provide power to this device, separate supplies must be used for each of the two voltages and proper power sequencing to the device must be provided. Both power supplies should always be brought up simultaneously to protect the device. If this is not possible, then the I/O supply (DVdd) must not exceed the core supply (CVdd) by more than 2 V, and CVdd must not exceed DVdd by more than 0.5 V. Both power supplies should achieve 95% of their voltage level within a 25-ms window, and should be able to handle an output current of 3 A (maximum consumption by the device).

In order to implement this modular approach to generating the required supply voltages, external circuitry must be added to insure that the sequencing requirements of the previous paragraph are met.

The SLVP108, SLVP109, and SLVP110 buck converters use the Texas Instruments TL5001A PWM controller to give power supply outputs of 3.3 V,

2.5 V, and 1.8 V at 0-A to 3-A with a 3% output voltage tolerance. Also featured in this design is the TPS2817 MOSFET driver IC. These converters operate over an input voltage range of 4.5-V to 6-V with typical efficiencies of 90% for 3.3 V out and 80% for 1.8 V out.

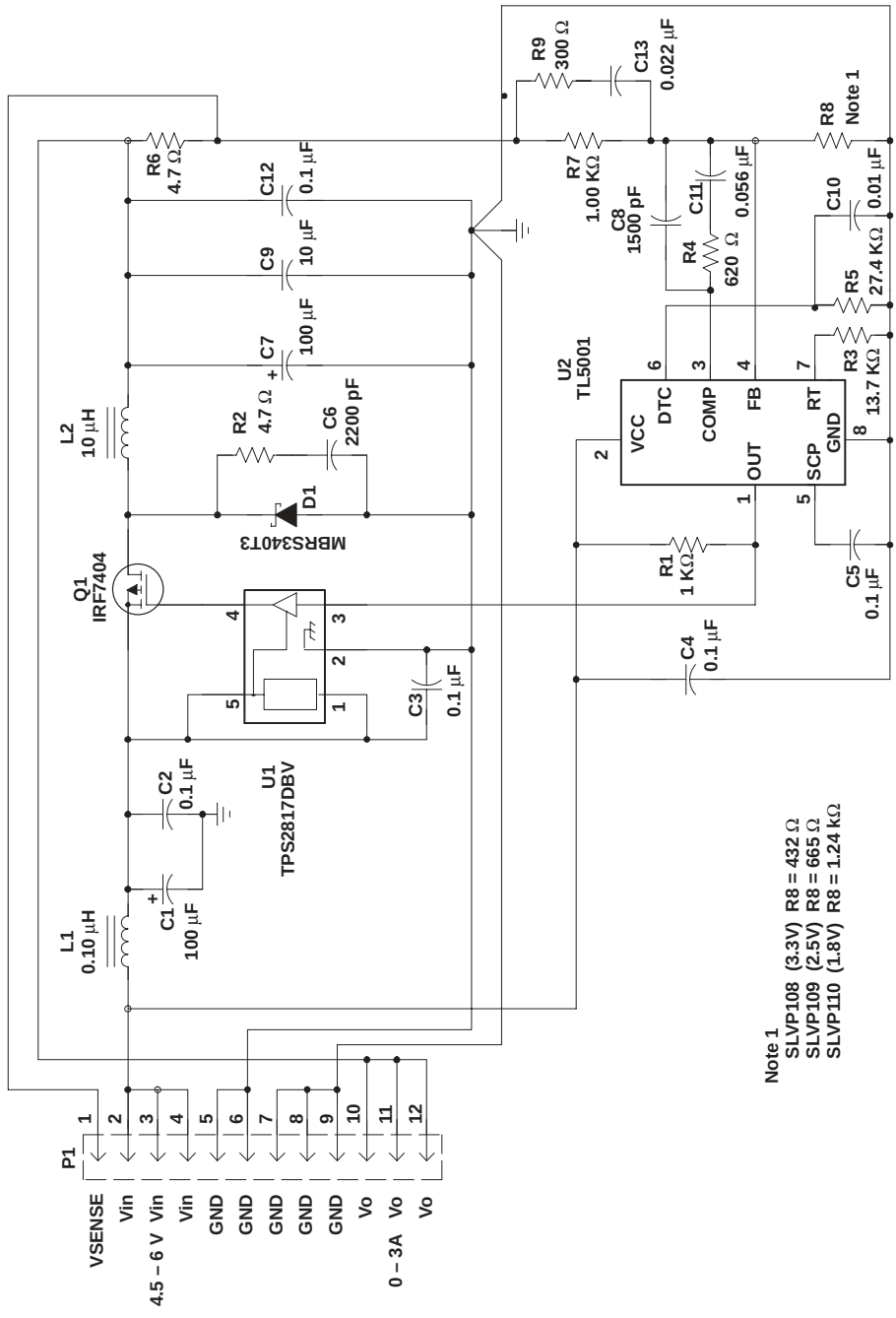
Chapter 2 lists full design specifications. The TL5001A controller IC provides the oscillator, the PWM comparator, undervoltage lock-out, and short circuit protection for the power supply. The oscillator sets the switching frequency. The PWM comparator compares the error amplifier output to a ramp voltage to produce the required pulse width for output voltage regulation. Undervoltage lock-out prevents the power supply from attempting to run when the input voltage is not sufficient for proper operation. Short circuit protection prevents accidental short circuits applied to the output from destroying the power supply.

Note:

The short circuit protection circuit provides protection from short circuits only. If the output load current is increased beyond the rated value, damage may occur to the power supply, i.e., short circuit protection does not imply overload protection.

1.2 Schematic

Figure 1–2. SLVP108/109/110 Schematic Diagram



1.3 Test Setup

For initial power up of the SLVP108, the following steps should be followed:

1) If necessary for improved load transient response, connect an external electrolytic capacitor of at least 100 μF from the SLVP108 output to ground. The external capacitor is not necessary for proper operation.

2) Connect an electronic load adjusted to draw approximately 1 A at 3.3 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is $I_O = \frac{3.3\ V}{R}$ where R is the value of the load resistor. The power rating of the resistor, P_R should be at least $\frac{(3.3)^2}{R} \times 2$.

3) Connect a lab power supply to the input of the SLVP108. Make sure that the current limit is set for at least 2 A. Turn the voltage up to 5 V.

4) Now verify that the SLVP108 output voltage (measured at the module output pins) is 3.3 V ± 0.10 V.

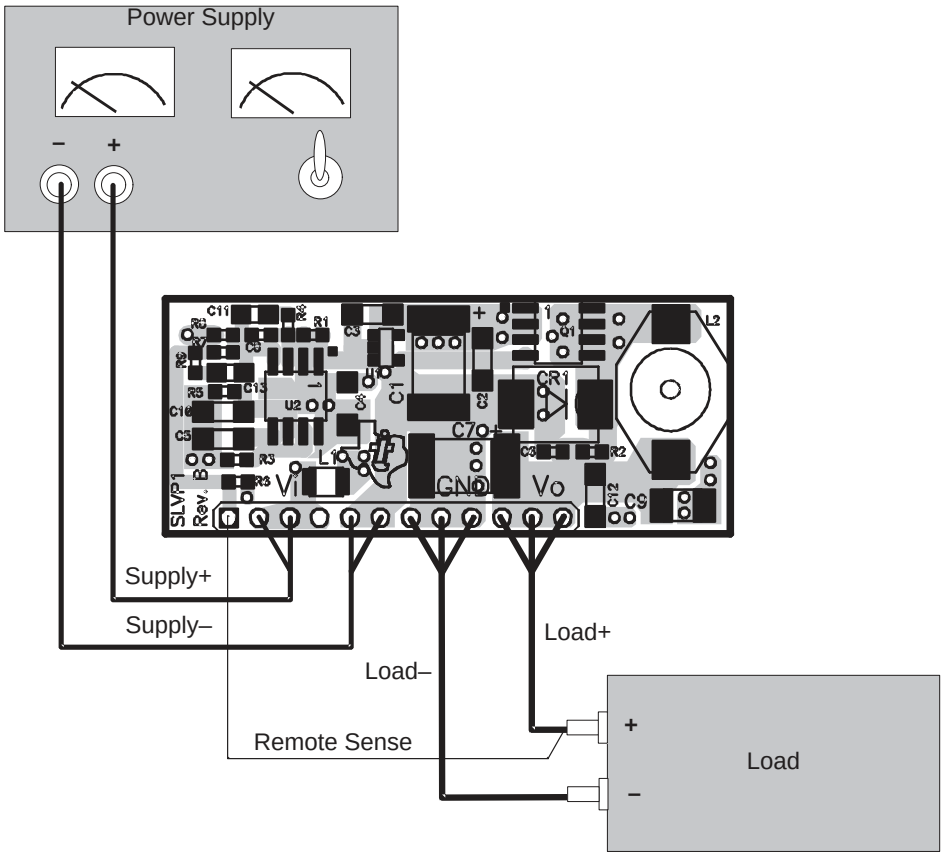
5) For subsequent testing, make sure the lab supply output current capacity and current limit are at least 3.5 A so that the SLVP108 can be operated at maximum load of 3 A.

6) Refer to Section 1.6 for selected typical waveforms and operating conditions for verification of proper module operation.

For initial power up of the other converters, simply replace any reference to 3.3 V in the above discussion with a reference to the appropriate output voltage.

Figure 1–3 shows the SLVP108 test setup.

Figure 1–3. Test Setup



1.4 Board Layout

Figure 1–4. Top Layer

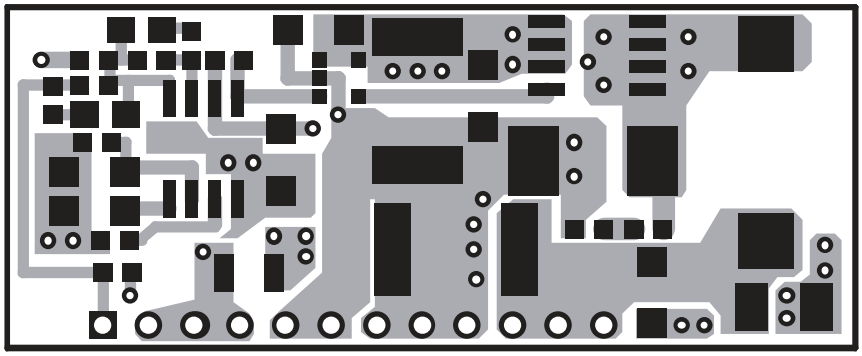


Figure 1–5. Bottom Layer (Top View)

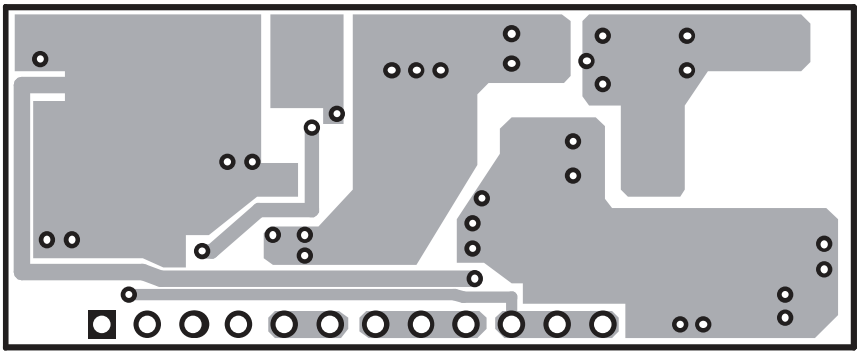


Figure 1–6. Silk Screen (Top Layer)

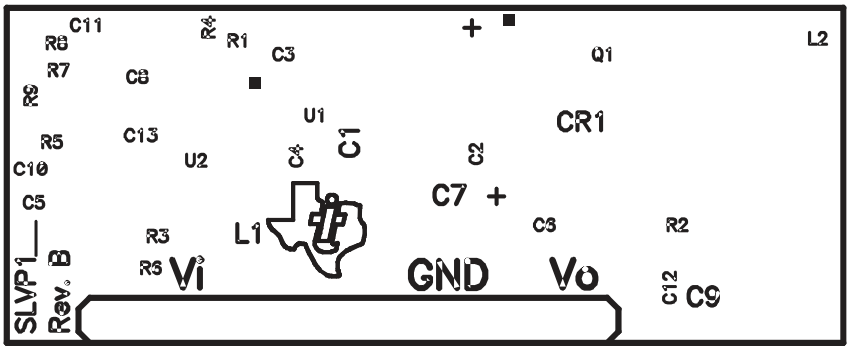
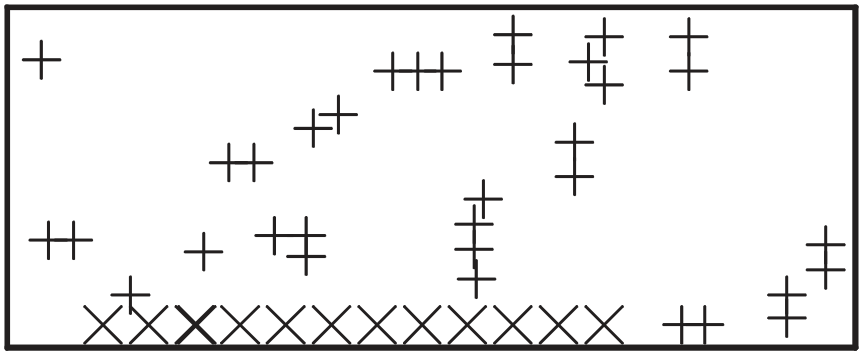


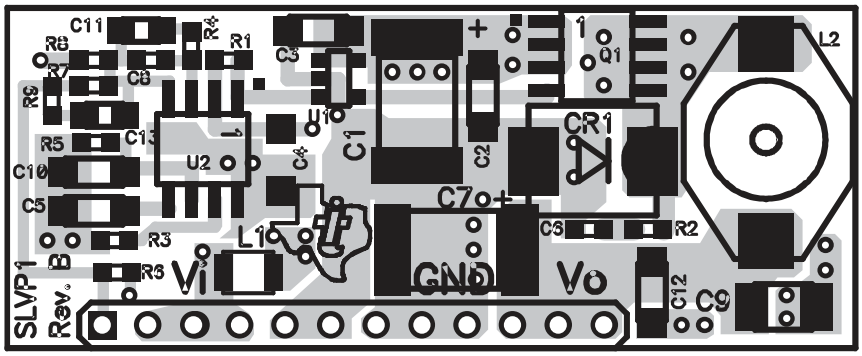
Figure 1–7. Drill Drawing



Drill Table			
Hole Dia (inch)	**Symbol**	**Quantity**	**Plated**
0.016	+	34	Yes
0.038	X	12	Yes

1.5 Assembly Drawing

Figure 1–8. Top Assembly Drawing



1.6 Bill of Materials

Table 1–1. Bill of Materials

Ref Des	Part Number	Description	Size	MFG
C1	10TPB100M	Capacitor, POSCAP, 100 µF, 10 V 20%	D	Sanyo
C2	GRM42-6X7R104M016A	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 20%	1206	muRata
C3	GRM42-6X7R104M016A	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 20%	1206	muRata
C4	GRM42-6X7R104M016A	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 20%	1206	muRata
C5	GRM42-6X7R104M016A	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 20%	1206	muRata
C6	GRM39X7R222M050A	Capacitor, Ceramic, 2200 pF, 50 V, X7R, 20%	603	muRata
C7	10TPB100M	Capacitor, POSCAP, 100 µF, 10 V 20%	D	Sanyo
C8	GRM39X7R152K050A	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 10%	603	muRata
C9	GRM235Y5V106Z016A	Capacitor, Ceramic, 10 µF, 16 V, Y5V, 80 –20%	1210	muRata
C10	GRM42-6X7R103M050A	Capacitor, Ceramic, 0.01 µF, 50 V, X7R, 20%	1206	muRata
C11	GRM40X7R563K050A	Capacitor, Ceramic, 0.056 µF, 50 V, X7R, 10%	805	muRata
C12	GRM442-6X7R104M016A	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 20%	1206	muRata
C13	GRM40X7R223K050A	Capacitor, Ceramic, 0.022 µF, 50 V, X7R, 10%	805	muRata
D1	MBRS340T3	Diode, Schottky, 3 A, 40 V	SMC	Mot
L1	S1008-101K	Inductor, SM, Shielded, 0.1 µH, 2.13 A, 25 mΩ	1008	Delevan
L2	DO3316P-103	Inductor, 10 µH, 3.9 A, 0.025 mΩ	0.51×0.37	Coilcraft
P1	PTC36SBBN	Header, Right Angle, 12-pin, 0.1 ctrs, 0.2″ pins	0.1	Sullins
Q1	IRF7404	MOSFET, P-ch, 20 V, 6.8 A, 40 mΩ	SO-8	IR
R1		Resistor, SMD, MF, 1.0 KΩ, 1/16 W, 5%	603	
R2		Resistor, SMD, MF, 4.7 Ω, 1/16 W, 5%	603	
R3		Resistor, SMD, MF, 13.7 KΩ, 1/16 W, 1%	603	
R4		Resistor, SMD, MF, 620 Ω, 1/16 W, 5%	603	
R5		Resistor, SMD, MF, 27.4 KΩ, 1/16 W, 1%	603	
R6		Resistor, SMD, MF, 4.7 Ω, 1/16 W, 5%	603	
R7		Resistor, SMD, MF, 1.00 KΩ, 1/16 W, 1%	603	
R8A		Resistor, SMD, MF, 432 Ω, 1/16 W, 1% (SLVP108 Only)	603	
R8B		Resistor, SMD, MF, 665 Ω, 1/16 W, 1% (SLVP109 Only)	603	
R8C		Resistor, SMD, MF, 1.24 KΩ, 1/16 W, 1% (SLVP110 Only)	603	
R9		Resistor, SMD, MF, 300 Ω, 1/16 W, 5%	603	
U1	TPS2817DBV	IC, MOSFET Driver, Single Ch, 2 A	SOT25	TI
U2	TL5001AD	IC, PWM Controller	SO-8	TI

1.7 Test Results (SLVP108)

Figure 1–9. Load Regulation

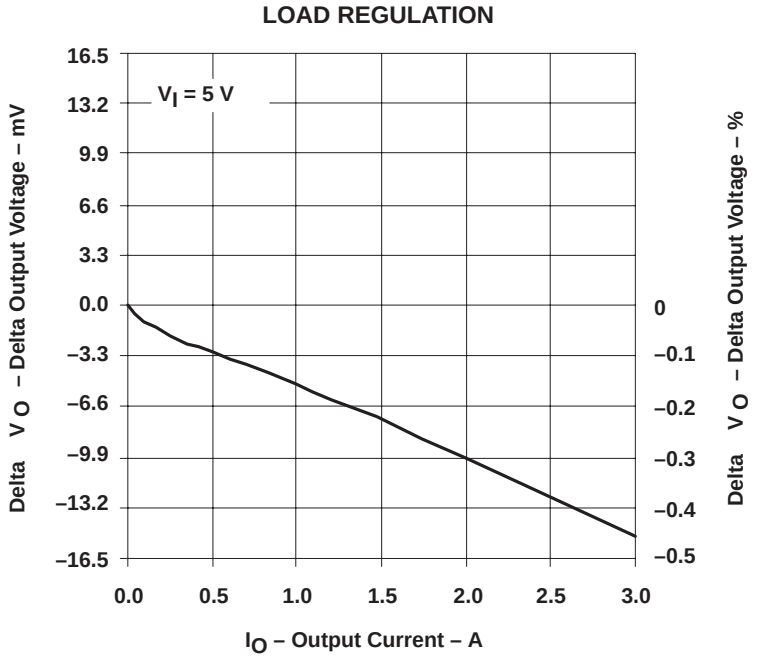


Figure 1–10. Line Regulation

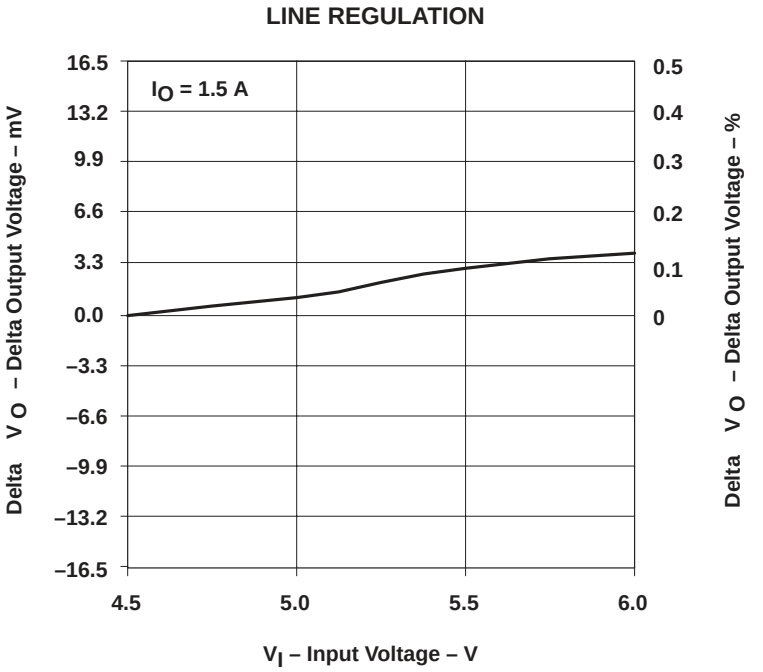


Figure 1–11. Efficiency

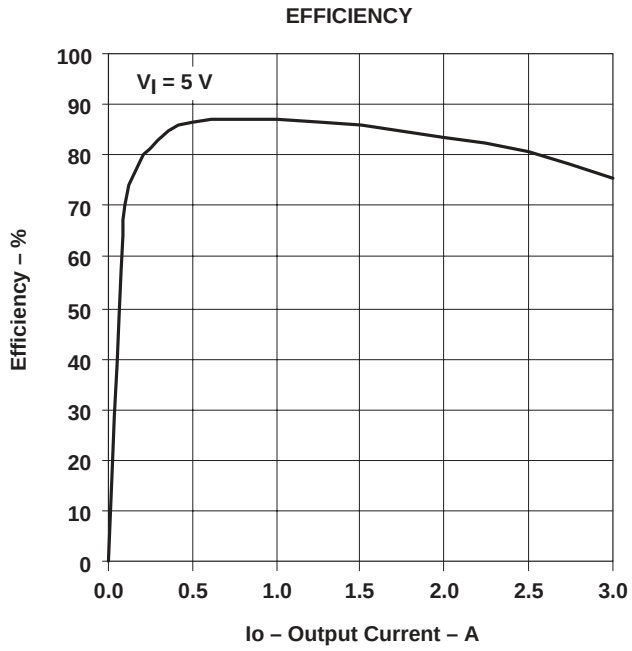


Figure 1–12. VDRAIN-To-GND Voltage

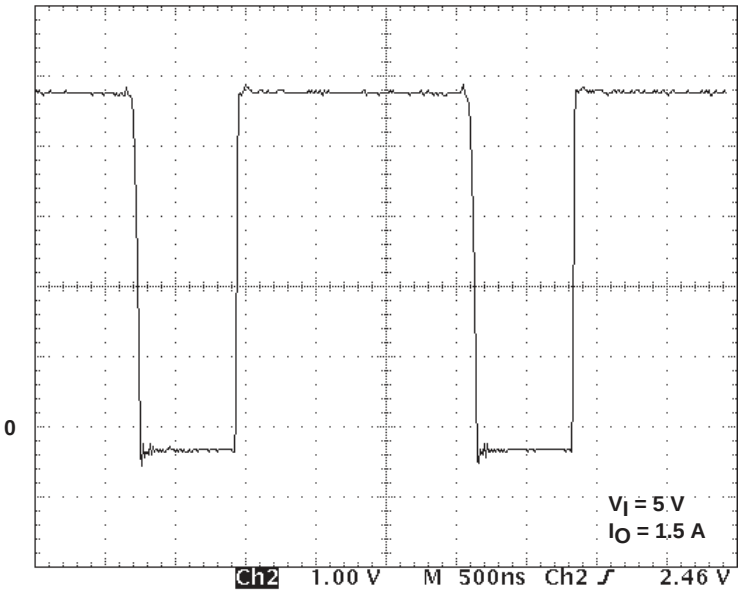


Figure 1–13. Power Switch Rise Time

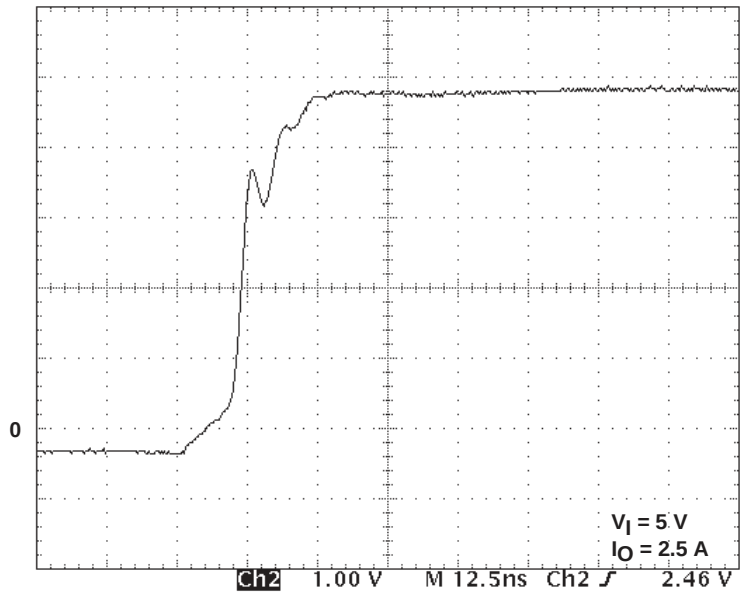


Figure 1–14. Power Switch Fall Time

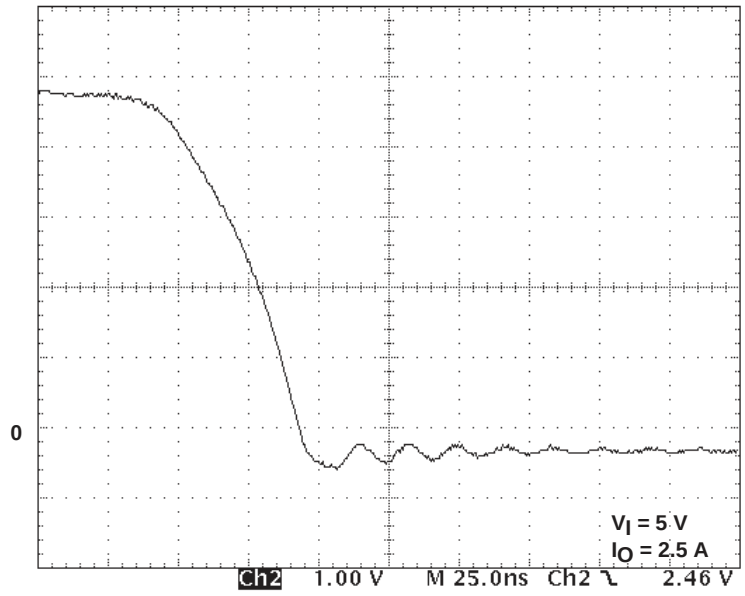


Figure 1–15. Output Voltage Ripple

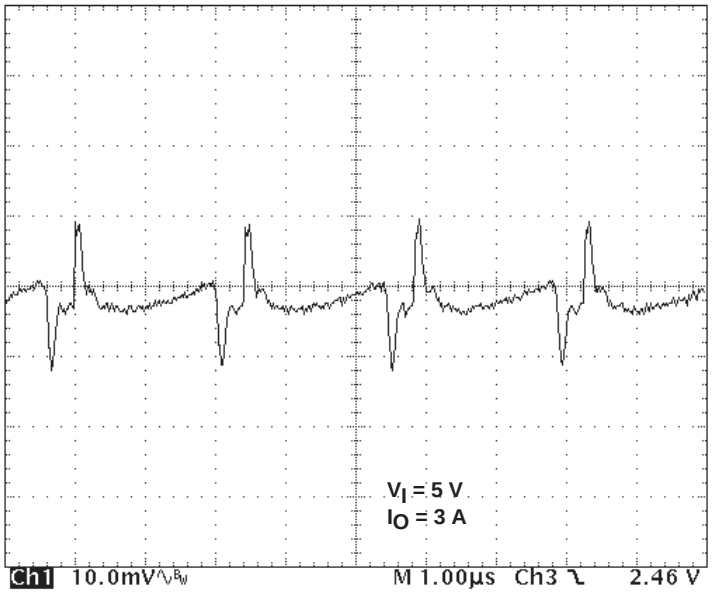
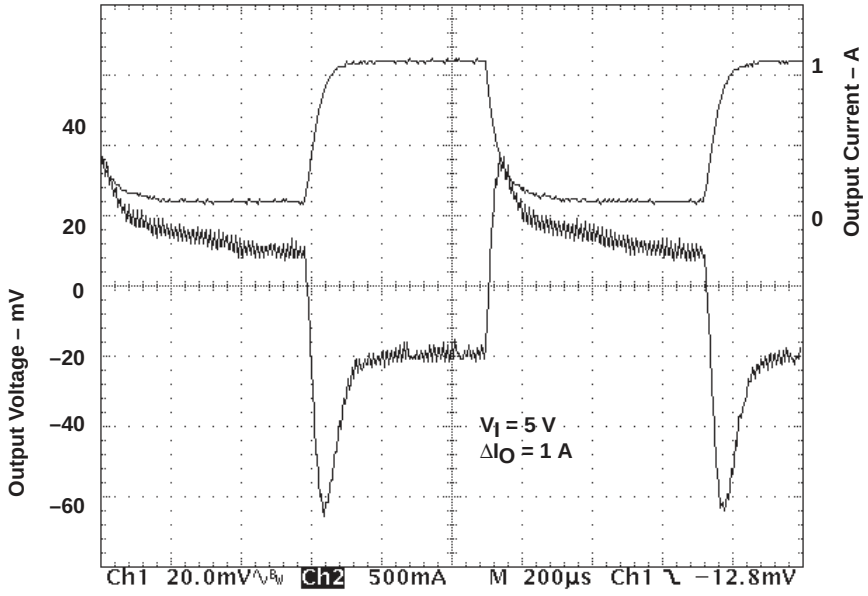


Figure 1–16. Load Transient Response



Chapter 2

Design Procedure

The SLVP108, SLVP109, and SLVP110 Buck Regulator DC/DC Converter Modules provide a method for evaluating the performance of the TPS2817 MOSFET driver and the TL5001A PWM controller. The TPS2817 contains all of the circuitry necessary to drive large power MOSFET transistors and includes a voltage regulator for higher voltage applications. This section explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP108, SLVP109, and SLVP110 are dc-dc buck converter modules that provide a regulated output voltage at up to 3.0 A with an input voltage range of 4.5 V to 6 V. The controller is a TL5001A PWM operating at a nominal frequency of 400 kHz. The TL5001A is configured for a maximum duty cycle of 100 percent and has soft-start and short-circuit protection built in. The output voltage has a ±3% tolerance. Using the procedure given below, the user can modify this design for any similar application.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP108, SLVP109, and SLVP110.

Table 2–1. Operating Specifications†

Specification		Min	Typ	Max	Units
Input voltage range		4.5		6	V
Static voltage tolerance (see Note 1)	SLVP108	3.2	3.3	3.4	V
	SLVP109	2.4	2.5	2.6	
	SLVP110	1.7	1.8	1.9	
Line regulation (see Note 2)			±4		mV
Load regulation (see Note 3)			±15		mV
Transient response (see Note 4)			±100		mVpk
			100		µsec
Output current range (see Note 5)		0		3	A
Current limit (see Note 6)			NA	NA	
Operating frequency†			400		kHz
Output ripple†			20		mVp-p
Efficiency, 3 A load	SLVP108		78%		
	SLVP109		75%		
	SLVP110		70%		
Efficiency, 1.5 A load	SLVP108		88%		
	SLVP109		82%		
	SLVP110		77%		

† Unless otherwise specified, all test conditions are T_A = 25°C, V_I = 5 V, I_O = 3 A, V_O = nominal.

Notes: 1) V_I = 5 V, I_O = 1.5 A.
2) I_O = 1.5 A.
3) V_I = 5 V
4) V_I = 5 V, I_O stepped repetitively from 0.1 A to 1.1 A
5) Output current rating is limited by thermal considerations. Load currents above this rating may cause damage to the power supply.

2.3 Design Procedures

Detailed steps in the design of a buck topology converter may be found in *Designing With the TL5001C PWM Controller* (literature number SLVA034) from Texas Instruments. This section shows the basic steps involved in this design, for a nominal 3.3-V output.

2.3.1 Duty Cycle Estimate

The duty cycle, D, is the ratio of the power switch conduction time to the period of one switching cycle. An estimate of the duty cycle is used frequently in the following sections. The duty cycle for a continuous mode step–down converter is approximately:

$$D = \frac{V_O + V_D}{V_I - V_{SAT}}$$

From the manufacturer's data sheet for the commutating diode, the forward voltage is V_D = 0.45 V at 3-A forward current. Similarly, from the IFR7404 data sheet, the switch ON voltage, V_{SAT}, can be estimated by multiplying the drain-source on resistance, $R_{DS(on)}$, of 40 mΩ by the on state drain current, I_D, of 3 A giving 0.12 V. The duty cycle for V_I = 4.5, 5, and 6 V is 0.86, 0.77, and 0.64, respectively.

2.3.2 Output Filter

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 15 percent of the rated output load (This value can range from 5% to 15%):

$$\Delta I_O = 2 \times 0.15 \times I_O = 2 \times 0.15 \times 3 = 0.9\ A$$

The inductor value needed is :

$$L = \frac{\left(V_I - V_{SAT} - V_O\right) \times D \times t}{\Delta I_O}$$

using a temperature-adjusted V_{SAT} of $0.12 \times 1.3 = 0.156$:

$$L = \frac{(9 - 0.156 - 3.3) \times 0.64 \times \left(2.5 \times 10^{-6}\right)}{0.9} = 9.86\ \mu H$$

The two criteria for selecting the output capacitor are the amount of capacitance needed and the capacitor's equivalent series resistance, ESR. After the capacitance and ESR requirements are determined, the capacitor can be selected.

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times \left(\Delta V_O\right)} = \frac{0.45}{8 \times \left(400 \times 10^3\right) \times 0.03} = 4.69\ \mu F$$

Now, assuming the capacitance is very large, the ESR needed to limit the ripple to 30 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.03}{0.9} = 0.033\ \Omega$$

To provide margin, the output filter capacitor should be rated greater than the calculated capacitance and have lower ESR than calculated. Due to available volume, this design uses a 100-μF electrolytic in parallel with a 10-μF ceramic capacitor. This capacitance provides adequate filtering with good load transient response.

2.3.3 Power Switch

The design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. The IRF7404 p-channel power MOSFET is selected for it's low rDS(on) of 40 mΩ and drain-to-source breakdown voltage of 20 V.

Power dissipation, which includes both conduction and switching losses, is given by:

$$P_D = \left(I_O^2 \times r_{DS(ON)} \times D\right) + \left(0.5 \times V_I \times I_O \times t_{r+f} \times f\right)$$

An example power MOSFET power dissipation calculation follows with the following assumptions:

The total switching time, t_{r+f} = 100 ns,
An $r_{DS(ON)}$ high temperature adjustment factor = 1.3,
A 55°C maximum ambient temperature,
V_I = 5 V and
I_O = 3 A then :

$$P_D = \left(3.0^2 \times (0.040 \times 1.3) \times 0.77\right) + \left(0.5 \times 5 \times 3 \times 100 \times 10^{-9} \times 400\ kHZ\right)$$

$$= 0.36 + 0.30 = 0.66\ W$$

The thermal impedance, $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (90 \times 0.66) = 114.4°C$$

Conduction losses are nearly equal to switching losses in this application but may not be in others. It is good practice to check dissipation at the extreme limits of input voltage to find the worst case.

2.3.4 Rectifier

The catch rectifier conducts during the time interval when the MOSFET is off. The MRBS340T3 is a 3-A, 40-V rectifier in a surface-mount SMC package.

For the same operating conditions as above, the rectifier power dissipation is:

$$P_D = I_O \times V_D \times (1–D) = 3 \times 0.45 \times 0.23 = 0.31\ W$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and the rectifier connect. The snubber design is very dependent on PWB layout and component parasitics, but as a starting point, select a snubber capacitor with a value that is 4 to 10 times larger than the estimated capacitance of the catch rectifier. The power dissipated in the snubber resistor is directly proportional to this capacitor value, so this value should be chosen with care. The MBRS340T3 has a capacitance of about 150 pF at a reverse voltage of 5 V. For this design, a capacitor value of 2200 pF was selected. A resistor value of 4.7 Ω was then selected. The resistor value selection is often a trial and error sequence of steps, but it should be chosen so that the snubber RC time constant times 3 is less than the minimum ON time of the power switch. This allows the snubber capacitor to fully charge and discharge during each portion of the switching period.

2.3.6 Controller Functions

The TL5001A controller functions, oscillator frequency, soft-start, dead-time control, and short-circuit protection, are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in Figure 6 of the TL5001A data sheet. For 400 kHz, a value of 13.7 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100% is chosen. Then R is calculated as:

$$R_{DT} = \left(R_{OSC} + 1.25\ k\Omega\right) \times \left[D \times \left(V_{OSC(100\%)} - V_{OSC(0\%)}\right) + V_{OSC(0\%)}\right]$$

$$= (13.7\ k\Omega + 1.25\ k\Omega) \times [1 \times (1.5 - 0.5) + 0.5] = 22.4\ k\Omega$$

Any value higher than the calculated value will be satisfactory since the duty cycle limit is 100%. A value of 27.4 kΩ is used in this design.

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 100 μs is used:

$$C = \frac{3 \times t_R}{R_{DT}} = \frac{3 \times 100 \times 10^{-6}}{27.4\ k\Omega} = 0.011\ \mu F \Rightarrow 0.01\ \mu F$$

The TL5001A has short circuit protection (SCP) instead of a current sense circuit. If not used, the SCP terminal must be connected to ground to allow the converter to start up. If used, a timing capacitor is connected to SCP that should have a time constant that is at least 10 times greater than the soft-start time constant. This time constant is chosen to be 10 ms:

$$C(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.01\ s = 0.125\ \mu F \Rightarrow 0.1\ \mu F$$

It should be emphasized here that the power supply is rated for a maximum output current of 3 A. This limit is due to thermal considerations. Although the

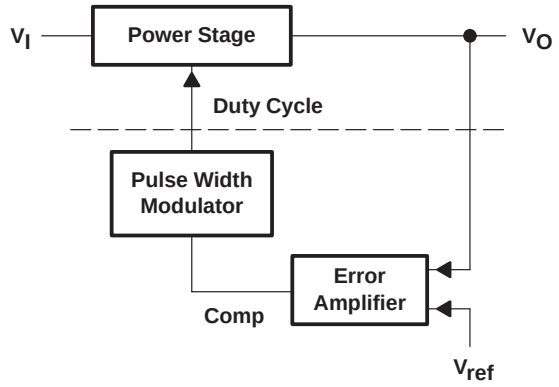
power supply has short circuit protection, it does not have overload protection. If a load current in excess of 3 A is applied, the power supply may fail or have a reduced lifetime.

In addition, if a short circuit is applied to the power supply, the short-circuit protection internal to the TL5001A will latch the power supply into an OFF state. To reset the latch, power must be removed from the input of the power supply and reapplied after the output short circuit is removed.

2.3.7 Loop Compensation

The control loop for this converter consists of three gains: the power stage (G_{PS}), the error amplifier ($G_{E/A}$), and the internal TL5001A PWM modulator (G_{PWM}). Figure 2–1 shows a simplified block diagram of the control loop. Negative feedback stabilizes the output voltage against changes in line or load without destroying the control-loop's ability to respond to line and/or load transients. To maintain good performance and stability, it is necessary to tailor the open-loop frequency response of the converter. The frequency response of the error amplifier is shaped by judicious selection of external components to obtain a desired overall open-loop response. This tailoring of the converter frequency response is called loop compensation. A detailed treatment of dc-to-dc converter stability analysis and design is beyond the scope of this report; however, several references on the subject are available.

Figure 2–1. Control Loop Simplified Block Diagram



The following is a simplified approach to designing networks to stabilize continuous mode buck converters that works well when the open-loop gain is below unity at a frequency at least one-half of the switching frequency of the power supply.

Before the error-amplifier frequency response can be designed, the frequency response of the rest of the control loop must be determined. As mentioned above, this consists of the power stage gain and phase and the pulse width modulator gain and phase.

The first component of the control loop to be determined is the power stage. A gain block and a damped LC filter with a double complex pole can approximate the frequency response of the buck power stage operating in continuous conduction mode. There is also a zero due to the ESR of the

external output capacitance. The low frequency magnitude of the gain is the change in output voltage divided by the change in the duty cycle. Without going through the detailed derivation, a simplified expression for the gain of this continuous–mode buck power stage is:

$$G_{PS}(s) = \frac{\Delta V_O}{\Delta D} = V_I \times \frac{R}{R + R_L} \times \frac{1 + s \times R_C \times C_O}{\left[1 + s \times \left(R_C \times C_O + \frac{L}{R}\right) + s^2 \times \left(L \times C_O \times \left(1 + \frac{R_C}{R}\right)\right)\right]} \times \frac{1}{1 + s \times C_{CER} \times \frac{R \times R_C}{R + R_C}}$$

Where:

R = load resistance = 1.1 Ω
C_O = 110-µF total output capacitance
R_C = ESR of aluminum electrolytic capacitance ≅ 75 mΩ
C_{CER} = 10-µF internal ceramic capacitance
L = 10-µH internal output inductor value
R_L = equivalent resistance of internal inductor and FET
$R_{DS(on)}$ ≅ 65 mΩ.

The double pole from the LC filter is at a frequency of :

$$\frac{1}{2 \times \pi \times \sqrt{L \times C_O \times \left(1 + \frac{R_C}{R}\right)}} = 4.64 \ kHz$$

The zero due to the output capacitance and its ESR is at a frequency of :

$$\frac{1}{2 \times \pi \times R_C \times C_O} = 19.3 \ kHz$$

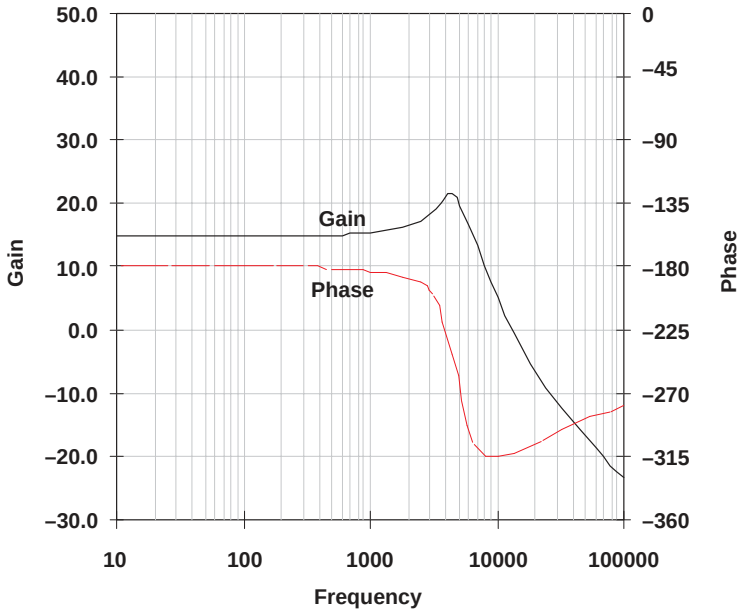
The second component of the control loop to be determined is the pulse width modulator. The response of a voltage-mode pulse-width modulator can be modeled as a simple gain block. The magnitude of the gain is the change in power supply output voltage for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). From the TL5001A Data Sheet, Figure 11, PWM Triangle Wave Amplitude vs Frequency, the maximum triangle wave voltage at 400 kHz is approximately 1.5 V and the minimum is 0.5 V. As the error-amplifier voltage swings from 0.5 V to 1.5 V, the power supply output voltage changes from 0 V to 5 V.

Thus, the gain, G_{PWM}, is:

$$G_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{5–0}{1.5–0.5} = 5.0 \Rightarrow 14 \ dB$$

The product (sum in dB) of the gains of these two control loop components, the power stage gain, G_{PS}, and the pulsewidth-modulator gain, G_{PWM}, makes up the uncompensated open–loop response. Figure 2–2 is a gain (solid line) and phase (dashed line) graph of the uncompensated open-loop response of the converter obtained from a MathCad analysis. The operating conditions for the graph below are: V_I = 5 V, I_O = 3 A, C_O = 110 µF, and R_C = 0.075 Ω.

Figure 2–2. Uncompensated Open-Loop Response



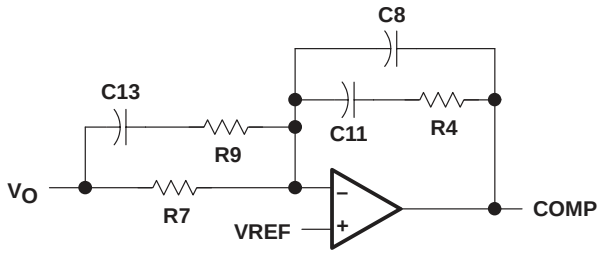
Now that the known parts of the control loop are determined, the error-amplifier frequency response can be designed. Unless the designer is trying to meet an unusual requirement, such as very wideband response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are at the discretion of the designer. Generally, the total open-loop response favored for stability is a 20-dB-per-decade rolloff with a desired phase margin of at least 30 degrees for all conditions. High gain at low frequencies is desired to minimize error in the output voltage and sufficient bandwidth must be designed into the circuit to assure that the converter has good transient response. These requirements can be met by adding compensation components around the error amplifier to modify the total loop response.

Therefore, the error amplifier design should provide the following:

- ❑ A pole at dc to give high low frequency gain
- ❑ Two zeroes near the filter poles to correct for phase shift due to the power stage frequency response
- ❑ Two additional poles to roll off high frequency gain

The compensation circuit shown in Figure 2–3 is used to implement the above functions.

Figure 2–3. Error-Amplifier Compensation Network



The first step in the design of the error-amplifier frequency response is the design of the output sense divider. This sets the output voltage, and the top resistor, R7, determines the relative impedance of the rest of the compensation design. A 1-kΩ resistor for the top of the divider gives a divider current of 2.3 mA for an output setting of 3.3 V and a Vref of 1 V. The bottom of the divider (omitted from Figure 2–3 for clarity) is calculated as:

$$R = V_{ref} \times \frac{R7}{V_O - V_{ref}} = 1\ V \times \frac{1.00\ k\Omega}{V_O - 1} = 435\ \Omega \Rightarrow 432\ \Omega$$

For 2.5-V operation, this resistor would be 665 Ω and for 1.8-V operation, it would be 1.24 kΩ. The advantage of changing the bottom resistor instead of the top divider resistor is that the compensation does not change with output voltage changes. The disadvantage is that divider current changes with changes in the output voltage and should be sufficient at the lowest voltage to make the error amplifier input bias current insignificant.

The transfer function for the circuit in Figure 2–3 is:

$$\frac{V_{COMP}}{V_O} = (-1) \times \frac{\left(f_{Z1}\right) \times \left(f_{Z2}\right)}{\left(f_{P1}\right) \times \left(f_{P2}\right) \times \left(f_{P3}\right)}$$

$$= (-1) \times \frac{[1 + s \times C13 \times (R7 + R9)] \times [1 + s \times C11 \times R4]}{[s \times R7 \times (C8 + C11)] \times [1 + s \times R9 \times C13] \times \left[1 + s \times R4 \times \frac{(C8 \times C11)}{(C8 + C11)}\right]}$$

These poles and zeros must be calculated to adjust the total loop response and desired gain-bandwidth. With R7 already selected, the next step is to calculate the pole at dc (the integrator) in order to give the correct crossover frequency. The capacitance C8 + C11 along with R7 provides this pole and also positions the gain at low frequencies. A crossover frequency of 30 kHz is selected. The higher the crossover, the better the transient response (assuming that the crossover frequency is much less than the operating frequency).

At 30 kHz, the gain of the modulator stage, as shown in Figure 2–2, is –11 dB. The sum of this gain, the integrator gain, and the two zeros must equal zero at 30 kHz. The zeros will be positioned around the LC filter poles (~ 4.64 kHz) and will have a gain of:

$$2 \times \left(20 \times Log\left(\frac{30\ kHz}{4.64\ kHz}\right)\right) = 32.4\ dB$$

Therefore, the required gain due to the integrator is 0 – (11 +32.4) = –21.4 dB, or a voltage gain of 0.0851. The integrator capacitance can now be calculated. In practice, C8 is much smaller than C11 and can usually be ignored:

$$C11 = \frac{1}{2 \times \pi \times f_{CO} \times R7 \times 0.0851} = 0.062\ \mu F \Rightarrow 0.056\ \mu F$$

The frequency of the first error amplifier zero, f_{Z1}, is used to compensate for one of the LC filter poles (4.64 kHz). Assuming a value for R9 of about 1/3 of R7, then C13 is:

$$C13 = \frac{1}{2 \times \pi \times f_{Z1} \times (R7 + R9)} = 0.026\ \mu F \Rightarrow 0.022\ \mu F$$

The second error amplifier zero, fZ2, also is 4.64 kHz:

$$R4 = \frac{1}{2 \times \pi \times f_{Z2} \times C11} = 612\ \Omega \Rightarrow 650\ \Omega$$

The two high frequency poles are placed well after the crossover frequency but less than the switching frequency. The first one kills the effect of the ESR zero at 19.3 kHz:

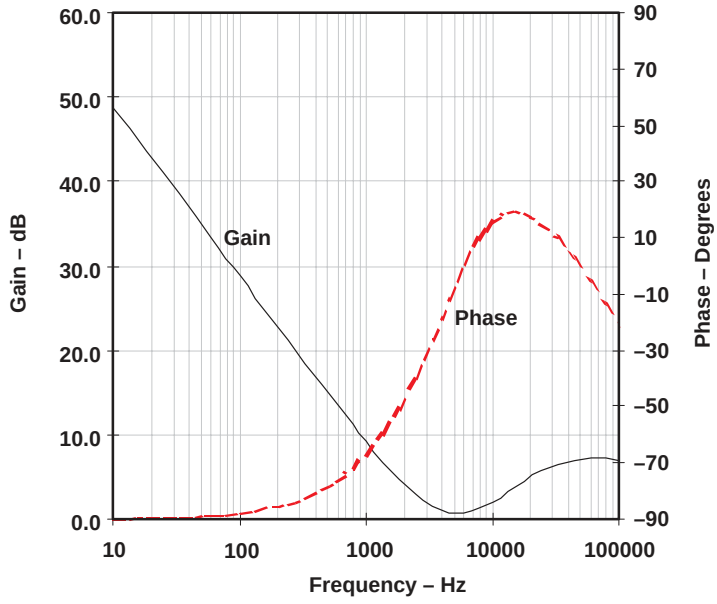
$$R9 = \frac{1}{2 \times \pi \times f_{ESR} \times C13} = 375\ \Omega \Rightarrow 300\ \Omega$$

The second is an optional high-frequency roll-off filter positioned about half of the operating frequency. Assuming that C8 is much smaller than C11, then the series combination of these capacitors is approximately equal to C8, therefore:

$$C8 = \frac{1}{2 \times \pi \times f_{P3} \times R4} = 1280\ pF \Rightarrow 1500\ pF$$

A graph of the error–amplifier response is given in Figure 2–4. The solid line is the gain and the dashed line is the phase.

Figure 2–4. Error-Amplifier Frequency Response



The overall open-loop frequency response of the converter is the product of the uncompensated open-loop response (Figure 2–2) and the error amplifier response (Figure 2–4). A Bode plot of the overall open loop frequency response of the converter is shown below in Figure 2–5. Again, the solid line is the gain and the dashed line is the phase. As seen in the graph, the gain crosses 0 dB in the vicinity of 20 kHz and the phase margin is approximately 100 degrees.

It should be emphasized that the power stage gain and hence the overall loop gain is dependent on input voltage, output voltage, output load resistance, and parasitic resistances present in the power stage and external components. The graph below represents a typical operating condition. However, it is good design practice to check for stability at the line voltage extremes and limits of output voltage settings and loads to ensure that variations do not cause problems.

Figure 2–5. System Frequency Response