LMC6464QML Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

Check for Samples: LMC6464QML

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Low Offset Voltage 500µV**
- **Ultra Low Supply Current 23 µA/Amplifier**
- **Operates from 3V to 15V Single Supply**
- **Rail-to-Rail Output Swing**
  - **(within 10 mV of Rail, V_S = 5V and R_L = 25 KΩ)**
- **Low Input Bias Current 150 fA**

APPLICATIONS

- **Battery Operated Circuits**
- **Transducer Interface Circuits**
- **Portable Communication Devices**
- **Medical Applications**
- **Battery Monitoring**

DESCRIPTION

The LMC6464 is a micropower version of the popular LMC6484, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6464 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, ensured for loads down to 25 KΩ, assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6464 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6464, with ensured specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60 µW per amplifier (at V_S = 3V) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.

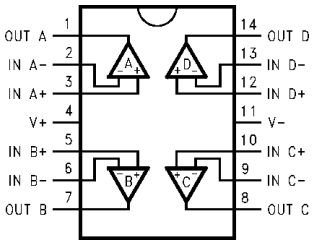


Figure 1. 14-Pin CDIP Top View

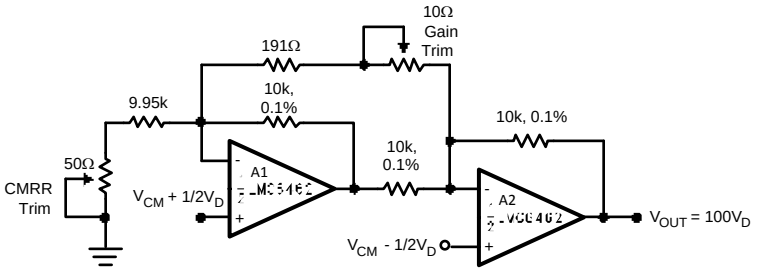


Figure 2. Low-Power Two-Op-Amp Instrumentation Amplifier

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage ($V^+ - V^-$)			16V
Differential Input Voltage			± Supply Voltage
Voltage at Input/Output Pin			$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Input Pin (2)			±5 mA
Current at Output Pin (3) (4)			±30 mA
Current at Power Supply Pin			40 mA
Junction Temperature (3), (5)			150°C
Power Dissipation (5)	LMC6464		6mW
Thermal Resistance (6)	θ_{JA}	14LD CDIP (Still Air)	74°C/W
		14LD CDIP (500LF/Min Air flow)	37°C/W
	θ_{JC}	14LD CDIP	8°C/W
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Lead Temp. (Soldering, 10 sec.)			260°C
ESD Tolerance (7)			2.0 KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(3) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(6) All numbers apply for packages soldered directly into a PC board.
(7) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Range (1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Operating Temperature Range	$-55°C \le T_A \le +125°C$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LMC6464 Electrical Characteristics DC Parameters: 3 Volt

The following conditions apply, unless otherwise specified. $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				0.8	mV	1
					1.7	mV	2
I_{IB}	Input Bias Current		(1)		25	pA	1
			(1)		100	pA	2
I_{IO}	Input Offset Current		(1)		25	pA	1
			(1)		100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3.0V$		60		dB	1
				57		dB	2, 3
V_{CM}	Input Common Mode Voltage Range	For CMRR ≥ 50 dB		3.0	0.0	V	1
				2.9	0.1	V	2, 3
V_{Op}	Output Swing	$R_L = 25K\Omega$ to $V^+/2$		2.9	0.10	V	1
				2.8	0.15	V	2, 3
I_{CC}	Supply Current	$V_O = V^+/2$			110	µA	1
					140	µA	2, 3
I_{SC}	Output Short Circuit Current	Sourcing $V_O = 0V$		8.0		mA	1
				6.0		mA	2, 3
		Sinking $V_O = 3V$		23		mA	1
				17		mA	2, 3

(1) Limits are dictated by testing limitations and not device performance.

LMC6464 Electrical Characteristics DC Parameters: 5 Volt

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				0.5	mV	1
					1.4	mV	2, 3
I_{IB}	Input Bias Current		(1)		25	pA	1
			(1)		100	pA	2, 3
I_{IO}	Input Offset Current		(1)		25	pA	1
			(1)		100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 5.0V$		70		dB	1
				67		dB	2, 3
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB		5.25	-0.10	V	1
				5.00	0.00	V	2, 3
V_{Op}	Output Swing	R_L = 100KΩ to $V^+/2$		4.990	0.010	V	1
				4.980	0.020	V	2, 3
		R_L = 25KΩ to $V^+/2$		4.975	0.020	V	1
				4.965	0.035	V	2, 3
I_{CC}	Supply Current	$V_O = V^+/2$			110	µA	1
					140	µA	2, 3
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V		19		mA	1
				15		mA	2, 3
		Sinking V_O = 5V		22		mA	1
				17		mA	2, 3

(1) Limits are dictated by testing limitations and not device performance.

LMC6464 Electrical Characteristics DC Parameters: 15 Volt

The following conditions apply, unless otherwise specified. $V^+ = 15V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				1.8	mV	1
					2.3	mV	2, 3
I_{IB}	Input Bias Current		(1)		25	pA	1
			(1)		100	pA	2, 3
I_{IO}	Input Offset Current		(1)		25	pA	1
			(1)		100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$		70		dB	1
				67		dB	2, 3
V_{CM}	Input Common Mode Voltage Range	For CMRR ≥ 50dB		15.25	-0.15	V	1
				15.00	0.00	V	2, 3
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, V^-= 0V, V_O = 2.5V		70		dB	1
				67		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	$-15V \le V^- \le -5V$, V^+ = 0V, V_O = -2.5V		70		dB	1
				67		dB	2, 3

(1) Limits are dictated by testing limitations and not device performance.

LMC6464 Electrical Characteristics DC Parameters: 15 Volt (continued)

The following conditions apply, unless otherwise specified. $V^+ = 15V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{Op}	Output Swing	$R_L = 100K\Omega$ to $V^+/2$		14.975	0.025	V	1
				14.965	0.035	V	2, 3
		$R_L = 25K\Omega$ to $V^+/2$		14.900	0.050	V	1
				14.850	0.150	V	2, 3
I_{CC}	Supply Current	$V_O = V^+/2$			120	µA	1
					140	µA	2, 3
I_{SC}	Output Short Circuit Current	Sourcing $V_O = 0V$		24		mA	1
				17		mA	2, 3
		Sinking $V_O = 12V$	(2)	55		mA	1
			(2)	45		mA	2, 3
A_V	Large Signal Voltage Gain	Sourcing $R_L = 100K\Omega$	(3)	110		dB	1
			(3)	80		dB	2, 3
		Sinking $R_L = 100K\Omega$	(3)	100		dB	1
			(3)	70		dB	2, 3
		Sourcing $R_L = 25K\Omega$	(3)	110		dB	1
			(3)	70		dB	2, 3
		Sinking $R_L = 25K\Omega$	(3)	95		dB	1
			(3)	60		dB	2, 3

(2) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(3) $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

LMC6464 Electrical Characteristics AC Parameters: 15 Volt

The following conditions apply, unless otherwise specified.
DC: $V^+ = 15V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate		(1)	15		V/mS	4
			(1)	7.0		V/mS	5, 6
GBW	Gain-Bandwidth			60		KHz	4
				45		KHz	5, 6

(1) Device configured as a Voltage Follower with a 10V input step. For positive slew, V_I swing is 2.5V to 12.5V, V_O is measured between 6.0V and 9.0V. For negative slew, V_I swing is 12.5V to 2.5V, V_O is measured between 9.0V and 6.0V.

Typical Performance Characteristics

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

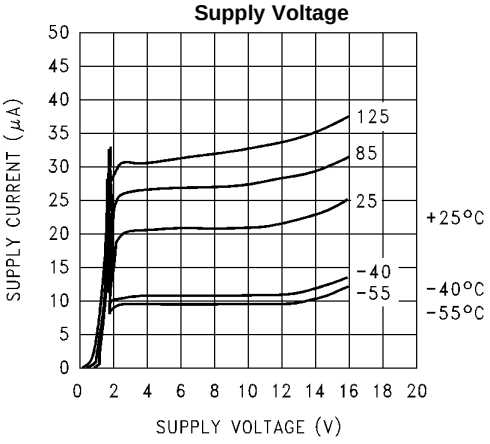


Figure 3.

Sourcing Current vs. Output Voltage

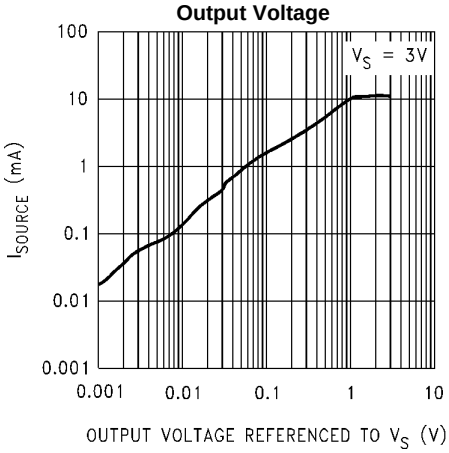


Figure 4.

Sourcing Current vs. Output Voltage

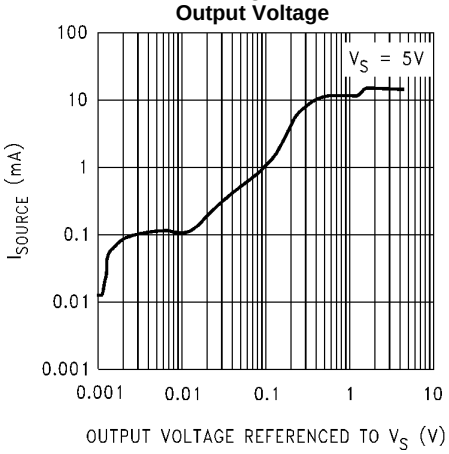


Figure 5.

Sourcing Current vs. Output Voltage

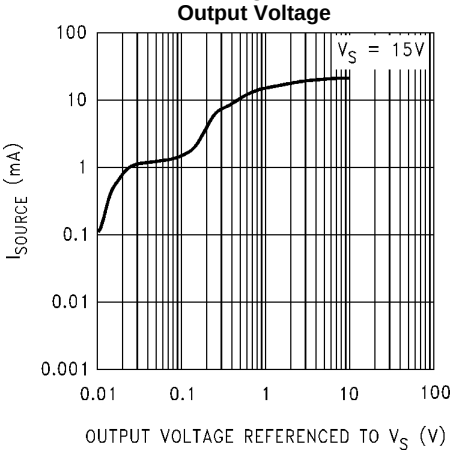


Figure 6.

Sinking Current vs. Output Voltage

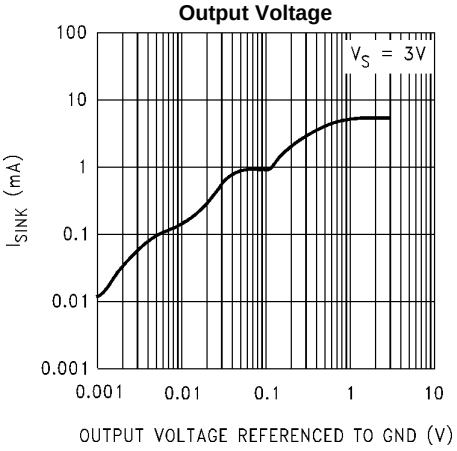


Figure 7.

Sinking Current vs. Output Voltage

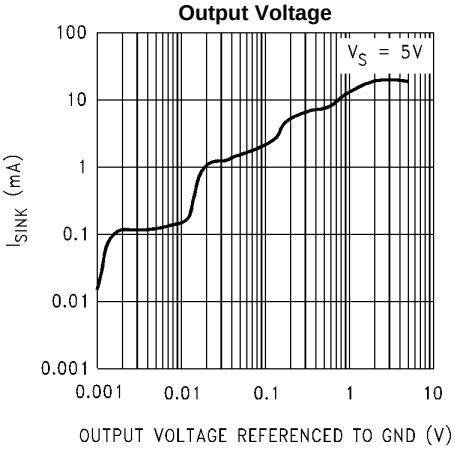


Figure 8.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Sinking Current vs. Output Voltage

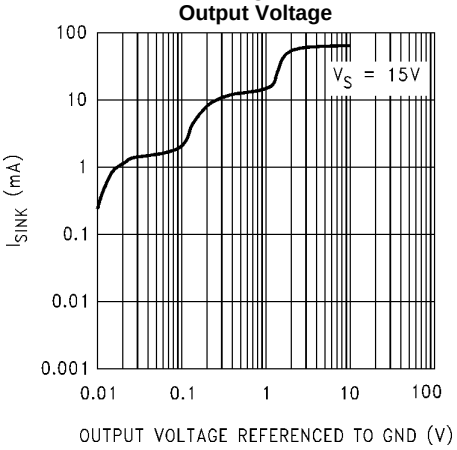


Figure 9.

Input Voltage Noise vs Frequency

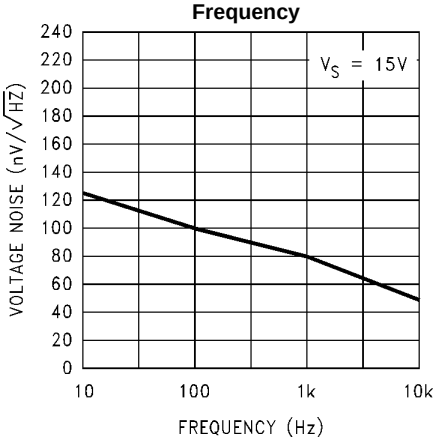


Figure 10.

Input Voltage Noise vs. Input Voltage

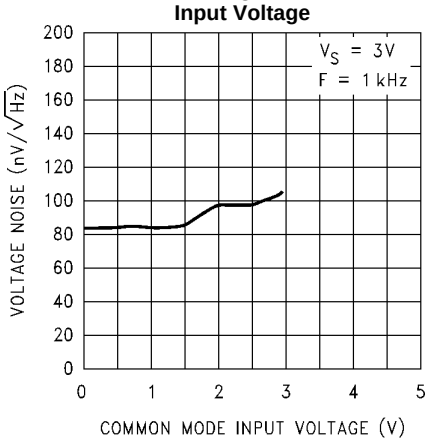


Figure 11.

Input Voltage Noise vs. Input Voltage

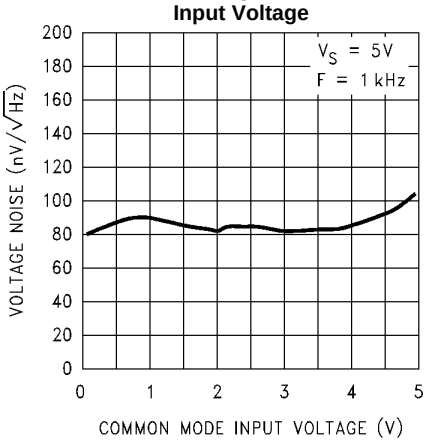


Figure 12.

Input Voltage Noise vs. Input Voltage

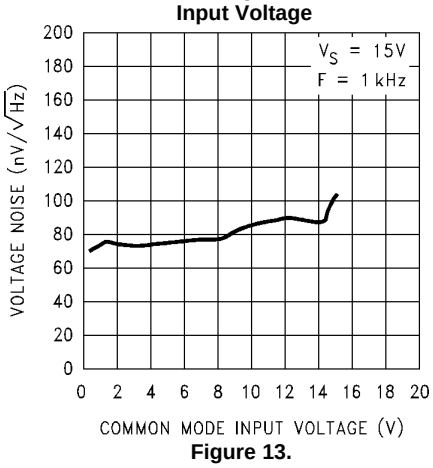


Figure 13.

ΔV_{OS} vs CMR

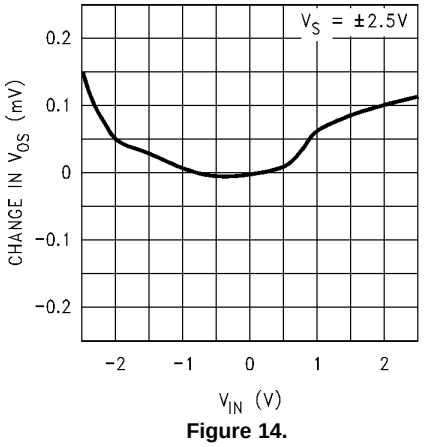


Figure 14.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage vs. Output Voltage

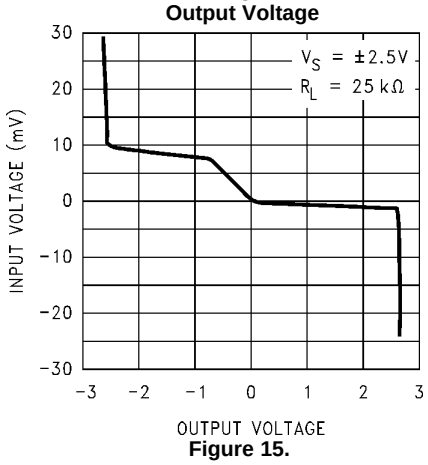


Figure 15.

Open Loop Frequency Response

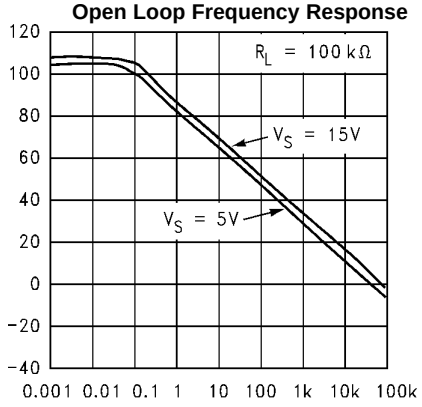


Figure 16.

Open Loop Frequency Response vs. Temperature

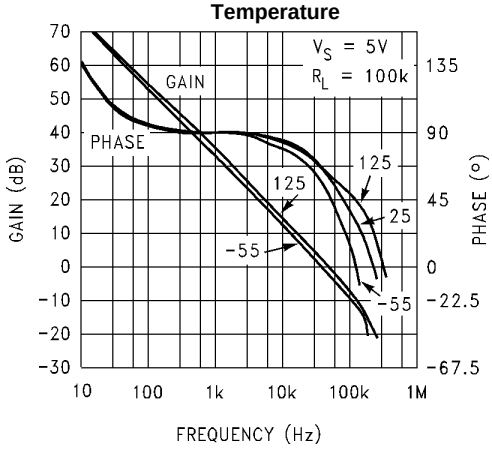


Figure 17.

Gain and Phase vs. Capacitive Load

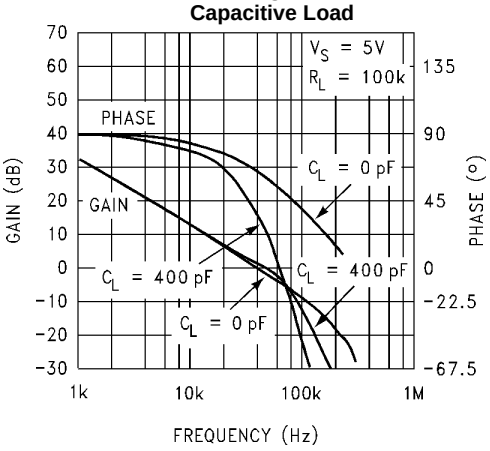


Figure 18.

Slew Rate vs. Supply Voltage

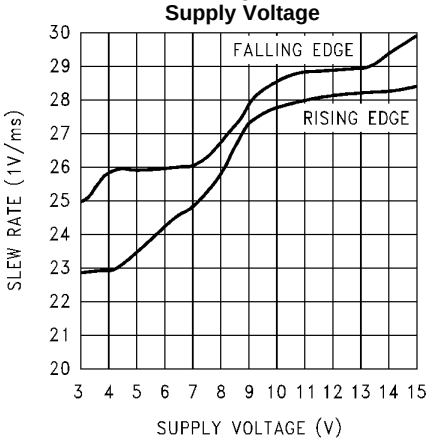


Figure 19.

Non-Inverting Large Signal Pulse Response

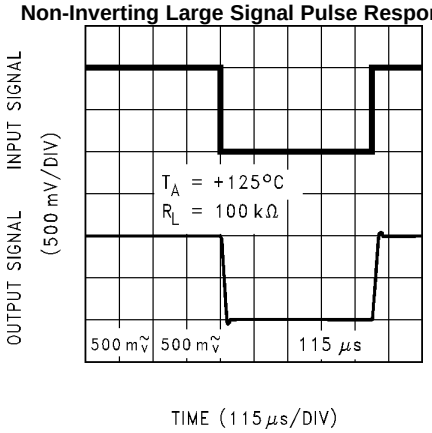


Figure 20.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Non-Inverting Large Signal Pulse Response

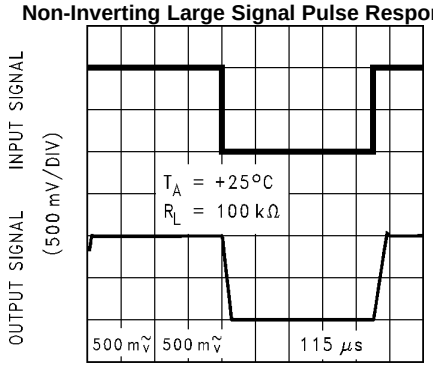


Figure 21.

Non-Inverting Large Signal Pulse Response

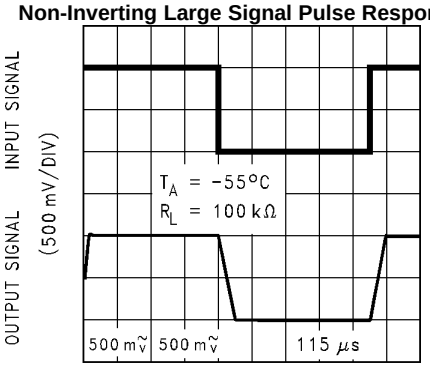


Figure 22.

Non-Inverting Small Signal Pulse Response

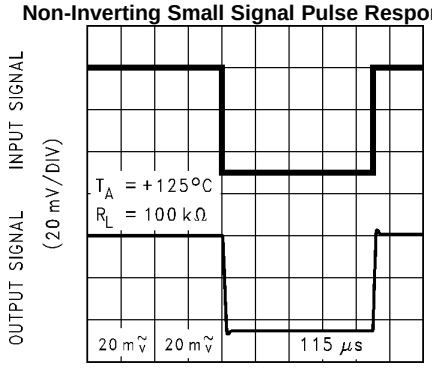


Figure 23.

Non-Inverting Small Signal Pulse Response

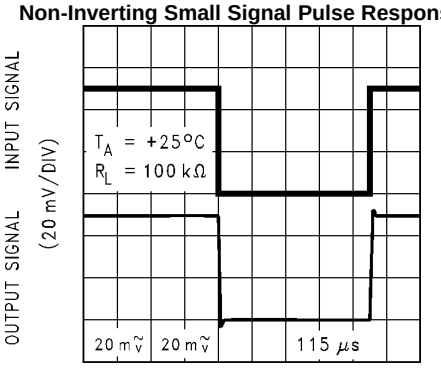


Figure 24.

Non-Inverting Small Signal Pulse Response

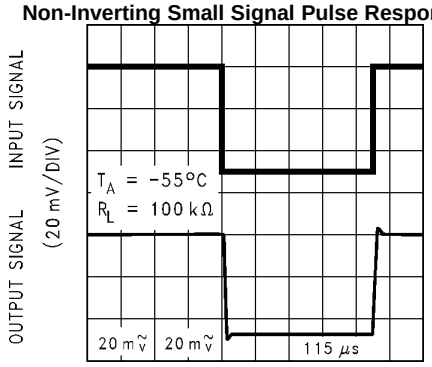


Figure 25.

Inverting Large Signal Pulse Response

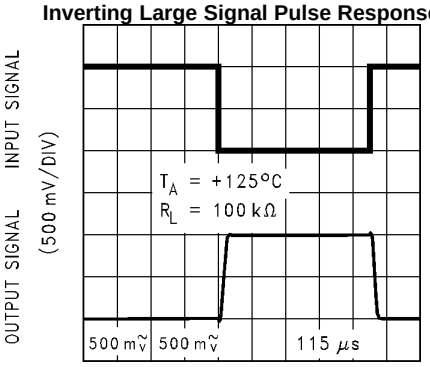


Figure 26.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Inverting Large Signal Pulse Response

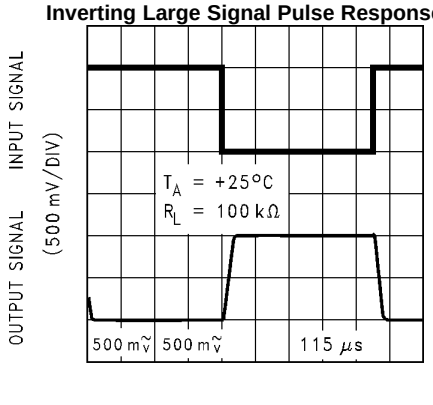


Figure 27.

Inverting Large Signal Pulse Response

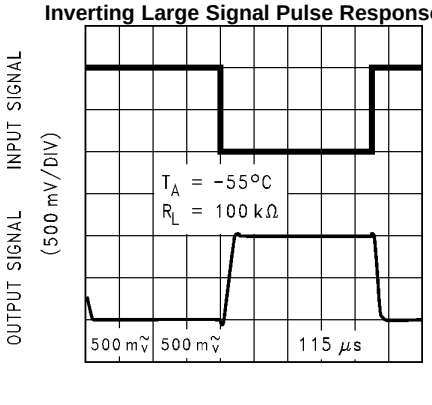


Figure 28.

Inverting Small Signal Pulse Response

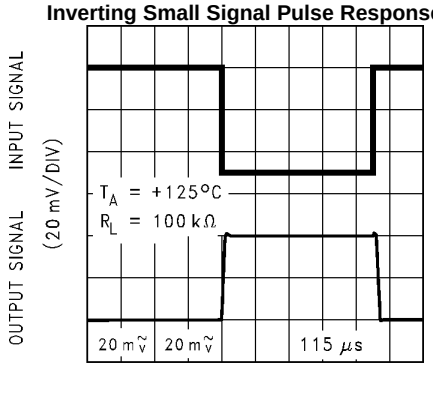


Figure 29.

Inverting Small Signal Pulse Response

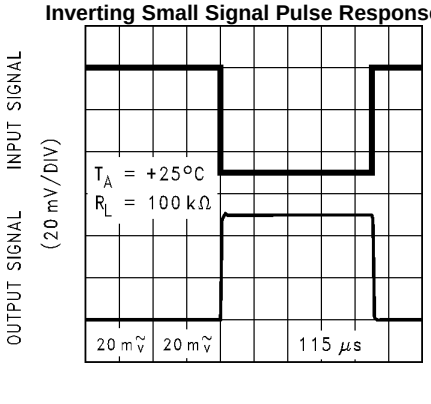


Figure 30.

Inverting Small Signal Pulse Response

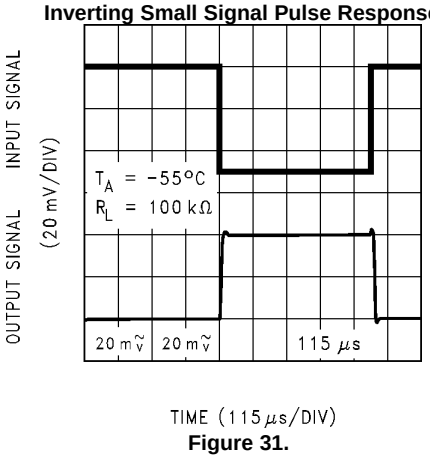


Figure 31.

APPLICATION INFORMATION

INPUT COMMON-MODE VOLTAGE RANGE

The LMC6464 has a rail-to-rail input common-mode voltage range. Figure 32 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

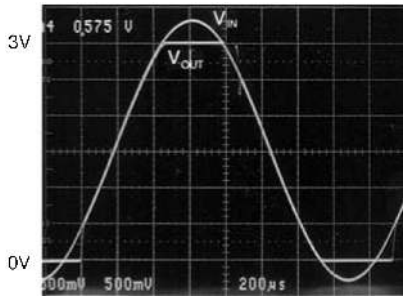


Figure 32. An Input Voltage Signal Exceeds the LMC6464 Power Supply Voltage with No Output Phase Inversion

The absolute maximum input voltage at V^+ = 3V is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 33, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to ±5 mA, with an input resistor, as shown in Figure 34.

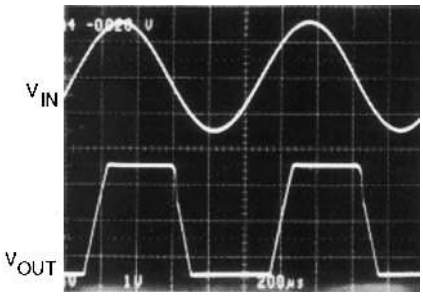


Figure 33. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in Figure 34 Causing No Phase Inversion Due to R_I

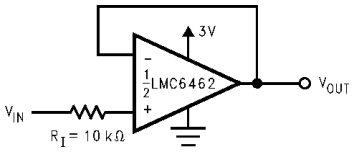


Figure 34. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

The approximated output resistance of the LMC6464 is 180Ω sourcing, and 130Ω sinking at V_S = 3V, and 110Ω sourcing and 83Ω sinking at V_S = 5V. The maximum output swing can be estimated as a function of load using the calculated output resistance.

CAPACITIVE LOAD TOLERANCE

The LMC6464 can typically drive a 200 pF load with V_S = 5V at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 35. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

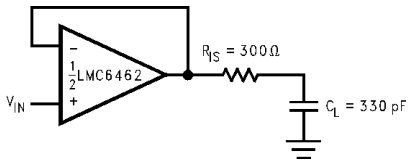


Figure 35. Resistive Isolation of a 300 pF Capacitive Load

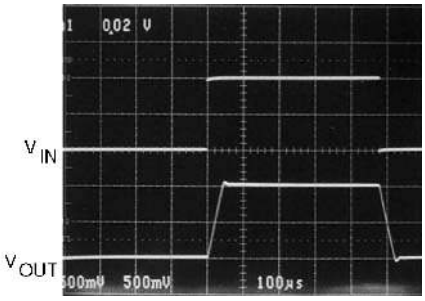


Figure 36. Pulse Response of the LMC6464 Circuit Shown in Figure 35

Figure 36 displays the pulse response of the LMC6464 circuit in Figure 35.

Another circuit, shown in Figure 37, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in Figure 35 because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.

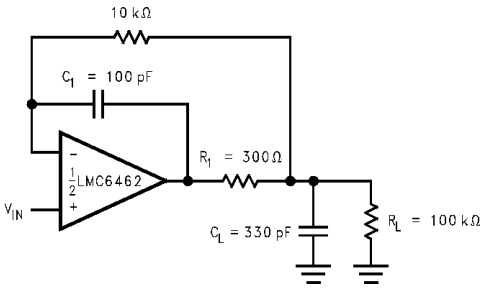


Figure 37. LMC6464 Non-Inverting Amplifier, Compensated to Handle a 300 pF Capacitive and 100 KΩ Resistive Load

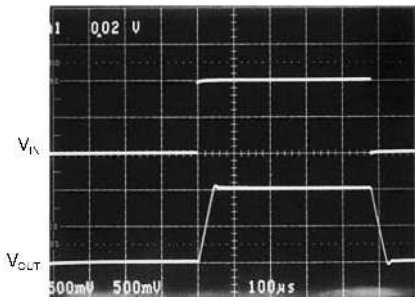


Figure 38. Pulse Response of LMC6464 Circuit in Figure 37

The pulse response of the circuit shown in Figure 37 is shown in Figure 38.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6464. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

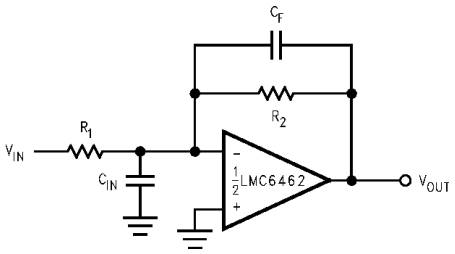


Figure 39. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 39), C_F, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F} \quad (1)$$

or

$$R_1 C_I \leq R_2 C_F \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

OFFSET VOLTAGE ADJUSTMENT

Offset voltage adjustment circuits are illustrated in Figure 40 and Figure 41. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

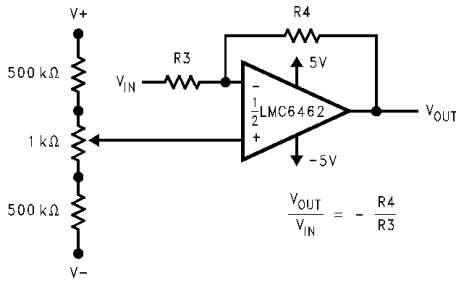


Figure 40. Inverting Configuration, Offset Voltage Adjustment

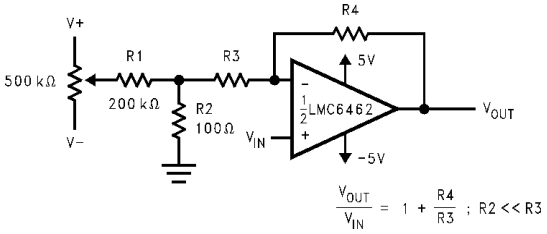


Figure 41. Non-Inverting Configuration, Offset Voltage Adjustment

SPICE MACROMODEL

A Spice macromodel is available for the LMC6464. This model includes a simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact the Texas Instruments Customer Response Center to obtain an operational amplifier Spice model library disk.

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6464, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6464's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 42. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 30 times degradation from the LMC6464's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Typical Connections of Guard Rings for standard op-amp configurations.

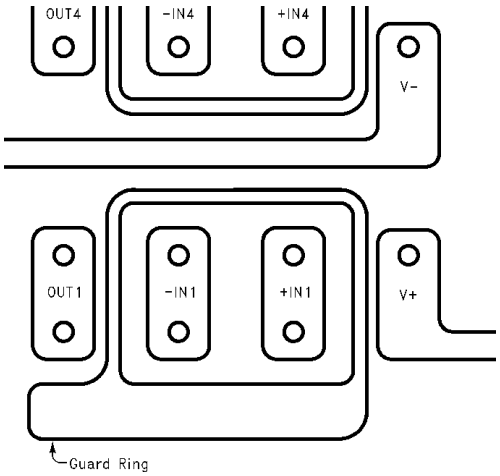


Figure 42. Example of Guard Ring in P.C. Board Layout

Typical Connections of Guard Rings

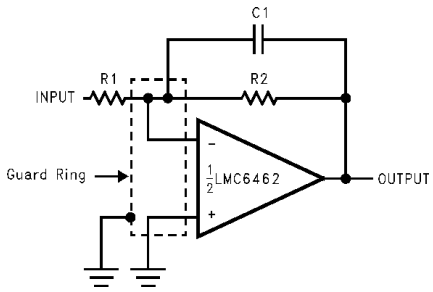


Figure 43. Inverting Amplifier

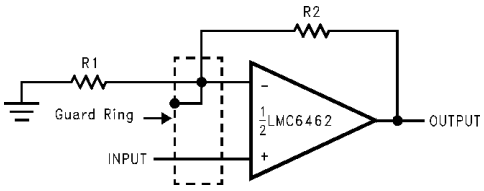


Figure 44. Non-Inverting Amplifier

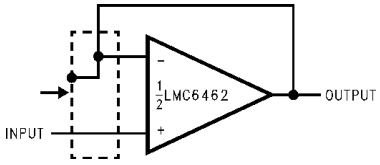
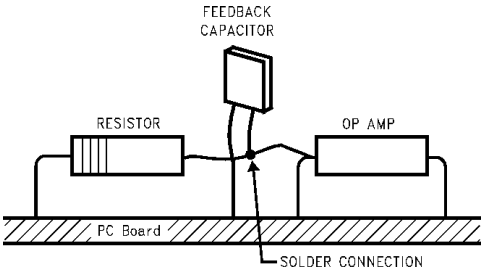


Figure 45. Follower

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 46.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 46. Air Wiring

INSTRUMENTATION CIRCUITS

The LMC6464 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6464 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6464 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_G to set the differential gain of the three op-amp instrumentation circuit in Figure 47. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

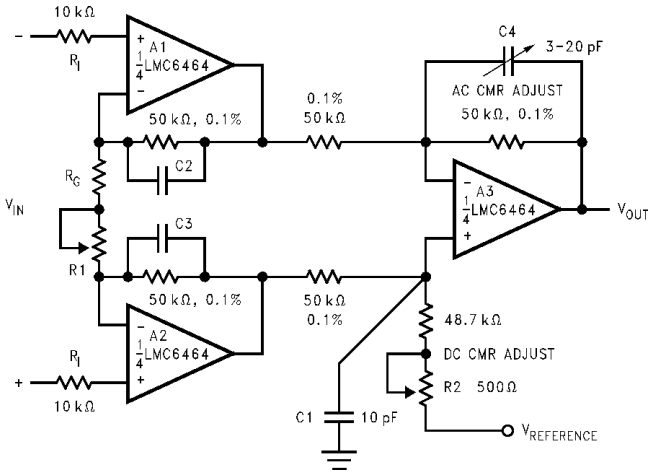


Figure 47. Low Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 48. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

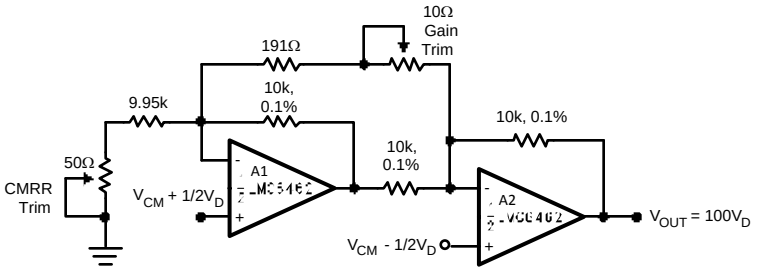


Figure 48. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications

TRANSDUCER INTERFACE CIRCUITS

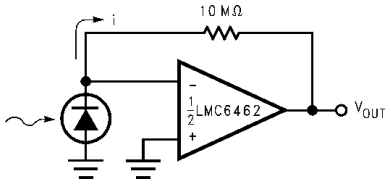


Figure 49. Photo Detector Circuit

Photocells can be used in portable light measuring instruments. The LMC6464, which can be operated off a battery, is an excellent choice for this circuit because of its very low input current and offset voltage.

LMC6464 AS A COMPARATOR

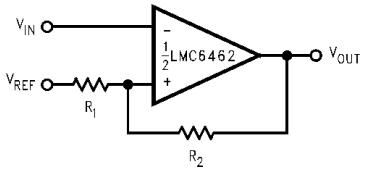


Figure 50. Comparator with Hysteresis

Figure 50 shows the application of the LMC6464 as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC6464 can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

HALF-WAVE AND FULL-WAVE RECTIFIERS

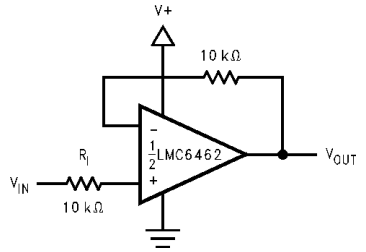


Figure 51. Half-Wave Rectifier with Input Current Protection (R_I)

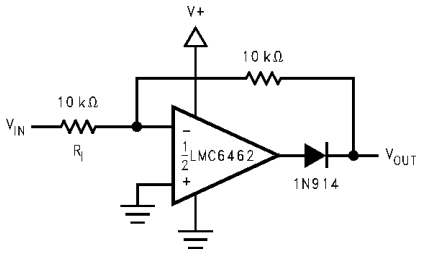


Figure 52. Full-Wave Rectifier with Input Current Protection (R_I)

In Figure 51 Figure 52, R_I limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

PRECISION CURRENT SOURCE

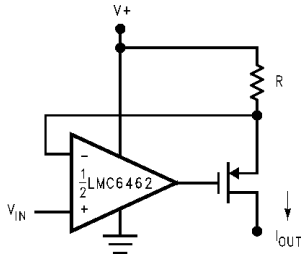


Figure 53. Precision Current Source

The output current I_{OUT} is given by:

$$I_{OUT} = \left(\frac{V^+ - V_{IN}}{R}\right) \quad (3)$$

OSCILLATORS

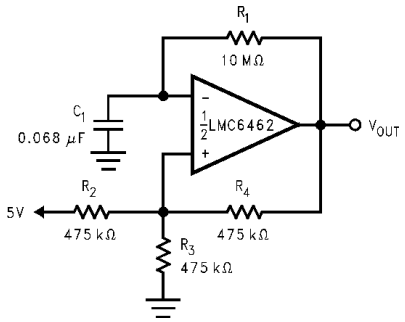


Figure 54. 1 Hz Square-Wave Oscillator

For single supply 5V operation, the output of the circuit will swing from 0V to 5V. The voltage divider set up R_2, R_3 and R_4 will cause the non-inverting input of the LMC6464 to move from 1.67V (⅓ of 5V) to 3.33V (⅔ of 5V). This voltage behaves as the threshold voltage.

R_1 and C_1 determine the time constant of the circuit. The frequency of oscillation, f_{Osc} is

$$\left(\frac{1}{2\Delta t}\right) \quad (4)$$

where Δt is the time the amplifier input takes to move from 1.67V to 3.33V. The calculations are shown below.

$$1.67 = 5\left(1 - e^{-\frac{t_1}{\tau}}\right) \quad (5)$$

where τ = RC = 0.68 seconds

$\rightarrow t_1$ = 0.27 seconds.

and

$$3.33 = 5\left(1 - e^{-\frac{t_2}{\tau}}\right) \quad (6)$$

$\rightarrow t_2$ = 0.75 seconds

Then,

$$f_{OSC} = \left(\frac{1}{2\Delta t}\right) \quad (7)$$

$$= \frac{1}{2\,(0.75 - 0.27)} \quad (8)$$

= 1 Hz

LOW FREQUENCY NULL

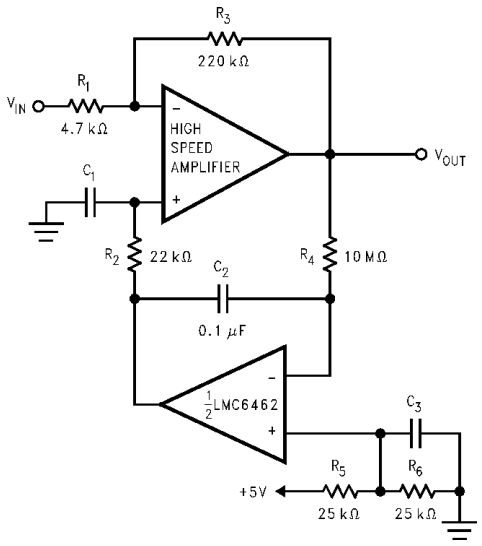


Figure 55. High Gain Amplifier with Low Frequency Null

Output offset voltage is the error introduced in the output voltage due to the inherent input offset voltage V_{OS}, of an amplifier.

Output Offset Voltage = (Input Offset Voltage) (Gain)

In the above configuration, the resistors R_5 and R_6 determine the nominal voltage around which the input signal, V_I should be symmetrical. The high frequency component of the input signal V_I will be unaffected while the low frequency component will be nulled since the DC level of the output will be the input offset voltage of the LMC6464 plus the bias voltage. This implies that the output offset voltage due to the top amplifier will be eliminated.

Table 1. Revision History

Released	Revision	Section	Changes
12/08/2010	A	New Release, Corporate format	1 MDS data sheets converted into one Corp. data sheet format. MNLMC6464AM-X Rev 1A1 will be archived.
03/26/2013	A	All	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9560302QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6464AMJ-QML 5962-9560302QCA Q	Samples
LMC6464AMJ-QML	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6464AMJ-QML 5962-9560302QCA Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

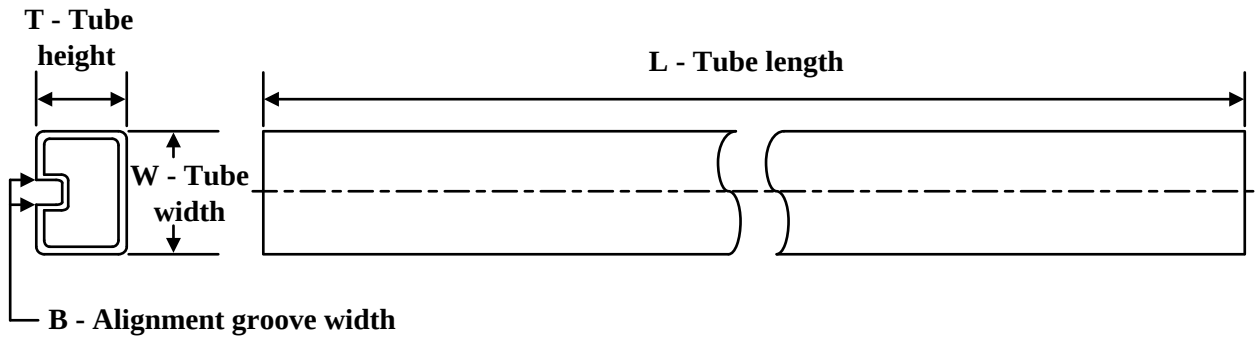
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



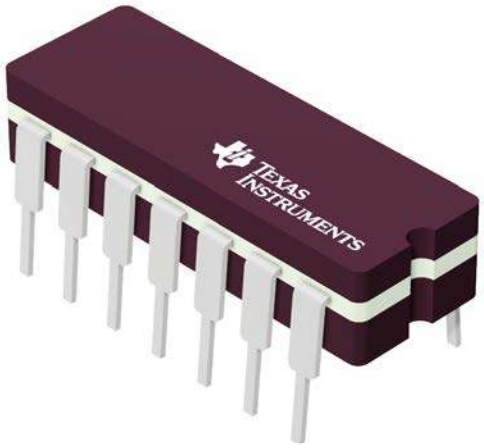
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9560302QCA	J	CDIP	14	25	506.98	15.24	13440	NA
LMC6464AMJ-QML	J	CDIP	14	25	506.98	15.24	13440	NA

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

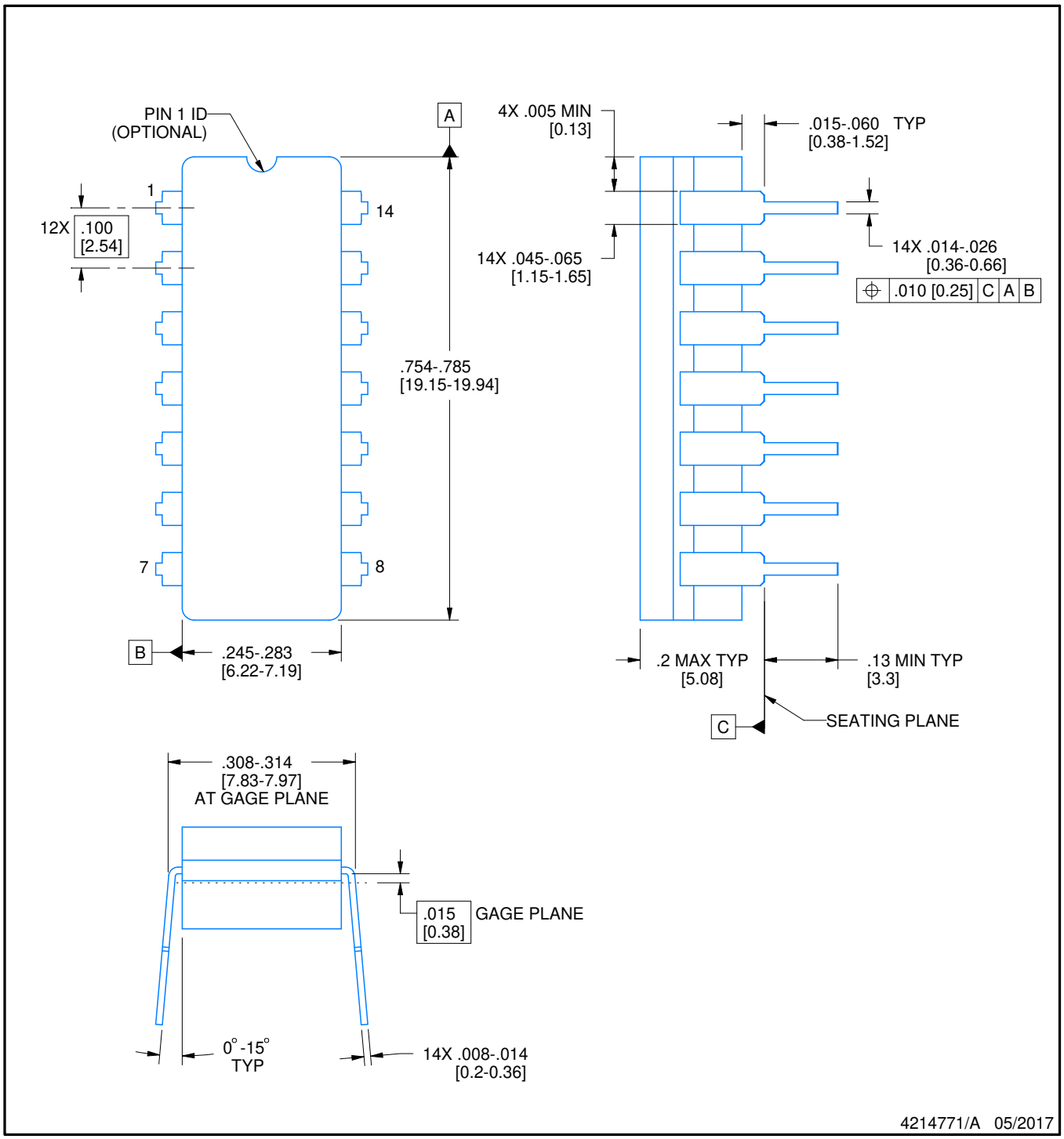
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

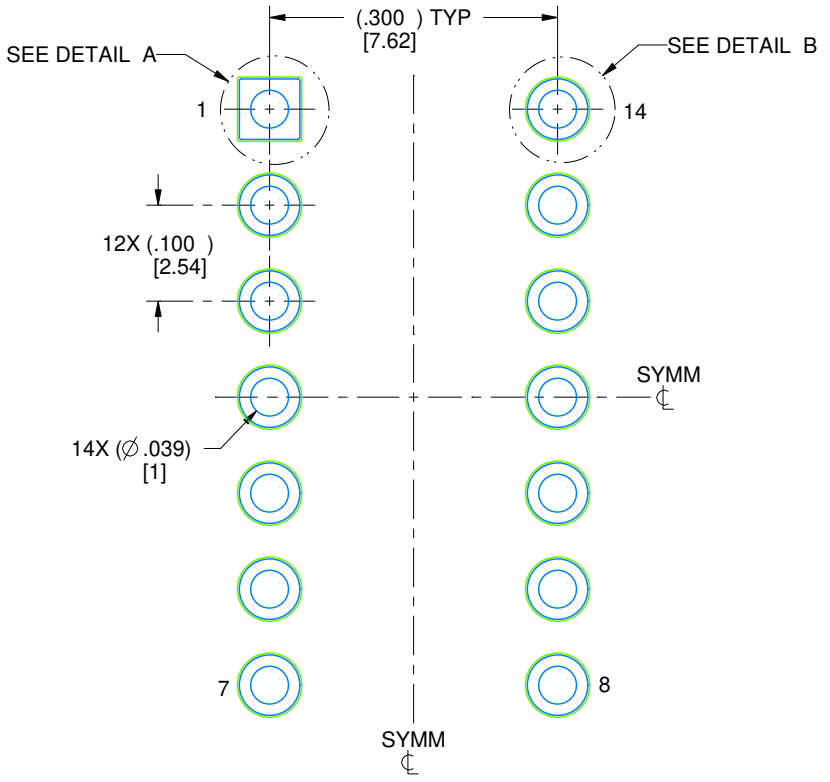
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

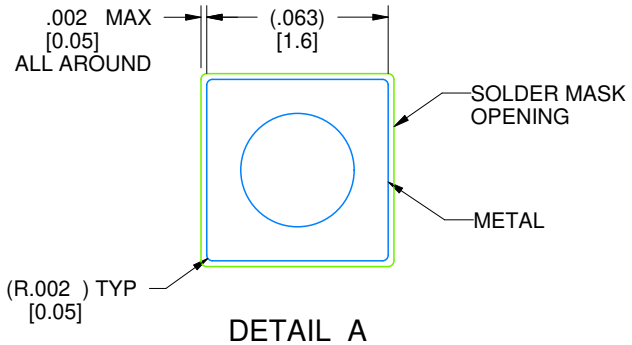
J0014A

CDIP - 5.08 mm max height

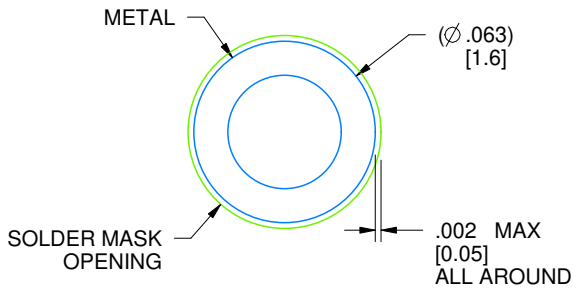
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265