

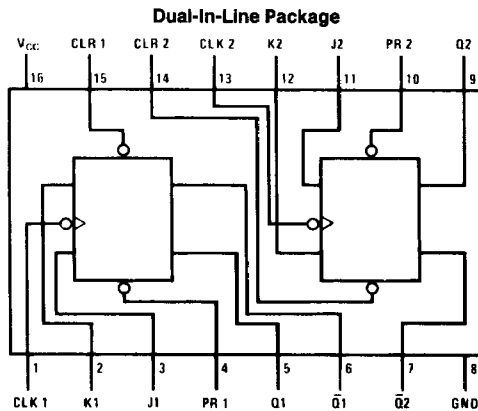
DM54S112/DM74S112 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K

inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram



Order Number DM54S112J or DM74S112N
See NS Package Number J16A or N16E

TL/F/6459-1

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	\bar{Q}_0

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q₀ = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	-55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S112			DM74S112			Units
			Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage		2			2			V
V _{IL}	Low Level Input Voltage				0.8			0.8	V
I _{OH}	High Level Output Current				-1			-1	mA
I _{OL}	Low Level Output Current				20			20	mA
f _{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f _{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t _w	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Clear Low	8			8			
		Preset Low	8			8			
t _w	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Clear Low	10			10			
		Preset Low	10			10			
t _{SU}	Setup Time (Notes 1 & 4)		7 ↓			7 ↓			ns
t _H	Input Hold Time (Notes 1 & 4)		0 ↓			0 ↓			ns
T _A	Free Air Operating Temperature		-55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54	2.5	3.4	V
			DM74	2.7	3.4	
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	J, K		50	μA
			Clear		100	
			Preset		100	
			Clock		100	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.5\text{V}$ (Note 4)	J, K		-1.6	mA
			Clear		-7	
			Preset		-7	
			Clock		-4	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54	-40	-100	mA
			DM74	-40	-100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)		30	50	mA

Note 1: All typicals are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics

at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to \bar{Q}		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to \bar{Q}		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \bar{Q}		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \bar{Q}		7		12	ns